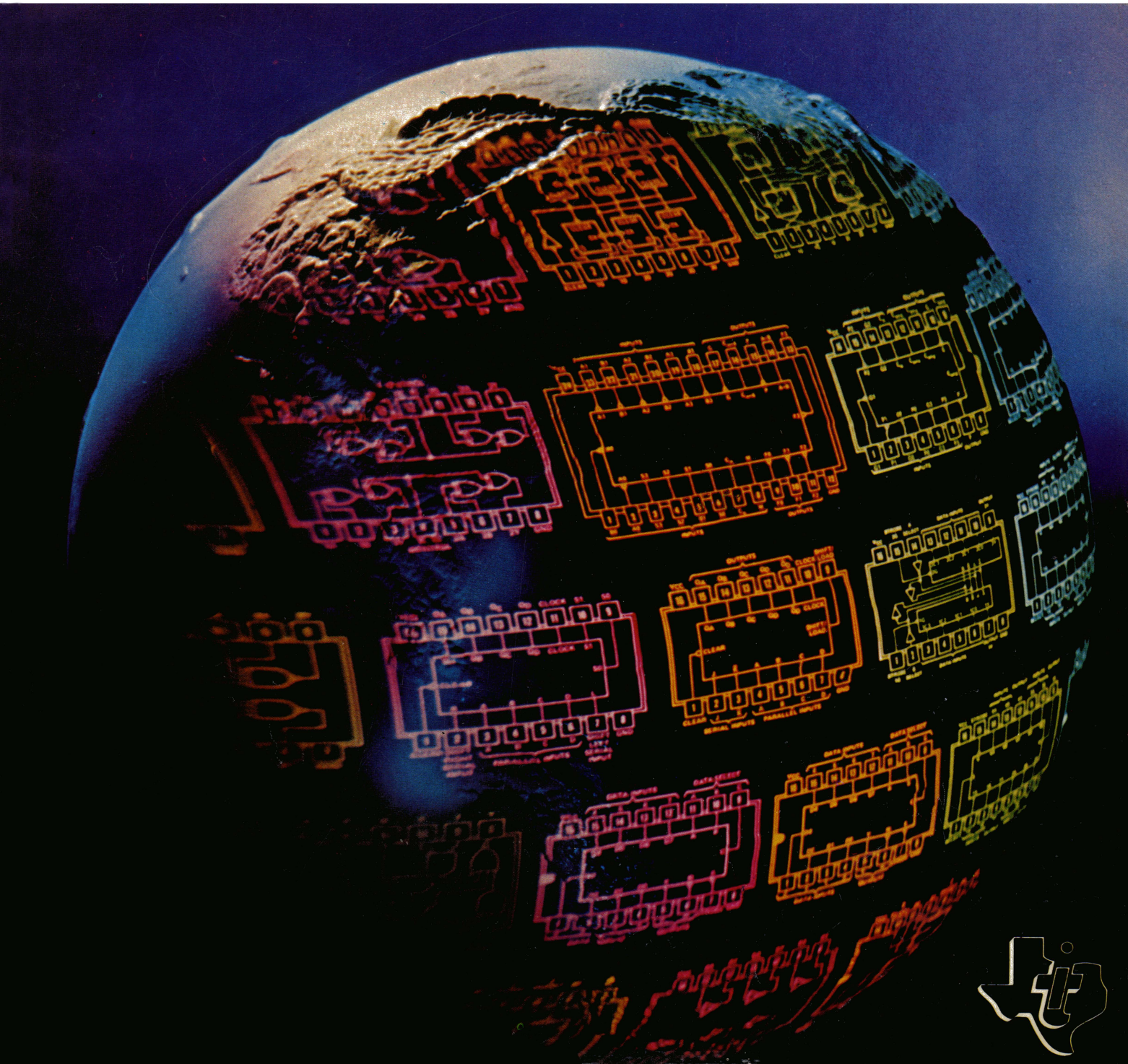
Recueil de notes d'applications
(vol. 5)

Texas Instruments



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Analyse et applications de la mémoire vive 64 Bits SN 7489
(NA 57)

LA MEMOIRE VIVE 64 BITS SN 7489

par M. Mairet

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I. Organisation de la mémoire SN 7489
II. Caractéristiques dynamiques
III. Extension de la mémoire SN 7489
IV. Applications de la mémoire SN 7489.

I. ORGANISATION DE LA MEMOIRE SN 7489 :

La mémoire SN 7489 est une mémoire TTL vive rapide de 64 bits constituée essentiellement :

- d'une matrice de 64 bascules organisées en 16 mots de 4 bits
- des circuits d'accès linéaire à cette matrice et de leur inhibition "Memory Enable"
- des circuits de lecture écriture associés à chaque bit et du signal de commande "Write Enable".

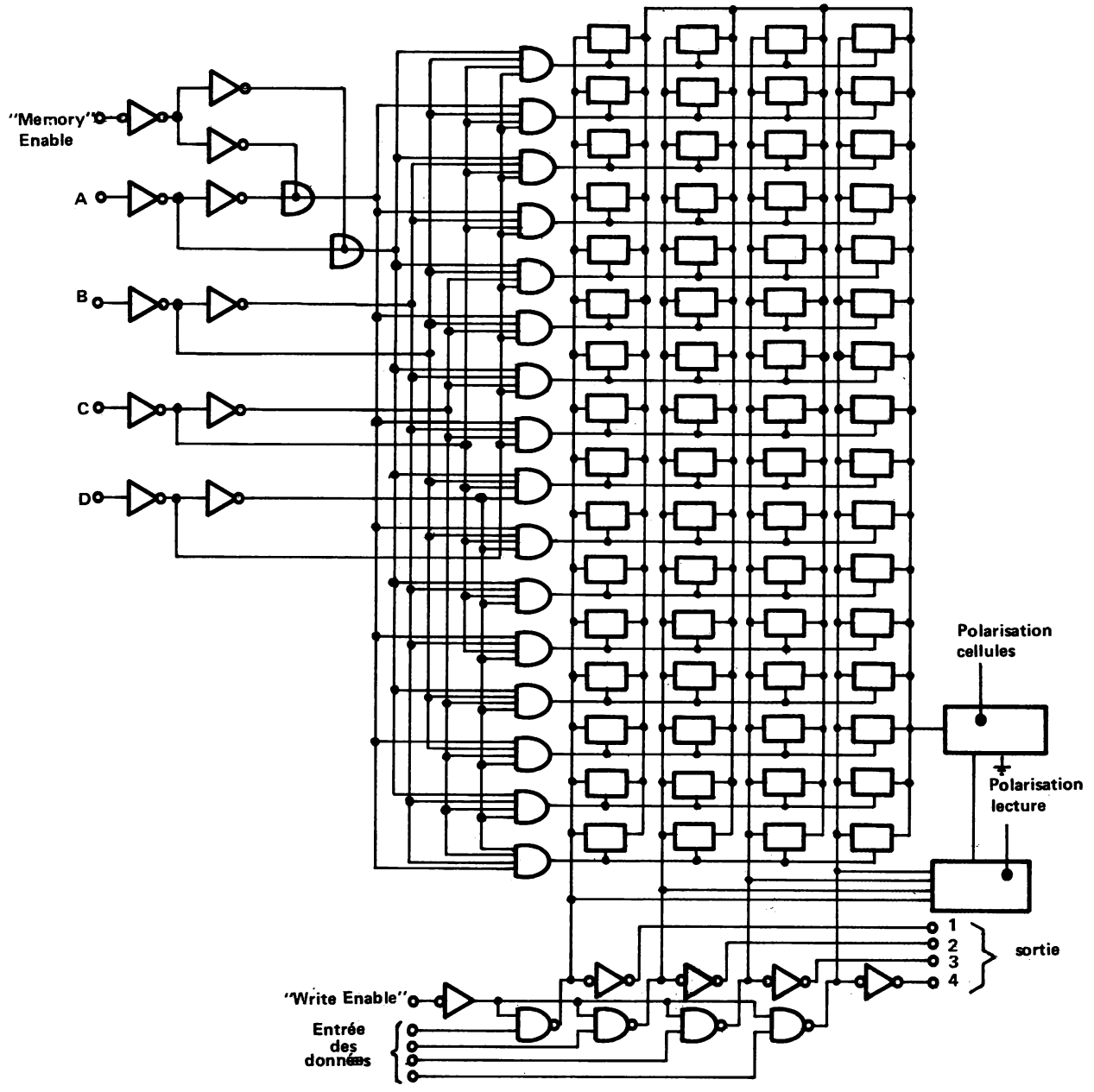
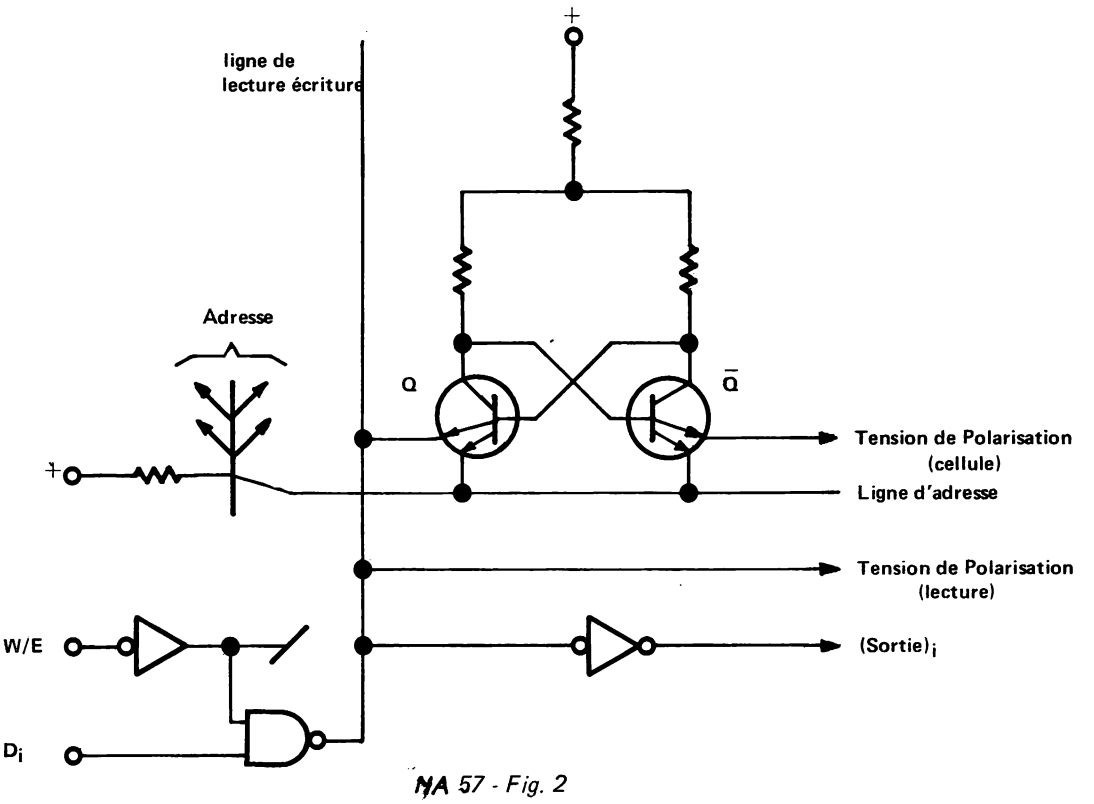


Fig. 1 - SN 7489 : ORGANISATION GENERALE



MA 57 - Fig. 2

La figure 2 montre la constitution d'une cellule élémentaire. Le flip flop est constitué de deux transistors rétrocouplés Q et $\bar{Q}$. Chacun de ces transistors a deux émetteurs. L'émetteur commun étant connecté à la ligne d'adresse, la sélection d'un mot, donc de 4 bascules, sera effective si la ligne d'adresse est à l'état "1". Les deux autres émetteurs sont reliés respectivement à une tension de seuil (de l'ordre du seuil TTL) commune à toutes les cellules pour $\bar{Q}$ et à un circuit de lecture écriture commun à tous les bits de même rang pour Q.

L'écriture d'un bit dans une bascule préalablement sélectionnée dépend de l'information présente sur D_i, quand "Write Enable" = "0". A un niveau "0" sur D_i correspond un niveau haut sur la ligne de lecture écriture; alors, l'action de la tension de seuil appliquée sur $\bar{Q}$ impose la conduction de $\bar{Q}$ et le blocage de Q. Un niveau "1" sur D_i, en appliquant un "0" sur la ligne de lecture rend Q conducteur et $\bar{Q}$ bloqué. Quand W/E revient à "1", le réseau de polarisation de la ligne de lecture maintient l'état final de la bascule de façon à éviter la perte de son information.

Si M.E = 0 et W.E = 1, l'émetteur Q_{ij} d'un flip flop sélectionné impose l'état de la sortie SO_i. Si Q est conducteur, SO_i est au niveau "0", si Q est bloqué, SO_i est au niveau "1".

Si M.E = 1, l'accès à la mémoire est impossible et les transistors de sortie sont bloqués si W.E. = 1. Si W.E. =0 les sorties SO_i indiquent le complément des informations présentes sur D_i.

Les différents fonctionnements précités sont résumés dans le tableau suivant (logique positive) :

M . E	W . E	Fonction	Sorties
0	1	Lecture	Complément du mot sélectionné
0	0	Ecriture	Complément des D_i
1	0	Inhibition du stockage	Complément des D_i
1	1	Aucune	niveau "1"

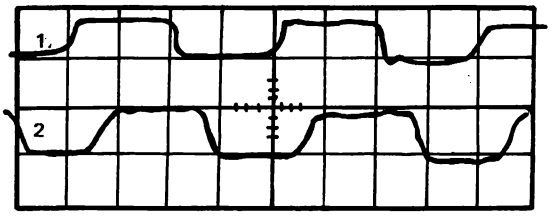
II. CARACTERISTIQUES DYNAMIQUES :

a) Lecture :

La lecture dans la mémoire SN 7489 peut être effectuée, soit à partir de l'adresse, le signal M E étant à "0", soit à partir du signal M.E, l'adresse désirée étant figée.

Le premier cas est indiqué sur la figure 3. Dans ces conditions, le temps de lecture (t_l) est la somme du temps d'accès t_a (35 ns typique) et du temps de traitement t_t

$$t_l = t_a + t_t.$$



1 - Adresse
2 - Sortie
H : 50 ns/div
V : 5 V/div
"Memory enable" = 0

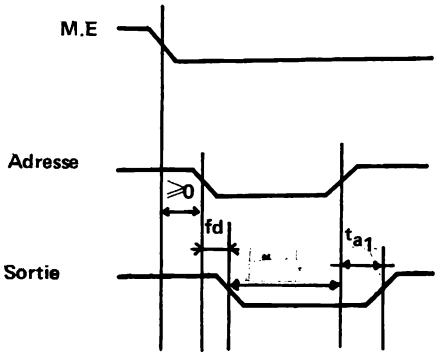
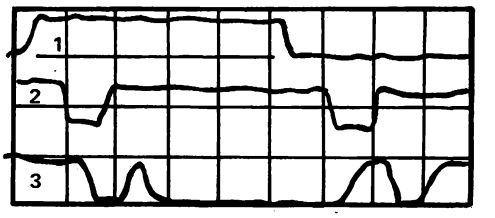


Fig. 3 : Lecture à partir de l'adresse

b) Ecriture :

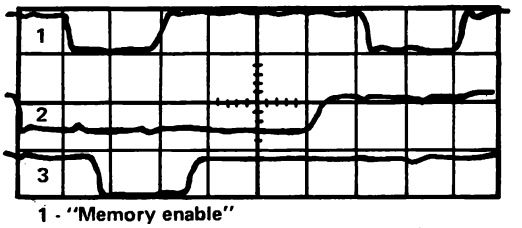
La figure 5 indique les signaux obtenus et le chronogramme dans le cas de l'écriture dans la mémoire. L'impulsion d'écriture doit avoir une durée au moins égale à 40 ns et être complètement incluse dans l'impulsion "donnée" D_i. Il existe un temps de recouvrement de lecture t_{sR} de durée inférieure ou égale à 48 ns dû aux circuits de lecture écriture. De toutes façons l'information est écrite dans la mémoire t_{WR} après la remontée de W.E. Le cycle d'écriture est donc $t_{set\text{-}up} + t_{WR}$.



1 - Entrée D
2 - Write Enable
3 - Sortie
H : 50 ns/div
V : 5 V /div

La figure 4 montre les signaux obtenus pour le deuxième cas; là aussi :

$$t_l = t_a + t_t$$



1 - "Memory enable"
2 - Adresse
3 - Sortie
H : 50 ns/div
V : 5V /div

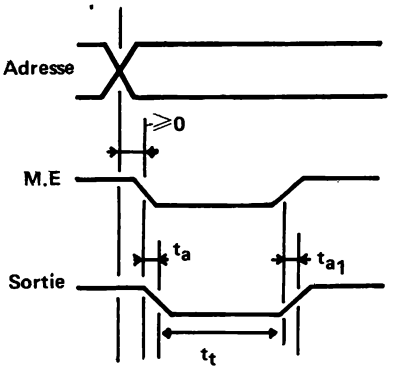


Fig. 4. Lecture à partir de "Memory Enable"

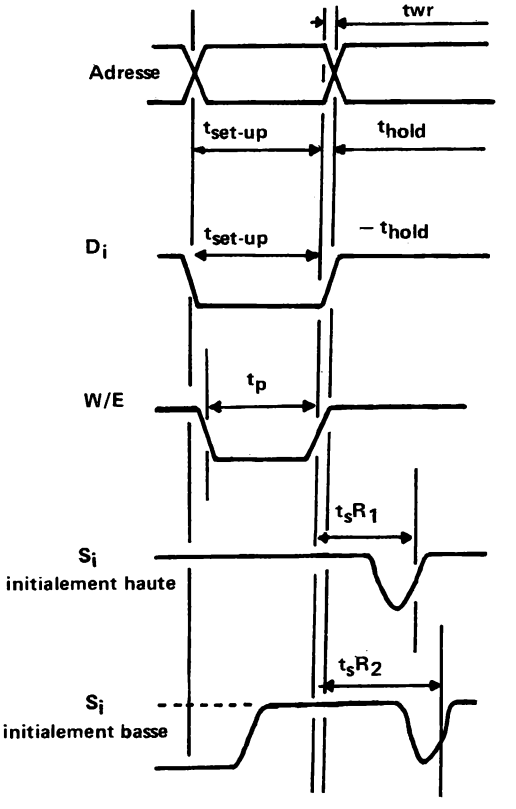


Fig. 5 - Cycle d'écriture

III. EXTENSION DE LA MEMOIRE SN 7489

La possibilité de réaliser la fonction "ET Connecté entre les sorties de la mémoire SN 7489 et la présence de l'entrée "Memory Enable" permettent la réalisation de mémoires de grande capacité. A titre d'exemple, la figure 6 montre la réalisation d'une mémoire de 16 mots de 16 bits obtenue simplement par interconnexions des entrées de sélection et "Memory Enable".

Le principe de l'extension du nombre de mots est montré sur la figure 7 qui représente une mémoire de 64 mots de 4 bits.

La sélection d'une mémoire SN 7489 parmi 4 est réalisée à l'aide d'un demi-boîtier SN 74155, adressé par les poids d'adresse E et F, dont les sorties commandent les entrées "Memory Enable". Les 4 autres poids d'adresse sont communs aux 4 mémoires ainsi que les signaux d'entrée D_1 à D_4.

Il est alors possible de connecter les sorties homologues entre elles et de réaliser la fonction "ET câblé" puisque les mémoires étant validées en séquence, seule une sortie peut être au niveau bas à un instant déterminé.

Le nombre maximum de sorties N_1 pouvant être reliées et la résistance de charge R_L dépendent de la possibilité d'absorption de courant (I_{sink}) du transistor de sortie et du nombre N_2 de charges TTL qui lui sont connectées.

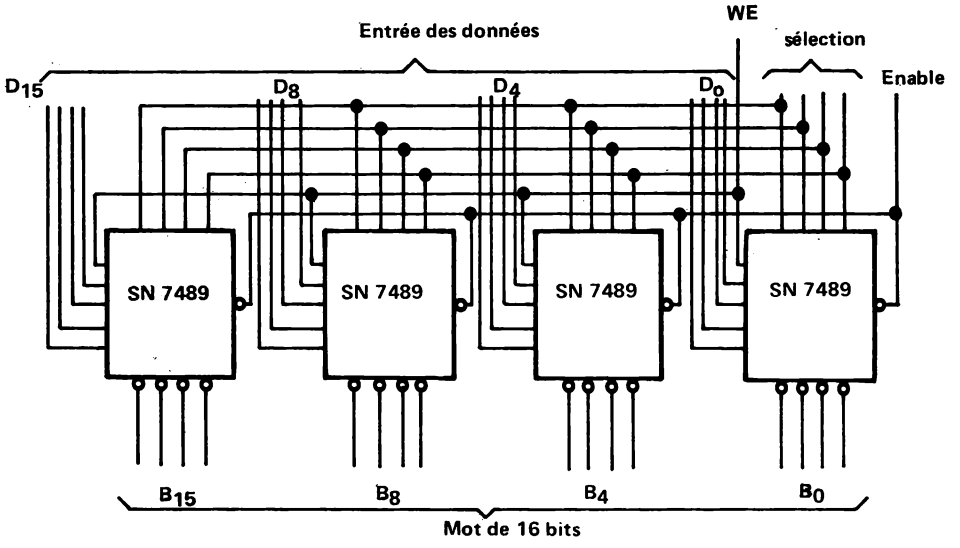


Fig. 6 - Mémoire de 16 Mots de 16 bits

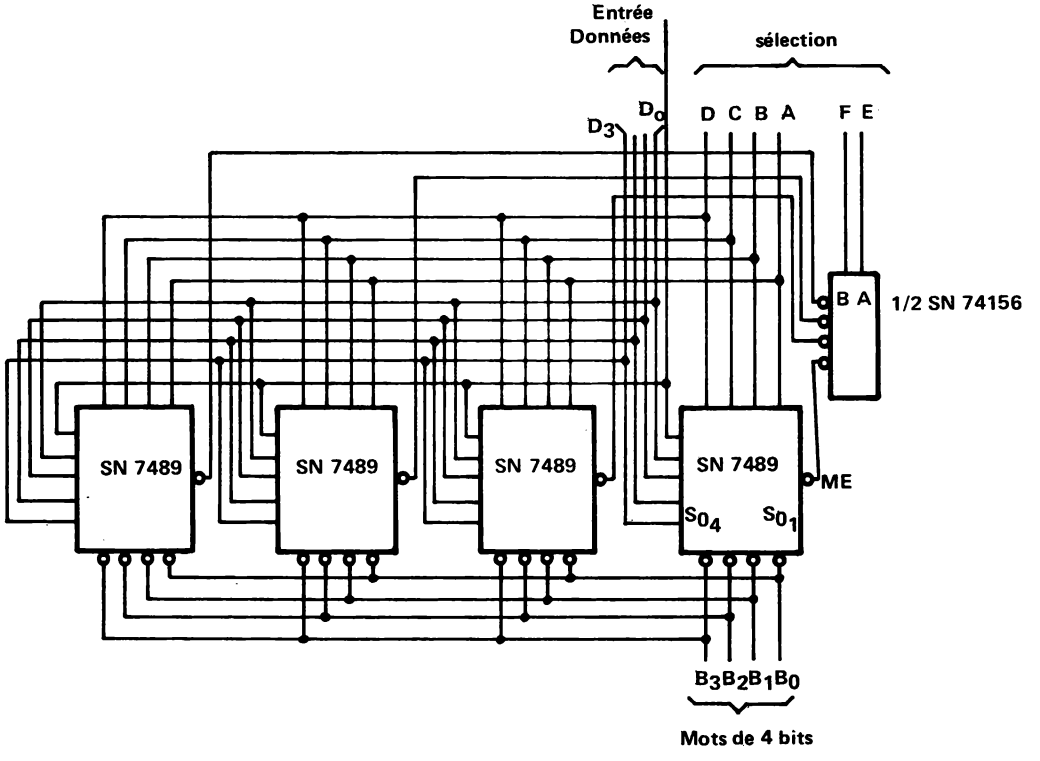


Fig. 7 - Mémoire de 64 mots de 16 bits

Dans ces conditions, la figure 8 donne le schéma équivalent au niveau "0" pour N_2 charges TTL standard (SN 54/74). Il vient :

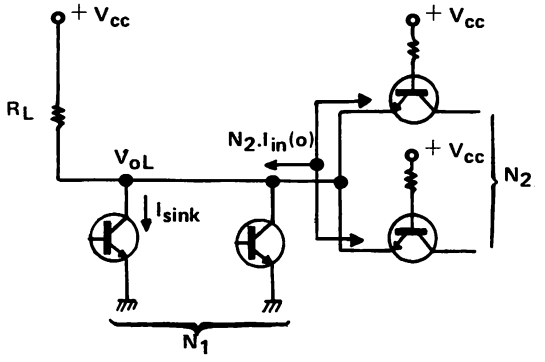


Fig. 8.

$$V_{OL} = V_{CC} - R_L (I_{sink} - N_2 \cdot I_{in}(0)) \leqslant 0{,}4V$$

soit :

$$R_L \geqslant \frac{V_{CC} - 0{,}4}{I_{sink} - N_2 \cdot I_{in}(0)}$$

Par exemple, si $N_2 = 1$, avec $I_{sink} = 12$ mA et $I_{in}(0) = 1{,}6$ mA, il vient :

$$R_L \geqslant 442\Omega.$$

Le schéma équivalent au niveau "1" est celui de la figure 9, avec :

$$V_{OH} = V_{CC} - R_L (N_1 \cdot I_{OH} + N_2 \cdot I_{in}(1)) \geqslant 2{,}4V$$

soit :

$$N_1 \leqslant \frac{V_{CC} - 2{,}4 - R_L \cdot N_2 \cdot I_{in}(1)}{R_L \cdot I_{OH}}$$

et si $N_2 = 1$, $I_{in}(1) = 40\mu A$, $I_{OH} = 20\mu A$:

$$N_1 \leqslant 292.$$

Ceci signifie que, si $N_2 = 1$, il est possible de réaliser avec des boîtiers SN 7489 une mémoire de 292 x 16 = 4672 mots de N bits, N pouvant être quelconque puisque l'entrée "Memory Enable" permet facilement le décodage des bits d'adresse de poids supérieurs à 2^4.

Il est alors possible de dresser le tableau donnant, en fonction du nombre de charges TTL (N_2), le nombre maximum N_1 de "ET câblé" pouvant être réalisé pour $V_{OL} \leqslant 0{,}4$ V.

Charges SN 54/74	R_L (min) (Ω)	N_1	Nombre max. de mots
1	442	292	4672
2	522	245	3920
3	638	197	3152
4	821	150	2400
5	1150	103	1648
6	1916	55	880
7	5750	8	128

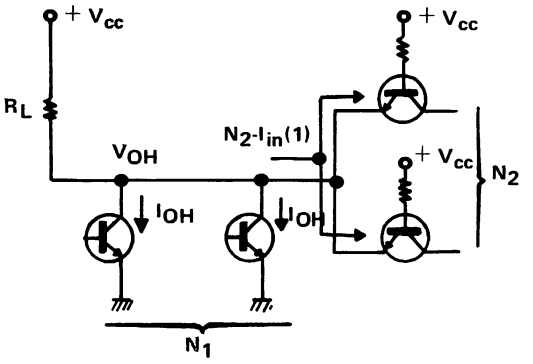


Fig. 9

Le temps d'accès sera affecté par les nombres $N_1 + N_2$; en effet, le temps de montée du signal de sortie est régi par la constante de temps :

$$R_L ((N_1 \cdot C_o) + (N_2 \cdot C_{in}))$$

où

C_o : Capacité de sortie à l'état haut (4pF typique)
C_{in}: capacité d'entrée d'une porte TTL (3pF typique)

IV. APPLICATIONS DE LA MEMOIRE SN 7489

La mémoire SN 7489 trouve son utilisation dans les systèmes nécessitant des mémoires vives à accès rapide, c'est-à-dire principalement dans les mémoires de type "scratchpad".

En outre, elle peut être utilisée lors de l'évaluation d'un système comme mémoire morte rapide permettant la vérification des données qui définiront la mémoire morte finale.

Une application intéressante de ce principe consiste en un générateur de 4 mots de 1 à 16 bits pouvant être utilisé en laboratoire comme générateur de séquence.

Deux autres applications intéressantes de cette mémoire sont décrites dans ce qui suit, soit :

- registre à longueur variable,
- mémoire tampon.

IV. 1 - Registre à longueur variable :

Les mémoires vives permettent de réaliser facilement des registres entrée-série, sortie-série à longueur variable, c'est-à-dire tels que le nombre de bascules les composant soit arbitraire. Pour cela, il suffit d'adresser la mémoire par un compteur de modulo N, où N<M (M nombre de mots de la mémoire). Ainsi, avec une mémoire de M mots de B bits, on réalise B registres de 1 à M bits (figure 10).

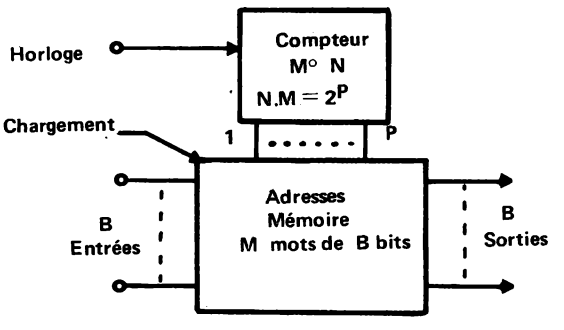


Fig 10

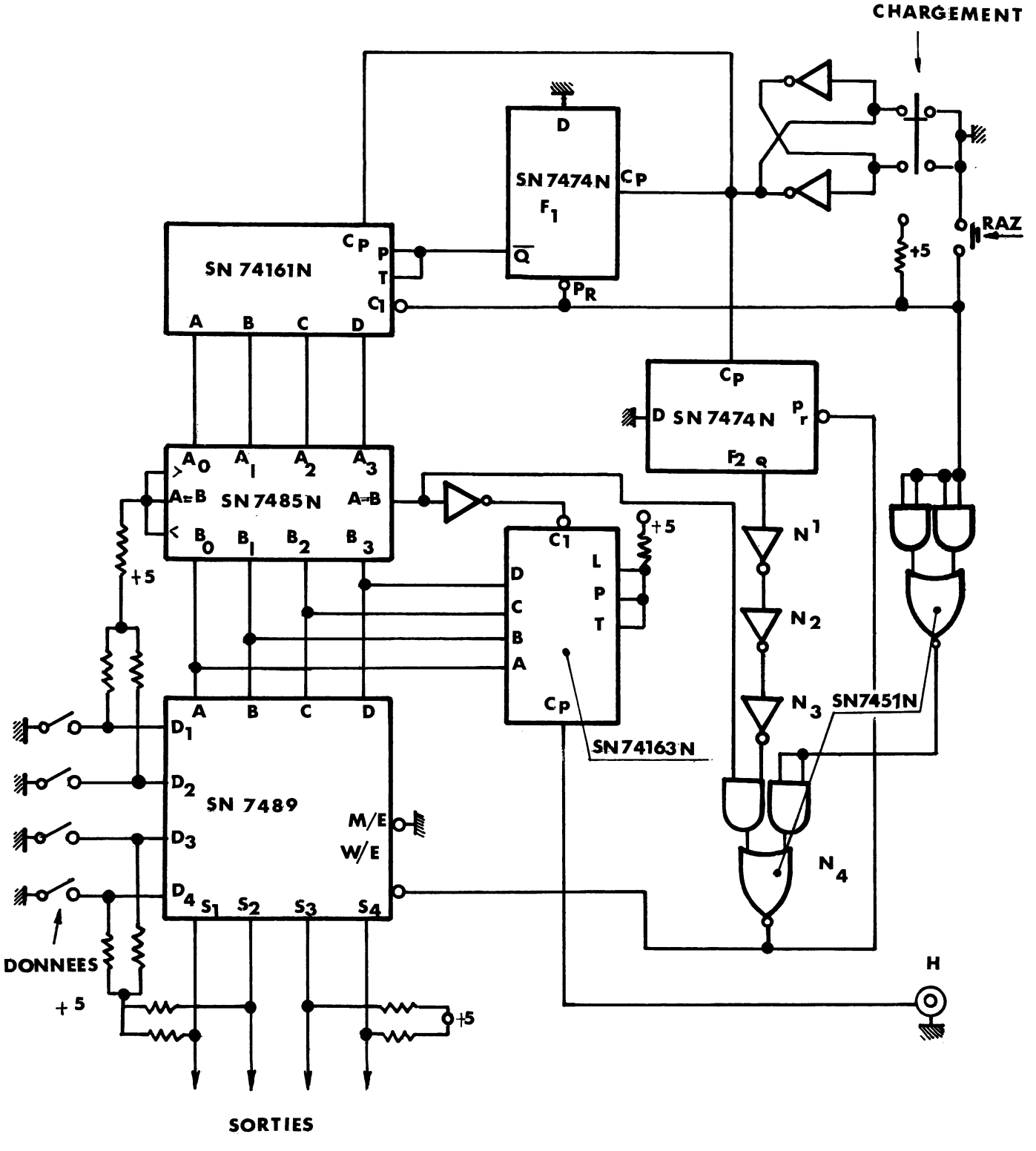
La figure 11 donne le schéma du générateur réalisé avec 7 boîtiers. La mémoire SN 7489 est adressée par les sorties du compteur SN 74163 N incrémenté par l'horloge H; les données sont fournies par bouton poussoir.

Après remise à zéro, le nombre de bits contenus dans chacun des mots correspond au nombre de pressions sur le bouton "chargement" : en effet, le compteur SN 74163 N sera remis à zéro dès que son contenu sera égal à celui du compteur SN 74161 N.

La bascule F_1, en amenant un retard, permet l'écriture des bits d'adresse "0".

La largeur de l'impulsion d'écriture (W.E) est déterminée par la boucle :

Q (F_2), N_1, N_2, N_3, N_4, Pr (F_2).



Le chronogramme de la figure 12 indique le fonctionnement du système pour les deux premiers chargements : dans ce cas, le générateur de mots fournira 4 mots de 2 bits chacun.

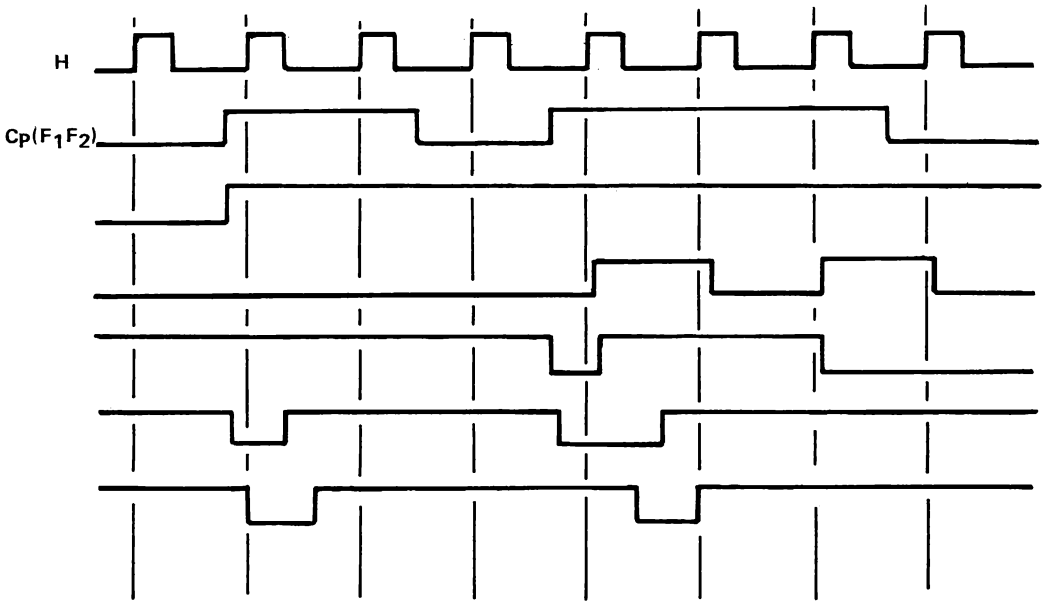


Fig. 12 - Générateur de mots : chronogramme.

Les oscillogrammes de la figure 13 montrent les signaux obtenus avec ce montage pour une horloge ` à 10 MHz.

Il est possible d'étendre les possibilités de ce générateur à 4 x N mots de B bits en utilisant les possibilités d'expansion de la mémoire SN 7489 décrites plus haut.

Le principe utilisé peut être étendu à d'autres applications, par exemple à la génération de mémoires circulantes rapides dans les systèmes de visualisation et, plus généralement, à toutes les applications nécessitant des registres de grande capacité à longueur variable.

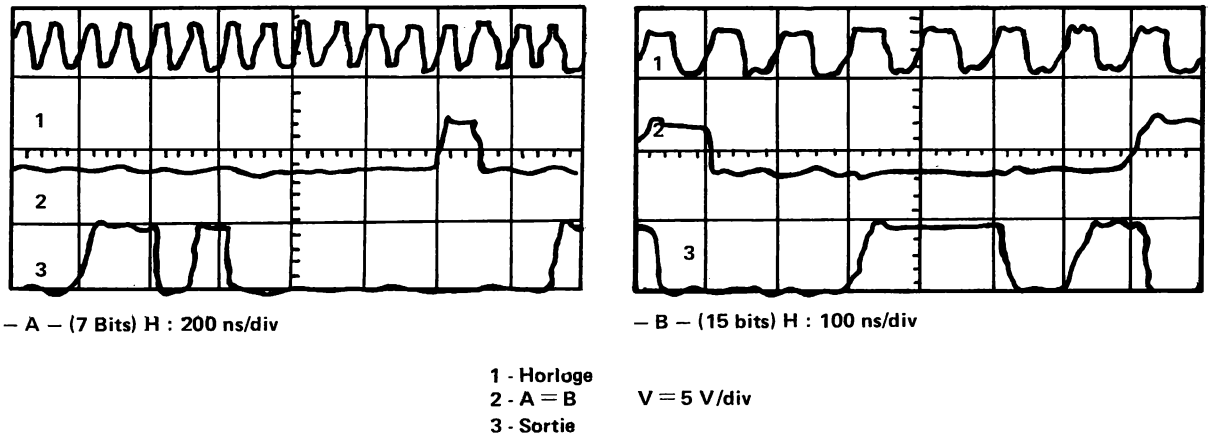


Fig. 13 - Générateur de mots : chronogramme.

IV.2 - Mémoire tampon :

Lorsque des informations doivent transiter entre deux systèmes asynchrones, l'un par rapport à l'autre, il est nécessaire d'utiliser une mémoire tampon de façon à stocker temporairement les données avant leur exploitation.

Un exemple d'un système utilisant une mémoire SN 7489 en élément tampon est indiqué sur la figure 14. Le problème est le suivant : 9 informations BCD présentées en série (entrées D_1, D_2, D_4 et D_8) et validées durant le signal "sélection" par l'horloge H_1 doivent être perpétuellement visualisées sur 9 afficheurs optoélectroniques du type TIL 302.

La mémoire SN 7489 est utilisée en registres à longueur variable (ici 4 registres de 9 bits chacun), son adressage étant effectué, soit par C_1 (compteur de caractères), soit par C_2 (compteur d'affichage). Lorsque "sélection" = 1, l'adresse est déterminée par C_1 (qui est connecté en diviseur par 9); les informations D_1 à D_8 sont alors écrites dans la mémoire et la visualisation est inhibée. Quand "sélection" = 0, l'adressage est effectué par le compteur par 9 (C_2) qui explore la mémoire. Les informations lues sont alors décodées par le décodeur SN 7447 A, tandis que la validation d'un caractère parmi 9 est effectuée par le décodeur SN 74 154.

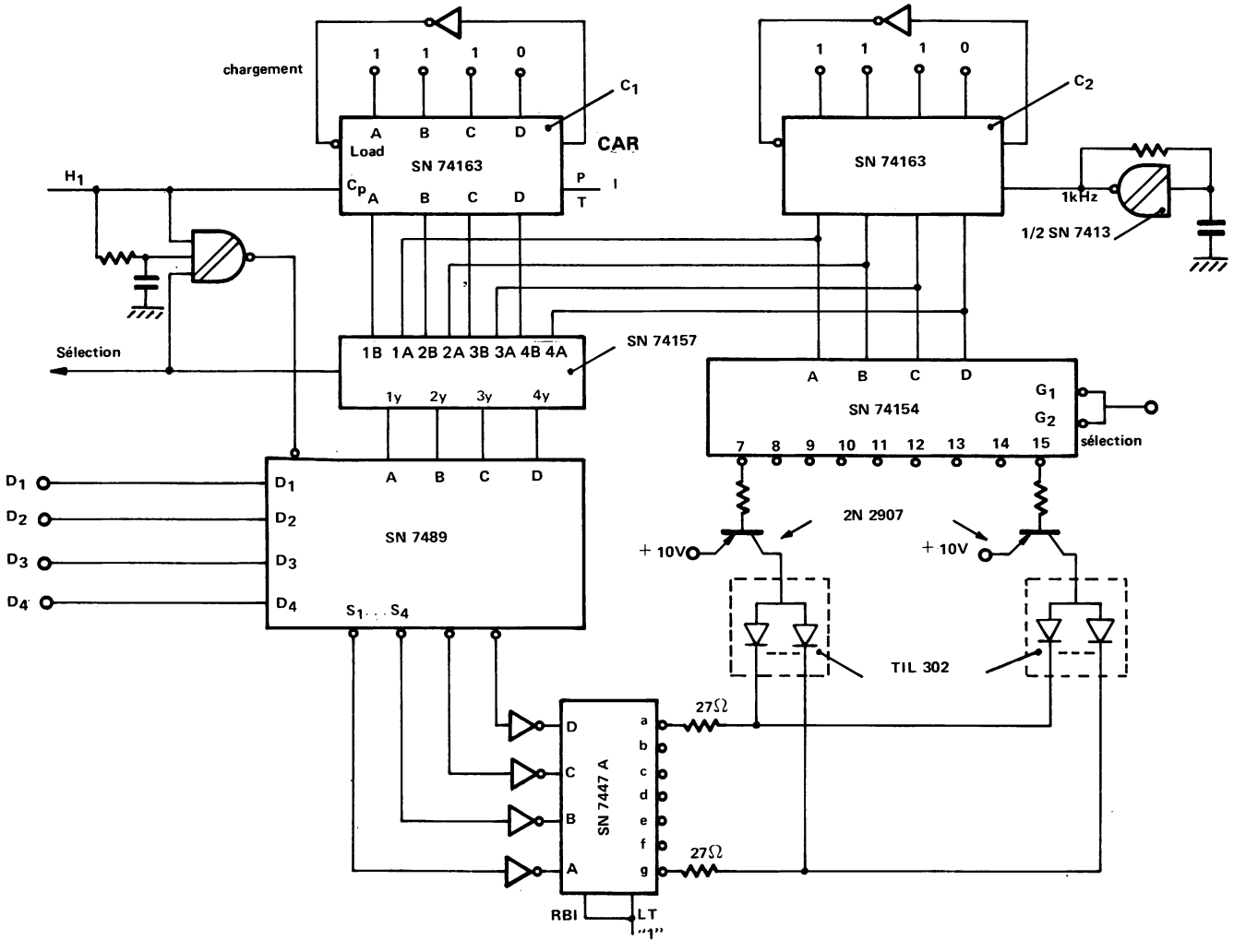


Fig. 14. Affichage tampon - Schéma de principe

La figure 15 donne les principaux signaux rencontrés dans l'affichage tampon.

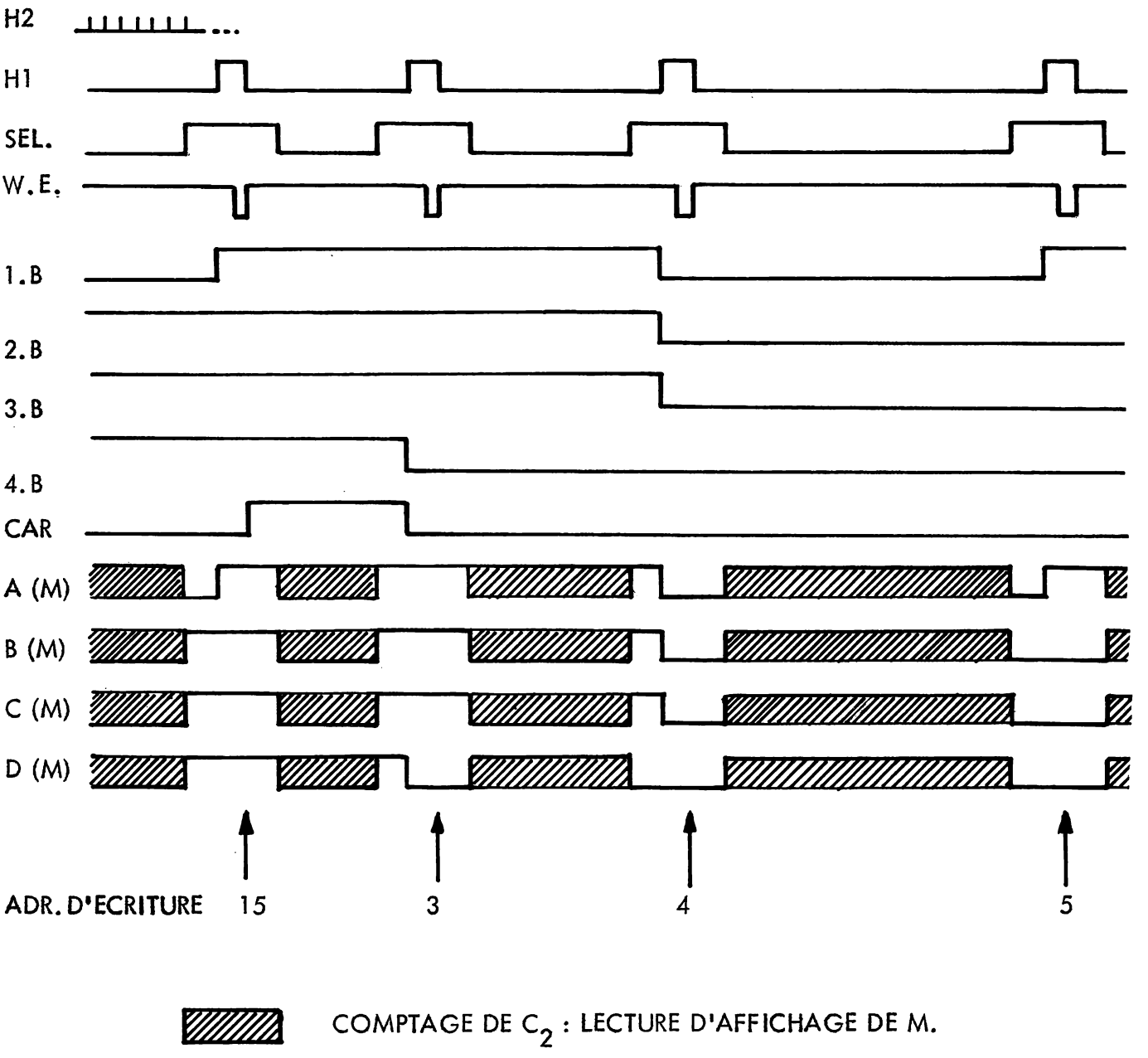


Fig. 15 - Affichage tampon

Etude et applications des monostables SN 74122, 123

(NA 55)

DESCRIPTION ET APPLICATIONS DES MONOSTABLES A REARMEMENT (SN 54/74 122 - SN 54/74 123)

par Jean Cholet

I. DESCRIPTION

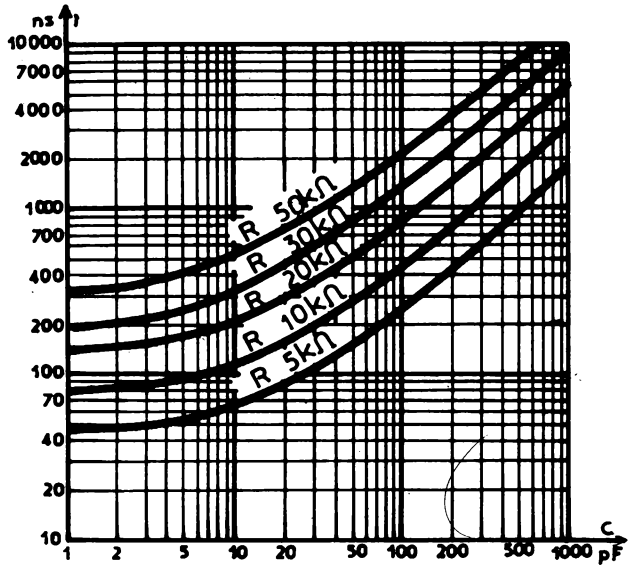
A. MONOSTABLE SN 54/74 122 N

Le monostable SN 54/74 122 N est un circuit qui délivre une impulsion positive et une impulsion négative, dont la durée est définie par un circuit R.C. extérieur, après avoir été déclenché par un front. Il est réarmable et peut être remis à zéro.

- La durée de l'impulsion est définie par la formule :

$$t = 0{,}32\ R.C.\ (1 + \frac{0{,}7}{R})$$

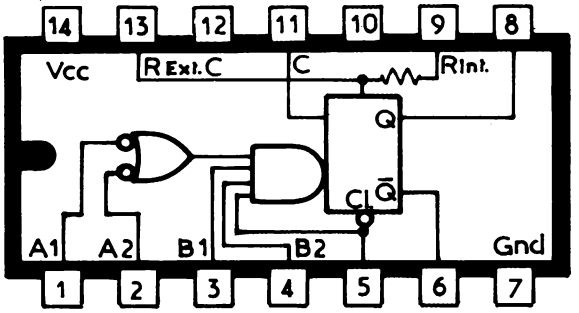
pour des valeurs de C supérieures à 1000 pF. Pour des valeurs inférieures, elle est définie par la figure 1 ci-dessous.



La valeur de la résistance ne doit pas dépasser 25 kΩ pour le SN 54 122 et 50 kΩ pour le SN 74 122. Il n'y a pas de limitation quant à la valeur maximale du condensateur par contre, la valeur minimale de celle-ci, qui est la capacité intrinsèque des connexions peut atteindre 50 pF.

- Le déclenchement a lieu pour un front négatif appliqué à l'une des deux entrées A ou pour un front positif appliqué à l'une des deux entrées B conformément à la table de vérité jointe en figure 2.

Il est à noter que ni les entrées A, ni les entrées B, n'ont une fonction "trigger" comme c'est le cas sur le monostable SN 54/74 121. C'est-à-dire que ces entrées doivent être commandées par des niveaux logiques et ne peuvent pas être attaquées par des rampes.



ENTREES			SORTIES	
$A_1 + A_2$	$B_1 . B_2$	RAZ	Q	$\bar{Q}$
1	X	X	0	1
X	0	X	0	1
X	0	0	0	1
X	0	↑	0	1
0	1	↑	⊓	⊔
0	↓	1	⊓	⊔
↓	1	1	⊓	⊔

- Le réarmement peut être effectué à n'importe quel moment du cycle pourvu que les temps de préconditionnement soient respectés. Chaque impulsion de réarmement entraîne la prolongation du cycle de travail d'une nouvelle durée égale à celle définie ci-dessous (figure 3).

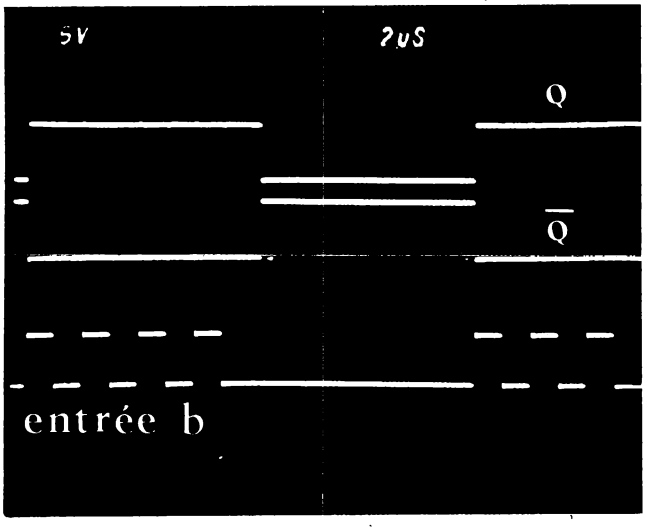


Fig. 3

- La remise à zéro peut avoir lieu à n'importe quel moment du cycle, mais il faut noter que, si on se trouve dans la configuration d'entrée $(A_1 + A_2)\ (B_1 . B_2) = 1$: on obtiendra une impulsion de sortie au moment du relâchement du signal de RAZ. Ceci est dû au fait que l'entrée

"Clear" agit également sur la porte d'entrée de façon à ne pas permettre de déclenchement. Il faut donc, pour avoir un fonctionnement correct de la remise à zéro, travailler avec le produit $B_1 B_2$ égal à zéro au moment du retour du signal "Clear" (figure 4).

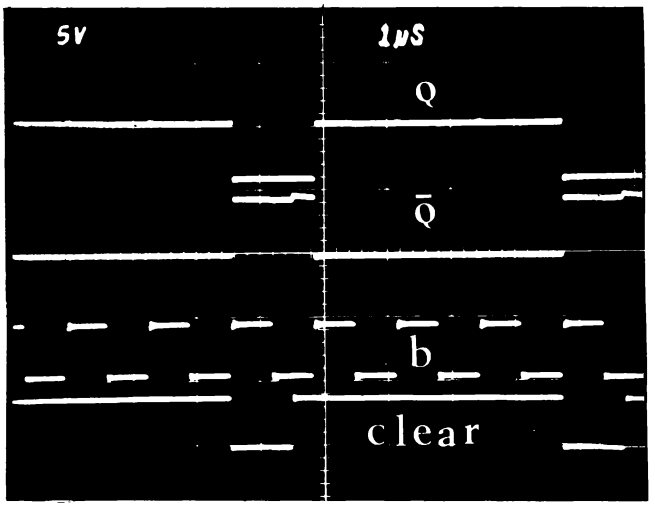


Fig. 4

Utilisation avec des condensateurs polarisés

Pour des périodes très longues, l'utilisateur peut être amené à utiliser des condensateurs électro-chimiques. Il faut donc s'assurer du sens de la tension continue qui peut leur être appliquée. Sur la figure 5 on voit, d'une part la sortie Q et d'autre part la tension différentielle présente aux bornes du condensateur. Cette tension étant mesurée avec des sondes 10 X, il convient de multiplier l'indication de la sensibilité par dix. On voit que cette tension varie de + 500 à -500 mV ce qui exclut l'utilisation d'un condensateur polarisé. Cet inconvénient peut être évité par l'utilisation d'un circuit de temporisation légèrement modifié, représenté sur la figure 6. N'importe quelle diode de commutation peut être employée, mais il n'est plus possible d'utiliser la résistance intérieure et la résistance extérieure doit alors être limitée à 30 kΩ. Dans ce cas, la durée de l'impulsion est modifiée et devient $t = 0{,}28RC\ (1 + 0{,}7/R)$, mais la tension différentielle ne change plus de signe, elle est comprise entre + 300 et 950mV (Fig. 7).

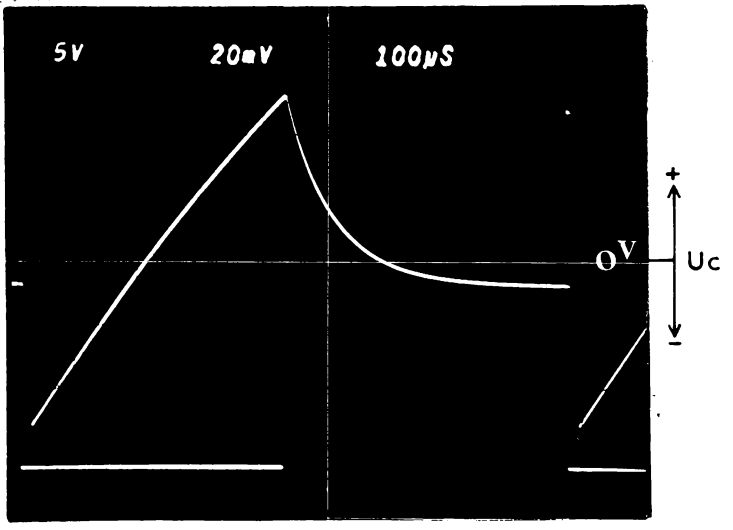


Fig. 5

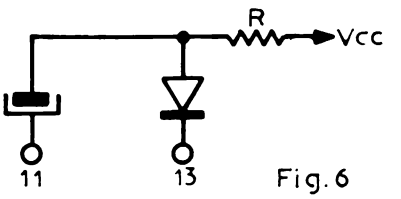


Fig. 6

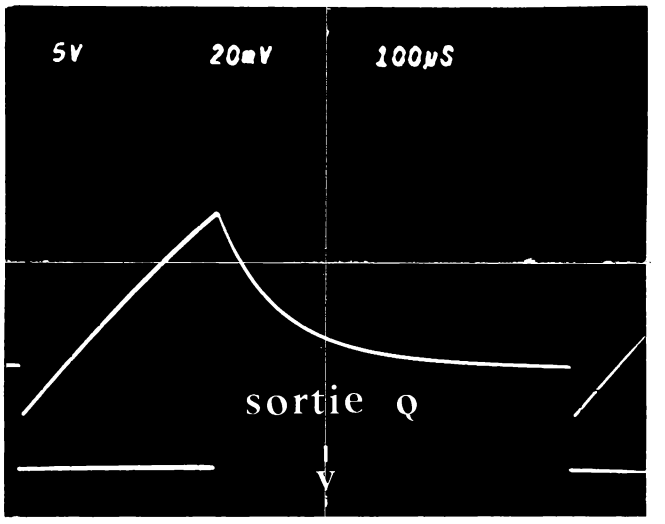


Fig. 7

Ce circuit de temporisation n'a aucune influence sur le comportement de la remise à zéro. Sur la figure 8, relevée sur un montage sans diode, la tension aux bornes du condensateur reste négative mais il est bien évident que si la RAZ arrivait plus tard, cette tension pourrait devenir positive.

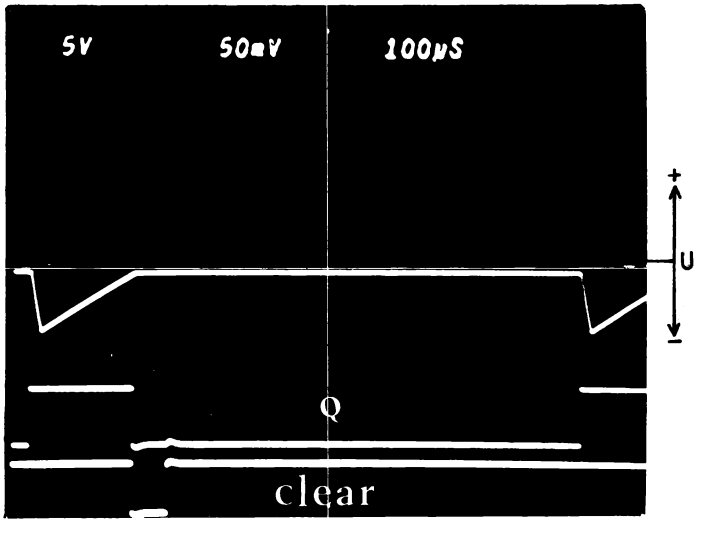


Fig. 8

Par contre, sur la figure 9 qui est relevée sur un montage avec diode, cette tension reste toujours positive. dans les deux cas, le déclenchement et la remise à zéro s'effectuent de la même façon.

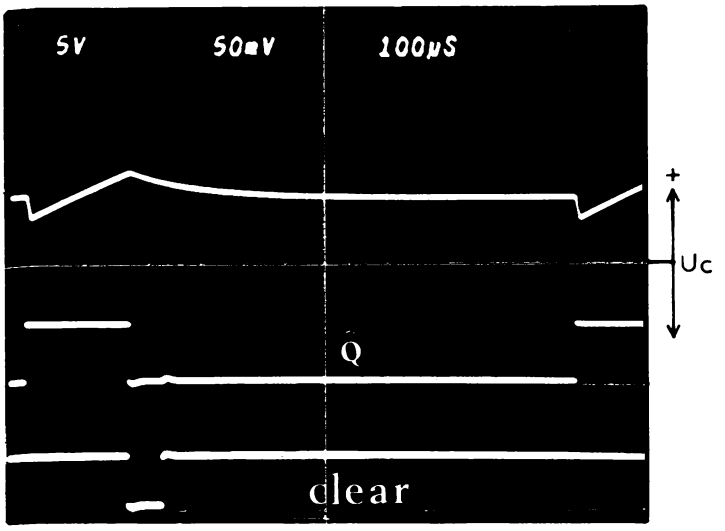


Fig.9

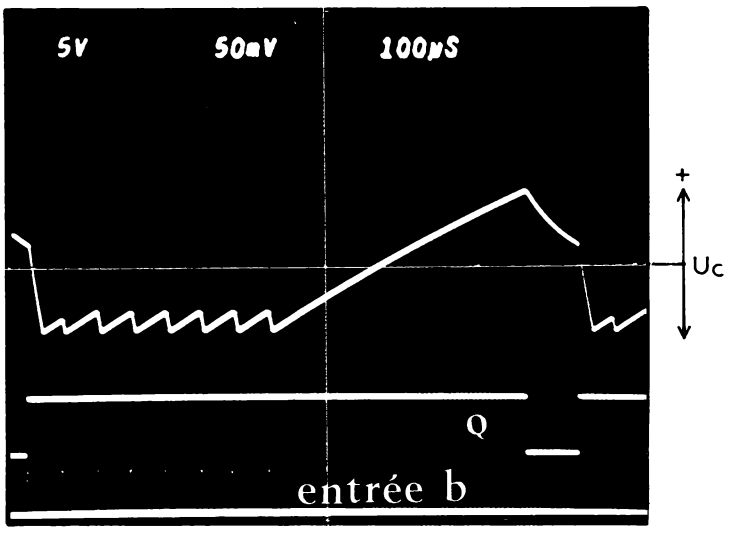


Fig.10

Il n'en est pas de même pour ce qui est du réarmement. Dans le montage sans diode (fig. 10), chaque impulsion de réarmement provoque le retour de la tension du condensateur à sa valeur de départ, soit -500 mV et la véritable rampe n'apparaît qu'après la dernière impulsion, mais si on utilise le montage avec diode, le réarmement n'a lieu que quand la tension du condensateur est supérieure à quelques 750 mV (fig. 11). La longueur du signal de sortie peut alors être complètement faussée. Ce montage ne convient donc pas pour être utilisé avec le réarmement.

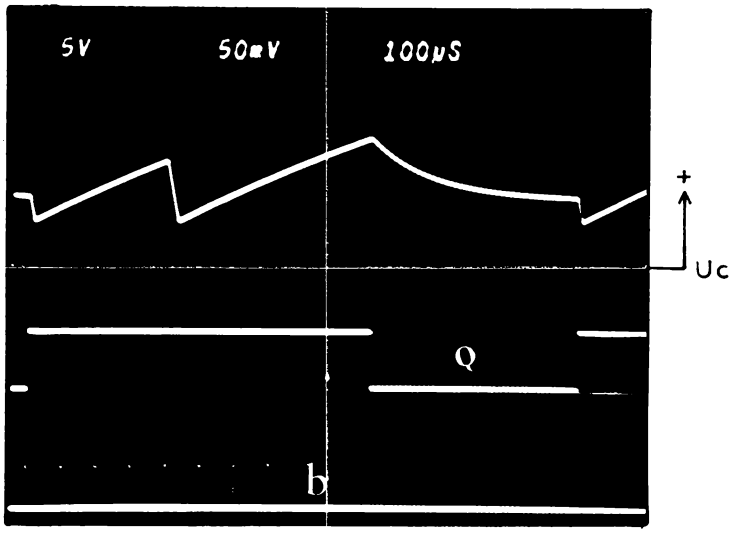
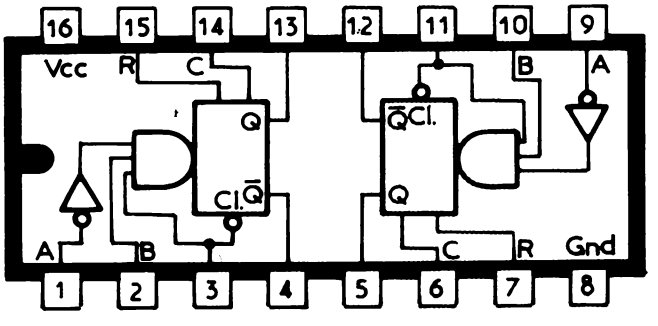


Fig.11

B. MONOSTABLE SN 54/74 123

Le monostable SN 54/74 123 N comprend, en fait, deux monostables identiques au SN 54/74 122 dans un seul boîtier à 16 sorties. Chaque élément ne comporte qu'une entrée A et une entrée B et n'a pas de résistance interne de temporisation. Dans le cas de l'utilisation du circuit de temporisation avec diode la valeur de la résistance extérieure doit être limitée à 15 kΩ. Ceci mis à part le fonctionnement des deux circuits est exactement semblable.



II. QUELQUES APPLICATIONS

- Codeur de clavier décimal

Ce circuit délivre un mot parallèle dont la valeur B.C.D. est égale au numéro de la touche du clavier qui vient d'être enfoncée. Il est réalisé suivant le schéma de la figure 12 ci-contre.

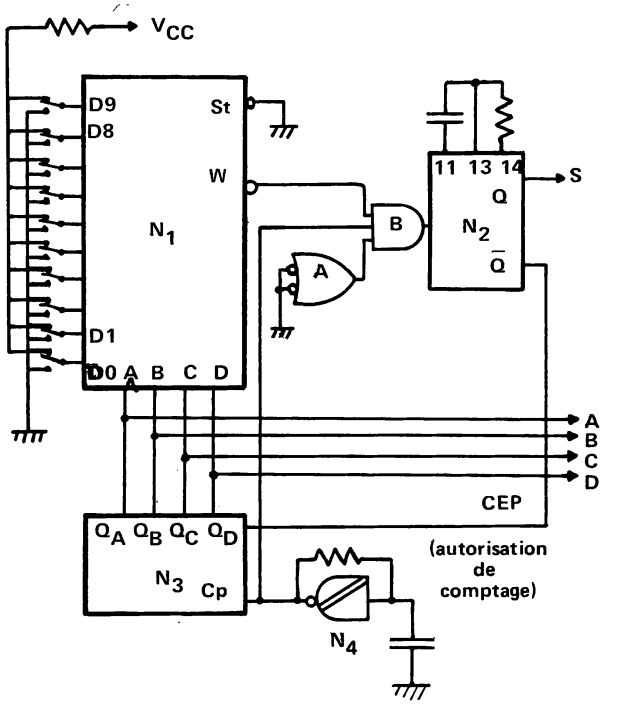


Fig. 12 (Note 1)

En l'absence de mise à la masse de l'une des touches du clavier, la sortie W du multiplexeur N_1 (SN 74 150) reste au niveau "O".

Lorsque l'une des touches est enfoncée la sortie W passe au niveau "1" quand la valeur des entrées ABCD correspond à la touche qui est enfoncée, mais, étant donné que les interrupteurs ont des contacts mécaniques, il peut se produire des rebondissements et la sortie W les reproduit fidèlement. On utilise donc un monostable dont la première fonction est de "nettoyer" les contacts : à chaque rebondissement le monostable est réarmé. Pendant la durée de l'impulsion de sortie, le compteur est bloqué par l'action de la sortie $\bar{Q}$ du monostable sur l'entrée "Enable P" du compteur. Un signal de prise en compte (S) est également délivré. et ce, tout le temps que la même touche reste enfoncée. Ceci est obtenu simplement en envoyant le signal d'horloge sur l'autre entrée B du monostable. Ce signal provoque le réarmement du monostable à chaque impulsion d'horloge. La durée de l'impulsion issue du monostable doit être environ $1{,}5\theta$, si θ est la période de l'horloge utilisée.

N_1 : SN 74 150
N_2 : SN 74 122
N_3 : SN 74 160
N_4 :

Note 1 : Les entrées non spécifiées doivent être réunies au niveau logique "1".

L'utilisation d'un compteur binaire SN 74 161 permet la réalisation d'un codeur de clavier à 16 touches.

- Transmission de données par trains d'impulsions

La donnée à transmettre est d'abord transformée en train d'impulsions, trains dans lesquels le nombre d'impulsions est égal à la valeur du mot binaire à transmettre; chaque train d'impulsion est séparé du suivant par une période de repos (il faut noter que la valeur zéro ne peut pas être transmise). Cette transformation peut être effectuée par le montage de la figure 13.

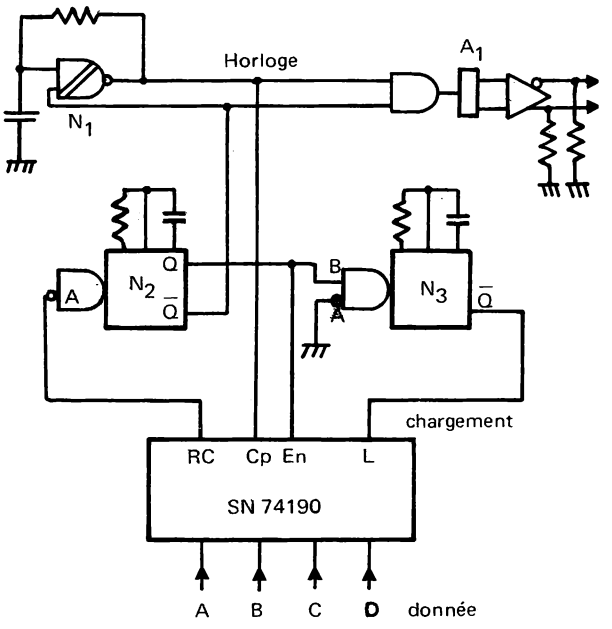


Fig. 13 (Note 2)

L'horloge est réalisée à l'aide d'un demi SN 7413. L'une des entrées est utilisée comme oscillateur et une autre pour le verrouillage. Le mot à transmettre est présenté sous la forme parallèle aux entrées d'un SN 74190 fonctionnant en décompteur. Les séquences de travail sont réalisées par un monostable SN 74123.

Au repos, l'entrée "Enable" du compteur est à l'état "0" et l'entrée "Load" à l'état "1". Les impulsions d'horloge provoquent donc le décomptage et ce, jusqu'à ce que le compteur soit arrivé à zéro.

A ce moment la sortie "Ripple Clock" fournit un "0". Ce signal va déclencher le monostable N_2 qui délivre l'impulsion de séparation des trains : pendant la durée de cette impulsion l'horloge est bloquée par $\bar{Q}$ et le compteur par Q. Cette impulsion, à son tour, déclenche le monostable N_3 qui fournit l'ordre de chargement au compteur. La largeur de cette impulsion n'est pas critique, il suffit qu'elle soit plus courte que la précédente. Dès que le compteur est chargé la sortie "Ripple Clock" remonte à 1 mais le compteur ne peut repartir qu'à la fin de l'impulsion de séparation. La transmission est effectuée sur une ligne bifilaire par un demi SN 75 109. Les impulsions d'horloge sont encadrées par le signal de sortie du premier monostable pour qu'elles se présentent sous la forme voulue.

A la réception, il s'agit de reconstituer, sous la forme parallèle le mot qui était présent à l'entrée du SN 74 190. Ceci est réalisé par le montage de la figure 14.

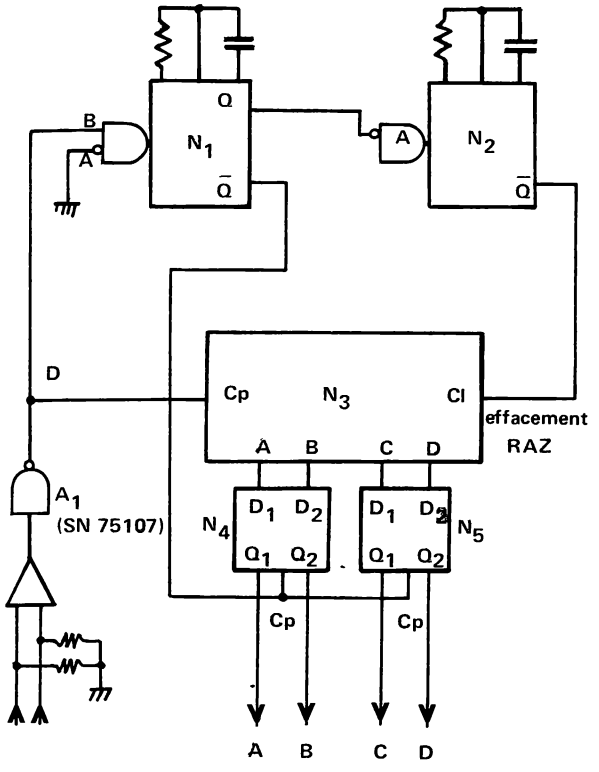
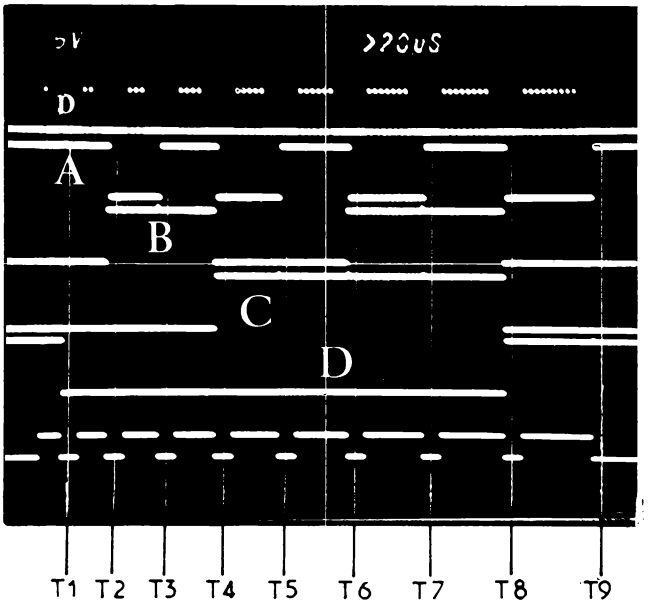


Fig. 14 (Note 3)

Les signaux sont reçus par le SN 75 107 et vont attaquer d'une part le monostable N_1 et d'autre part le compteur synchrone SN 74 160. La période de travail du monostable N_1 est plus longue que la durée qui sépare deux impulsions mais plus courte que le temps de séparation des impulsions de façon à permettre le réarmement du monostable. Celui-ci fournit donc un créneau légèrement plus long que la durée du train d'impulsions; pendant ce temps, le compteur N_3 a compté le nombre d'impulsions. Ce nombre est présent aux entrées des bistables D N_4 et N_5 (SN 7474). A la fin du créneau délivré par N_1, le mot présent à la sortie de N_3 est transféré dans N_4 et N_5 puis N_2 est déclenché et fournit une impulsion brève de remise à zéro pour N_3. Le montage est alors prêt pour détecter un nouveau train d'impulsions. Le fonctionnement des récepteurs est illustré sur la photo de la figure 15



On voit qu'à l'instant T_1 qui suit la transmission d'une impulsion les sorties de la mémoire sont dans l'état : A = 1; B = 0; C = 0; D = 0 puis à T_2 : A = 0; B=1; C = 0; D = 0; etc.

Note 2 : Les entrées non représentées doivent être raccordées au niveau "1".
A_1 : : 1/2 SN 75109
$N_2 + N_3$: SN 74123

Note 3 : Les entrées non représentées doivent être raccordées au niveau "1"
$N_1 + N_2$: SN 74123
N_3 : SN 74160
$N_4 + N_5$: SN 7475

Compteurs synchrones SN 74160, 1, 2, 3
(NA 60)

NA 60 COMPTEURS SYNCHRONES SN 54/74160, 1, 2, 3

par G. Chauvel

I. DESCRIPTION

Les compteurs SN 54/74160, SN 54/74162, SN 54/74161, SN 54/74163, dont le brochage est indiqué figure 1, sont des compteurs synchrones 4 bits contenant une logique interne permettant de les connecter en cascade sans éléments extérieurs. Le synchronisme des transitions qui apparaissent sur le front positif de l'horloge permet de s'affranchir des parasites de décodage souvent associés aux compteurs non synchrones.

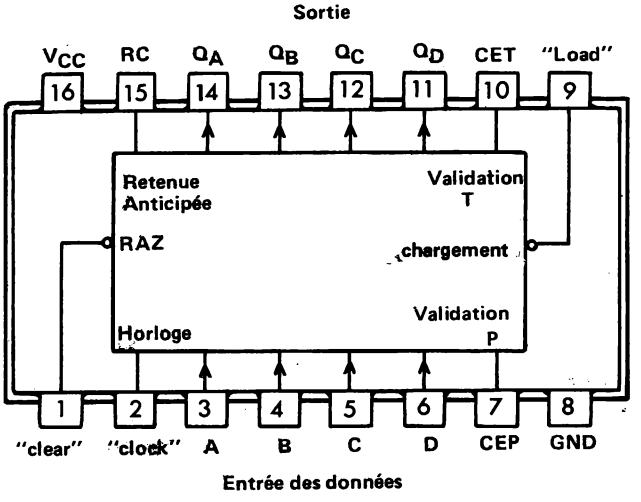


Fig. 1 : Brochage des compteurs 74160/161/162

Ces compteurs sont complètement programmables. Il suffit pour cela d'inhiber le comptage en positionnant l'entrée "load" à l'état bas ("0") pour que les informations présentes sur les entrées de forçage soient présentes sur les sorties à la prochaine horloge.

La remise à zéro RAZ de ces compteurs peut être synchrone ou asynchrone, comme indiqué sur le tableau suivant .

	COMPTAGE	CHARGEME	RAZ
SN 54/74160	synchrone BCD	synchrone	asynchrone
SN 54/74161	synchrone binaire	synchrone	asynchrone
SN 54/74162	synchrone BCD	synchrone	synchrone
SN 54/74163	synchrone binaire	synchrone	synchrone

Dans le cas de la remise à zéro asynchrone, le fait de positionner l'entrée "clear" à "0" imposera en sortie l'état 0000 indépendamment de l'état de l'impulsion d'horloge (figure 2).

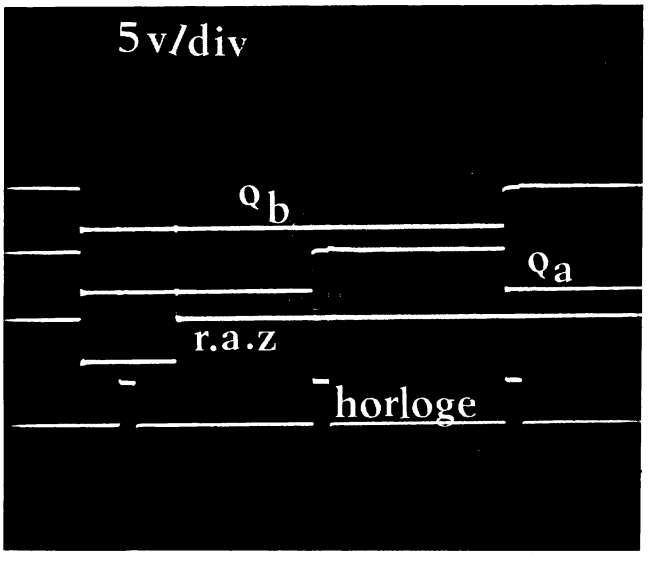


Fig. 2. SN 54/74160 : Remise à zéro asynchrone .

La remise à zéro synchrone, particulièrement utile pour la réalisation de compteurs de 0 à N, est obtenue au coup d'horloge suivant l'instant où "clear" est porté à l'état "0" (figure 3).

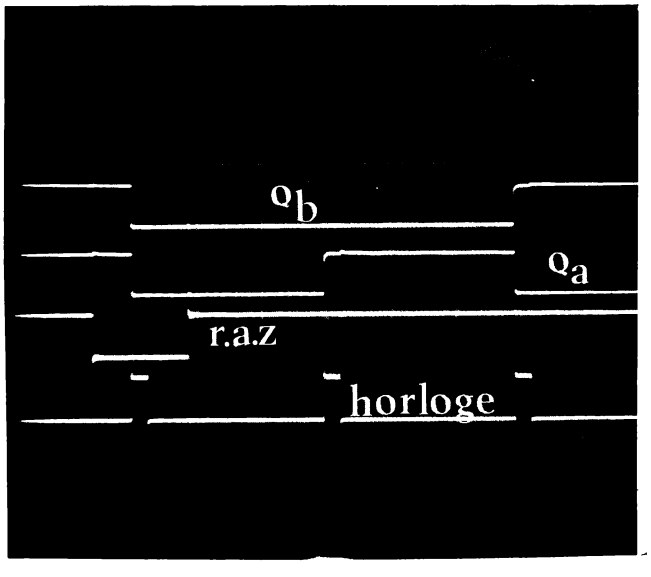
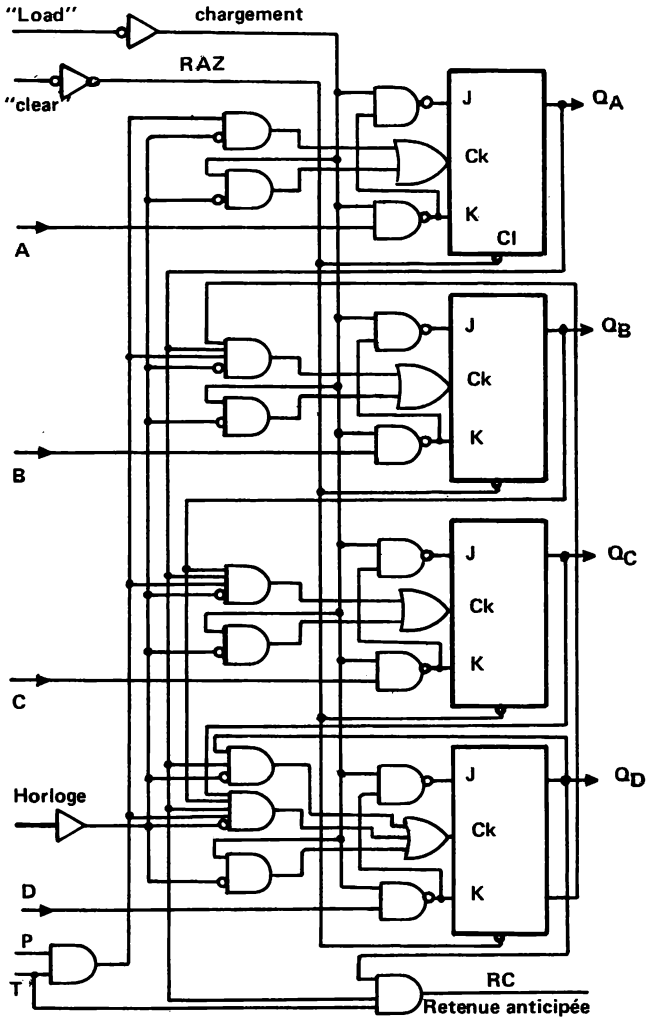


Fig. 3. SN 54/74162 : Remise à zéro synchrone

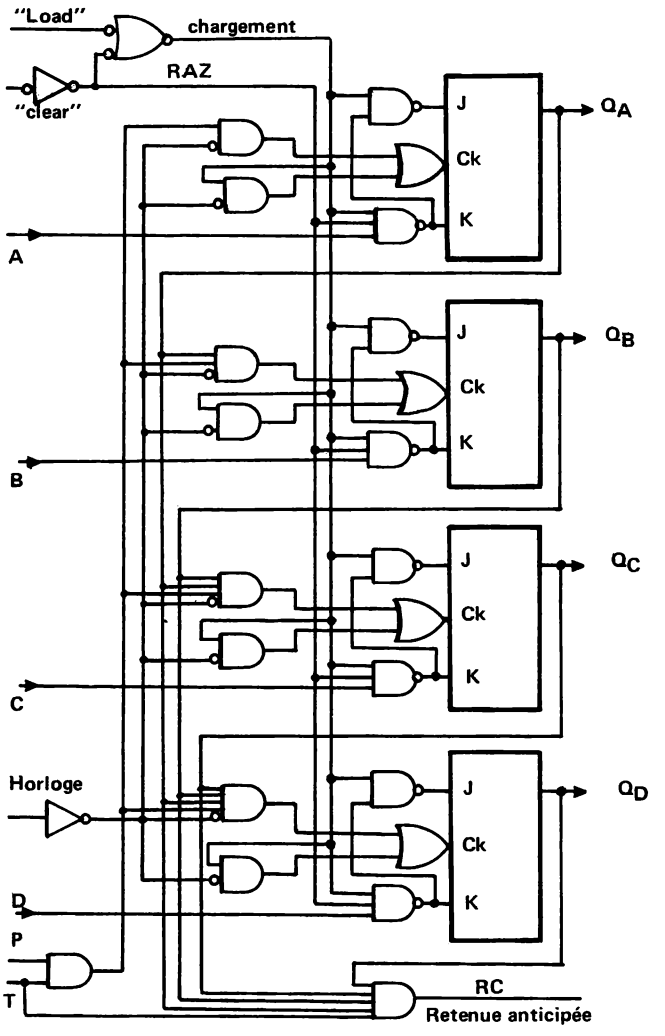
Les figures 4 et 5 donnent les schémas des compteurs SN 54/74160 et SN 54/74163, les schémas des compteurs SN 54/74161 et SN 54/74162 en étant facilement déduits.

Fig. 4 : Decade synchrone SN 54/74160



Le schéma du SN 54/74162/ Compteur 4 bits synchrone est similaire; seule la RAZ est asynchrone comme indiqué sur le schéma du SN 54/74163.

Fig. 5 : Compteur 4 Bits synchrone SN 54/74163



Le schéma du SN 54/74161/ compteur 4 Bits synchrone est similaire, seule la RAZ est asynchrone comme indiqué sur le schéma du SN 54/74160.

Ces schémas appellent quelques remarques :

• Le circuit de retenue anticipée permettant la mise en cascade de plusieurs compteurs est constitué des entrées COUNT ENABLE P ou T (CEP ou CET) et de la sortie RIPPLE CARRY (RC), avec :

$RC = CET . Q_A . Q_B . Q_C . Q_D$

pour les compteurs binaires

et $RC = CET . Q_A . Q_D$

pour les compteurs BCD.

La durée de RC sera approximativement égale à la durée d'une impulsion positive issue de Q_A (figure 6).

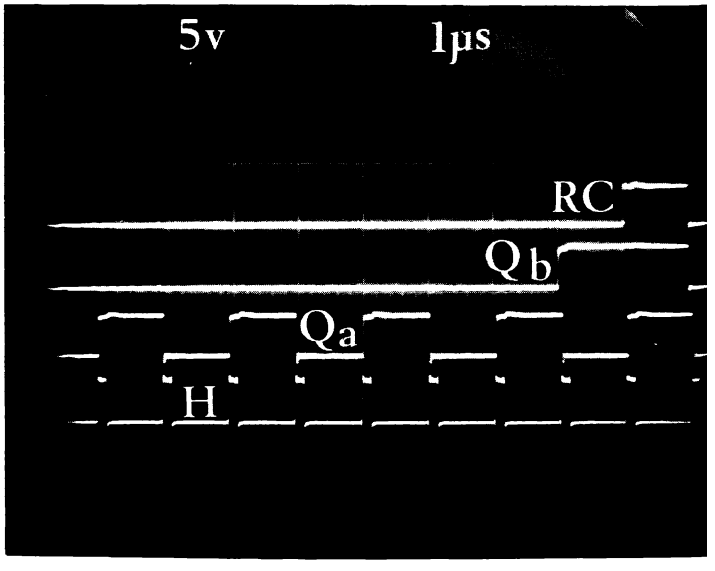


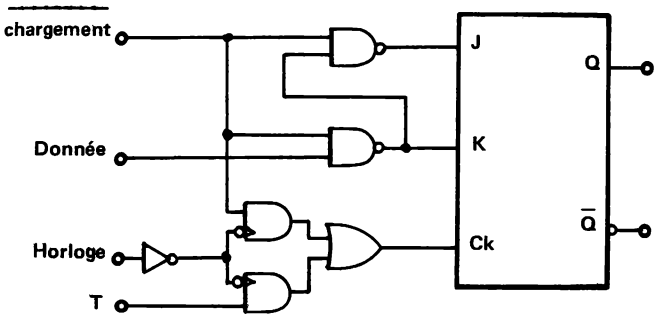
Fig. 6. SN 54/74160 - Sortie ripple carry.

Dans ces conditions, le tableau suivant donne les principaux modes d'opération des compteurs en fonction des états de CEP, CET et Load.

LOAD	CEP . CET	MODE
1	1	Comptage
1	0	Inhibition
0	ϕ	Chargement synchrone

• Les bascules utilisées, de technologie maître esclave, sont des bascules JKT dont la figure 7 donne à la fois le schéma logique et la table de vérité.

Sur cette figure, le signe ⇔ signifie que les transitions sur Q ($\overline{Q}$) apparaissent sur le front de montée de l'horloge.



chargement	Donnée	J	K
0	0	0	1
0	1	1	0
1	ϕ	1	1

J_n	K_n	T_n	Q_{n+1}
1	0	ϕ	1
0	1	ϕ	0
1	1	0	Q_n
1	1	1	$\overline{Q_n}$

Fig. 7. Schéma et table de vérité de la bascule JKT.

• D'éventuelles impulsions négatives sur les entrées sont protégées par des diodes d'écrêtage. La sortance au niveau bas est 10 charges standard TTL et 20 au niveau haut, ce qui permet de faciliter les connexions des entrées non utilisées aux entrées utilisées. La dissipation moyenne des compteurs est de l'ordre de 325 mW.

II. MISE EN CASCADE

La mise en cascade de plusieurs compteurs est facilitée par la logique interne qui génère le signal RC (voir figure 8) et les entrées CEP et CET. La figure 9 donne le mode de connexion permettant de réaliser cette fonction.

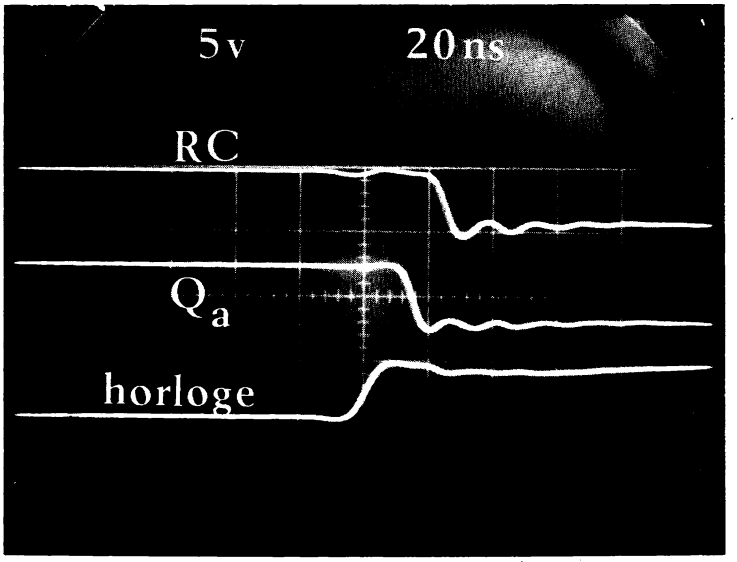


Fig. 8. Compteurs synchrones - ripple carry -

La validation de comptage est déterminée par le produit logique CEP. CET; ainsi; pour le deuxième compteur, CEP . CET vaut "1" durant l'état 15 (ou 9) de C_1 permettant ainsi d'incrémenter de 1 le compteur 2. Pour le compteur de rang n ($n < 10$ à cause de la sortance de RIPPLE CARRY), CEP CET aura toujours la même durée, déterminée par (RC) 2 - figure 10 -.

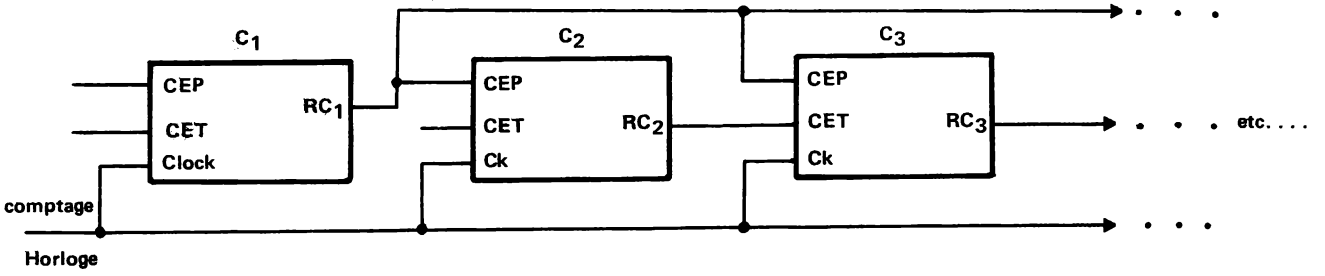


Fig. 9 : Mise en cascade

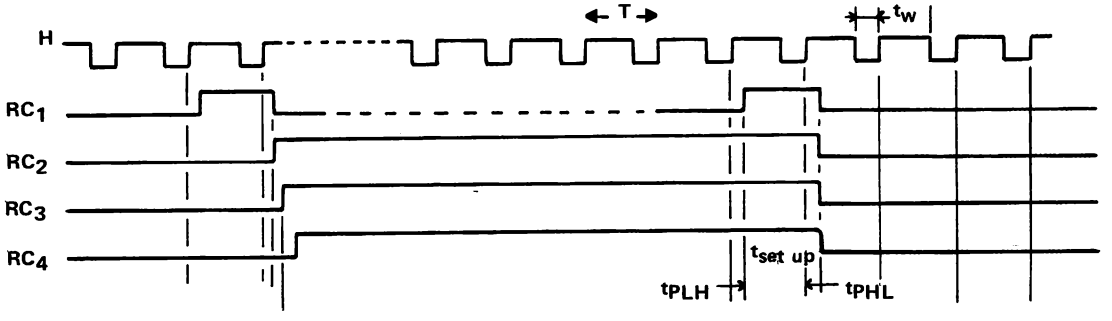


Fig. 10 : Propagation de la retenue anticipée

La mise en cascade de n compteurs ne limite donc pas la fréquence de comptage à partir du deuxième compteur.

La période minimale de répétition est alors telle que :

$$T > tpLh + t\ set\text{-}up$$

ou

$$T > tpHL + (tw)\ min$$

ou tpLH, tpHL, t set-up et (tw) sont indiqués sur la figure 10. La fréquence typique d'utilisation dans ce cas sera de l'ordre de 20 Mhz.

III. APPLICATIONS

La possibilité de charger les compteurs de façon synchrone et, pour certains d'entre eux, l'existence d'une remise à zéro synchrone permettent de réaliser facilement la plupart des applications de comptage, à savoir :

- Diviseur par N
- Compteur 0 à N
- Compteur N_1 à N_2.

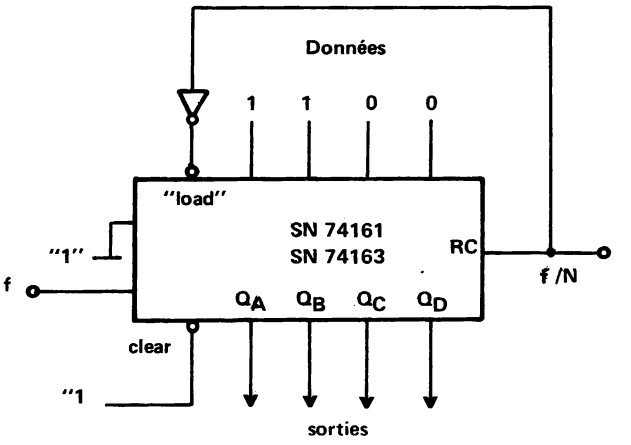
Le tableau suivant donne les équivalences entre compteurs binaires et BCD.

BINAIRE	BCD
SN 54/74161 SN 54/74163	SN 54/74160 SN 54/74162

3.1. - Diviseur par N : les compteurs SN 54/74163 et SN 54/74161 sont particulièrement bien adaptés à la division d'une fréquence par un nombre N compris entre 1 et 16. Ceci est obtenu simplement en chargeant le compteur au coup d'horloge suivant la présence de CARRY par 16 - N, c'est-à-dire par le complément à 2 de N. La figure 11 donne un exemple de diviseur par 13. Le complément à 2 de 13 (1101) est 0011, le compteur comptera donc jusqu'à 15 (1111) puis passera à 0011.

Ce type de comptage peut être étendu à plusieurs boîtiers. Soit, par exemple, à diviser par 731, dont la valeur binaire est, les faibles poids étant à droite :

1 0 1 1 0 1 1 0 1 1



	D	C	B	A	
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	chargement
4	0	1	0	0	16 - 13 = B
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	comptage
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	commande
15	1	1	1	1	chargement

Fig. 11 : Diviseur par N

Puisqu'il est nécessaire d'utiliser 3 circuits SN 74163 pour réaliser ce diviseur, le complément à 1 de 731 est :

1 1 0 1 0 0 1 0 0 1 0 0

et le complément à 2, obtenu en ajoutant 1 au complément à 1 est :

1 1 0 1 0 0 1 0 0 1 0 1

Le schéma du compteur est donné sur la figure 12 : l'état 1111 de tous les compteurs est détecté par la porte NAND qui charge le complément à 2 de 731 au coup d'horloge suivant.

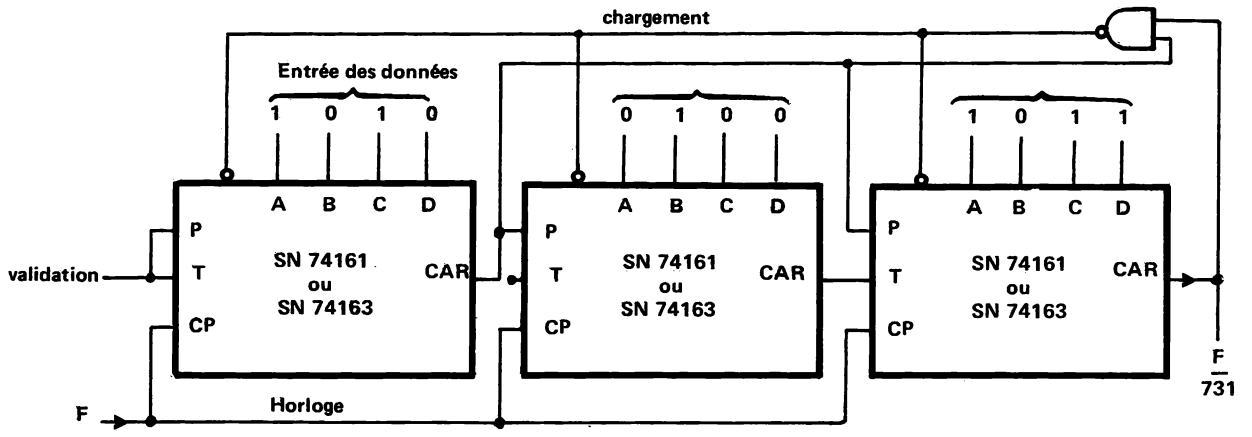


Fig. 12 : Diviseur par 731

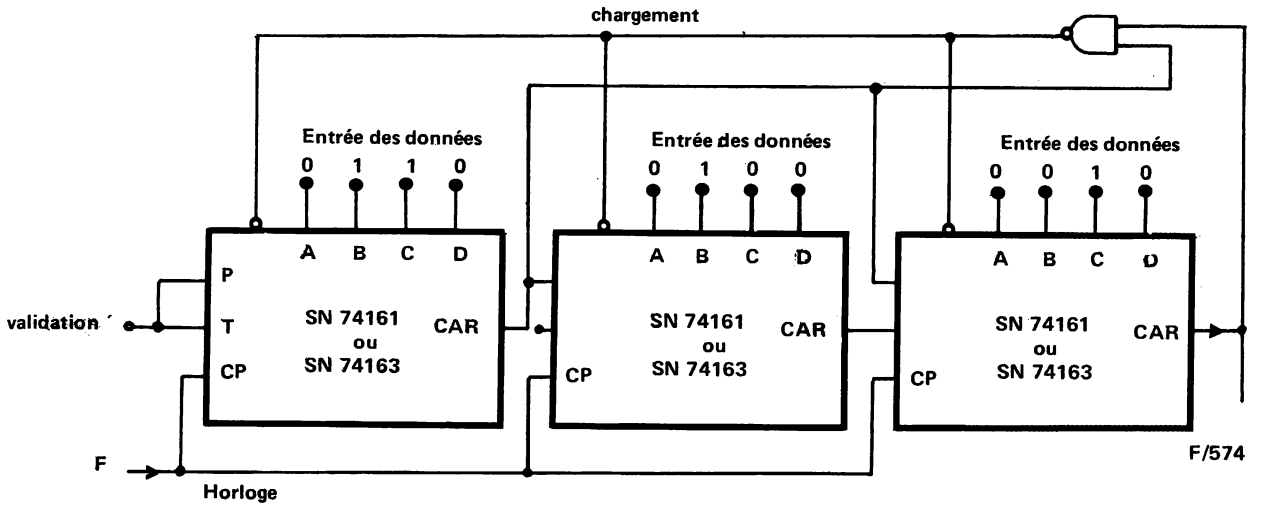


Fig. 13 : Diviseur par 574

De la même façon, en utilisant des décades SN 74160 ou SN 74162, on peut réaliser un diviseur programmable en chargeant les compteurs par le complément à 10 du nombre à diviser que l'on obtient en complémentant à 9 tous les digits et en ajoutant 1 au résultat obtenu. La figure 13 donne un exemple de diviseur par 574.

3.2. - Compteur 0 à N : les compteurs à remise à zéro synchrone (SN 54/74162 et SN 54/74163) sont particulièrement utiles pour ces applications. La figure 14 donne un exemple de compteur de 0 à 12 : l'état 12 (1100) est décodé et le compteur est remis à zéro au coup d'horloge suivant.

Il est possible d'étendre ce principe à plusieurs compteurs connectés en cascade, comme indiqué sur la figure 15 qui montre un compteur de 0 à N, avec $1 \leqslant N \leqslant 999$, la programmation étant effectuée par "straps" sur les "ET" à collecteur ouvert (SN 7417). Sur la figure 15, les connexions effectuées permettent de compter de 0 à 631.

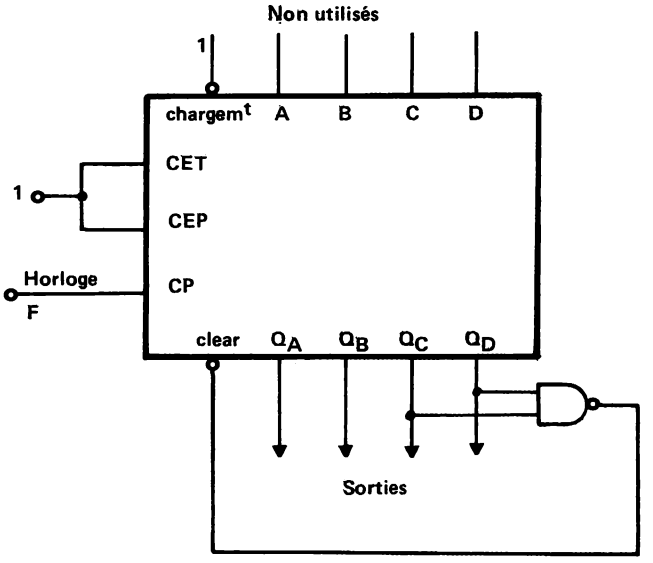


Fig. 14 : Compteur de 0 à 12

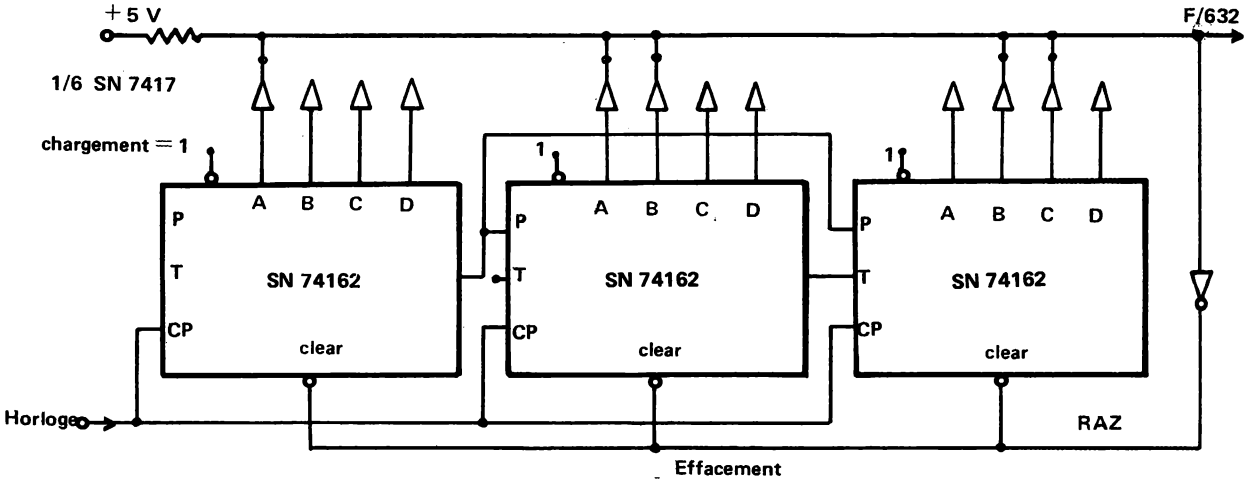
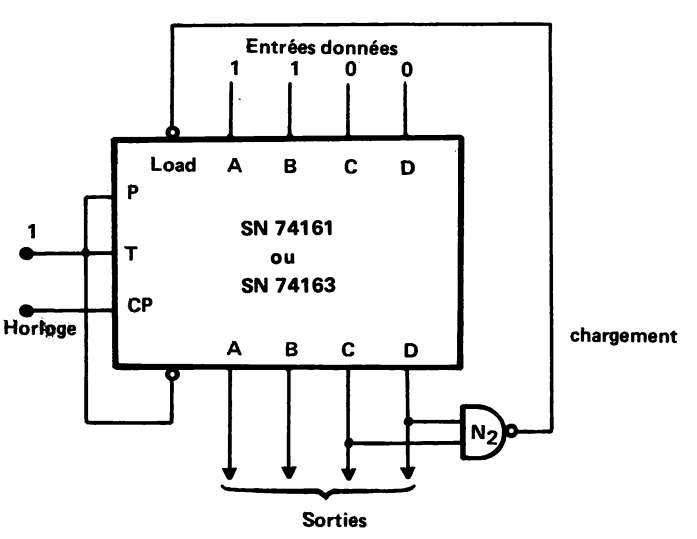


Fig. 15 : Compteur de 0 à 631

3.3. - **Compteur de N_1 à N_2** : ici, comme indiqué sur la figure 16, pour un compteur "Excess 3", code obtenu en additionnant systématiquement 3 au code BCD, N_2 (12) est décodé et autorise, au coup d'horloge suivant, le chargement de N_1 (3).



	D	C	B	A	
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	$N_1 = 3$
4	0	1	0	0	
5	0	1	1	1	
6	0	1	1	0	
7	0	1	1	1	excess 3
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	$N_2 = 12$
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

Fig. 16 : Compteur "Excees 3"

N_1 et N_2 peuvent prendre n'importe quelle valeur et ce type de compteur peut s'appliquer aussi bien aux compteurs binaires que décimaux, comme l'indique la figure 17 qui représente un compteur de 15 à 273 constitué de décades synchrones SN 74160 ou SN 74162.

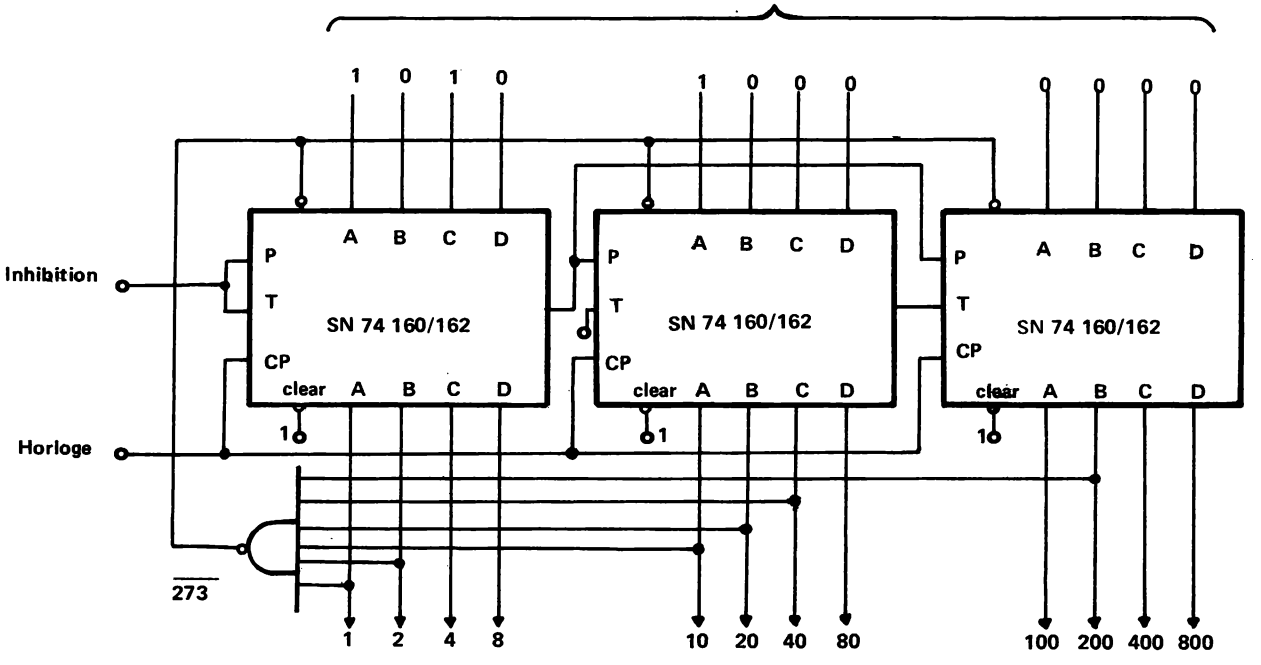


Fig. 17 : Compteur de 15 à 273

Générateurs de séquences utilisant le SN 54/74120 (NA 61)

NA 61 SN 54/74120 - DESCRIPTION ET APPLICATIONS

Certains circuits de contrôle nécessitent des générateurs de séquence, train d'impulsions, un unique, etc..., en fonction de diverses commandes externes. Le circuit SN 54/74120 (fig. 1a) permet de réaliser ces fonctions et peut être aussi utilisé en synchronisateur d'impulsions. Il se décompose en trois parties principales; chacune d'elles est constituée d'une bascule RS (fig. 1b). Ces bascules sont commandées par les entrées du circuit ou par des connexions internes.

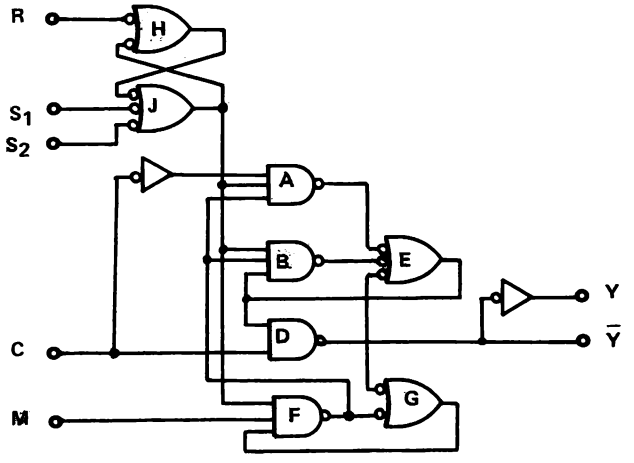


Fig. 1a : Schéma électrique du circuit SN 54/74120

Le passage des impulsions d'horloge vers la sortie est autorisé quand les entrées S_1 ou S_2 sont au niveau bas et inhibé quand R = 0 en fonction de la table de vérité de la figure 2.

Après initialisation par les entrées S_1 ou S_2, l'entrée "mode control" M détermine si une impulsion unique ou un train d'impulsions passera vers la sortie. En l'absence de commande d'arrêt, le circuit laisse passer les impulsions tant que l'entrée "mode control" est au niveau zéro.

Si "mode control" est au niveau haut, le circuit restitue uniquement une impulsion vers la sortie lors de chaque utilisation de S_1 (ou S_2) et R.

I. DESCRIPTION DU CIRCUIT

Le circuit est essentiellement composé de 3 bascules RS (fig. 1b). La bascule RS_1 est constituée par deux portes NAND H et J rétrocouplées. La sortie J est au niveau haut dès qu'une des entrées S_1 ou S_2 est active (niveau bas), elle restera dans cet état tant que l'entrée R ne sera pas au niveau bas. La porte J valide les portes NAND A, B, et F et autorise ainsi la commande des deux autres bascules RS_2 et RS_3.

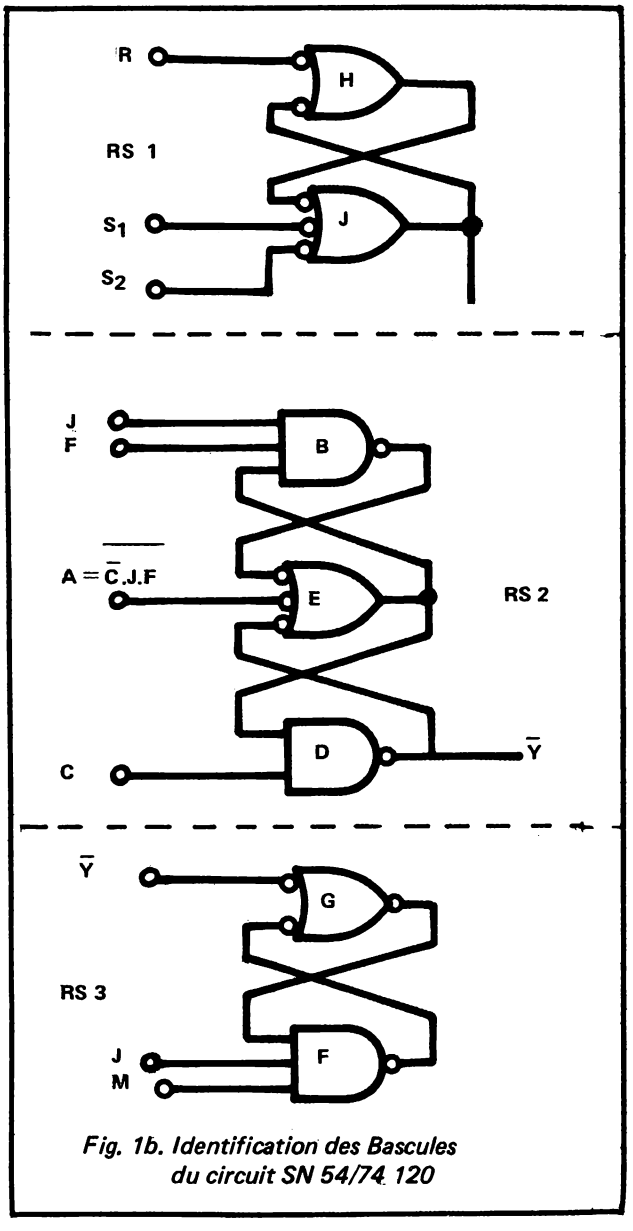


Fig. 1b. Identification des Bascules du circuit SN 54/74 120

La deuxième bascule RS_2 est composée par les portes B, E et D; c'est en réalité une double bascule RS qui, initialisée par la porte A, est maintenue dans son état par la porte B, tant que les sorties J de RS_1 et F de RS_3 restent au niveau haut, et maintenue par la porte D, tant que l'entrée C est au niveau haut.

Cette double condition de maintien permet de conserver toute la durée des impulsions d'entrée, même si le signal d'arrêt des impulsions R arrive pendant une période haute de l'horloge.

La troisième bascule RS est composée de circuits F et G. Elle détermine le mode de fonctionnement. Si M reste au niveau bas, elle n'a aucune action sur le fonctionnement du circuit.

Entrées			Fonction
R	S_1	S_2	
ϕ	0	ϕ	Sortie des impulsions
ϕ	ϕ	0	Sortie des impulsions
0	1	1	Inhibition de la sortie des impulsions
1	↓	1	Départ de la sortie des impulsions
1	1	↓	Départ de la sortie des impulsions
↓	1	1	Arrêt de la sortie des impulsions

Fig. 2. SN 54/74120 - Table de vérité.

1.1. - Circuit d'entrée (fig. 3)

Toutes les entrées, sauf l'entrée d'horloge C, sont ramenées au potentiel Vcc par une résistance de 10 KΩ, ce qui permet de commander le circuit directement par un interrupteur sans composant extérieur. De plus, les rebondissements de l'interrupteur n'ont pas d'effet sur le fonctionnements du circuit puisque les entrées sont suivies de bascules RS qui "nettoient les contacts.

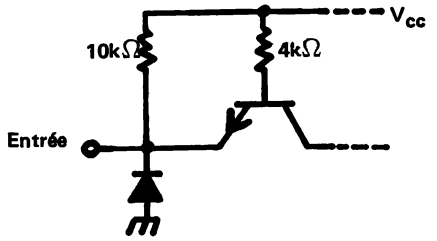


Fig. 3. Configuration des entrées R, S et M

Cette résistance augmente sensiblement le courant d'entrée qui est de 2,1 mA (au lieu de 1,6 mA) pour le niveau bas et de 0,2 mA (au lieu de 40μA) au niveau haut.

L'entrée d'horloge "C" est identique aux entrées TTL standard SN 54/74, si ce n'est son entrance qui est 2. Toutes les entrées sont protégées par des diodes d'écrêtage.

1.2 - Circuit de sortie (fig. 4)

Les circuits de sortie du type "totem-pole" avec DARLINGTON permettent de commander 60 charges TTL au niveau haut et 30 charges au niveau bas. De plus, les faibles impédances de sortie aux niveaux haut et bas facilitent la transmission sur lignes.

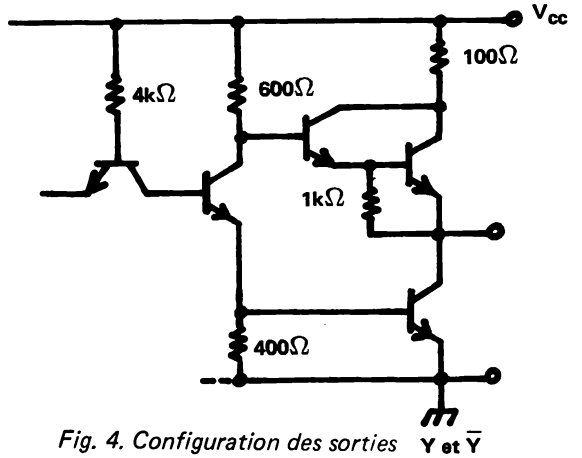
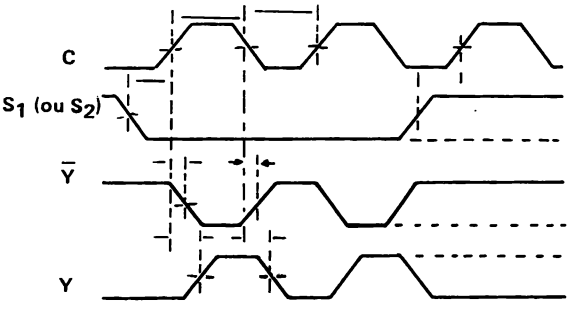


Fig. 4. Configuration des sorties Y *et* $\bar{Y}$

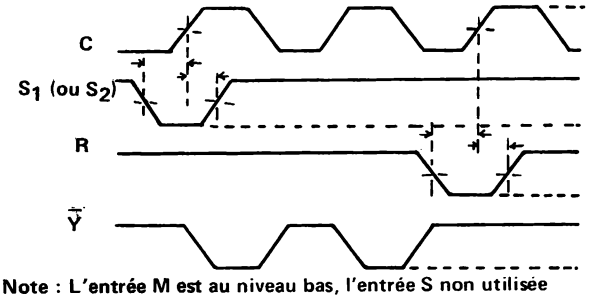
1.3. - Limites d'utilisation :

Le fonctionnement correct du circuit SN 54/74120 est lié au respect des temps de préconditionnement (t set-up) et de maintien (t hold) : les limites de ces deux temps pour les différentes entrées, ainsi que les temps de propagation de l'horloge sont répertoriés dans le tableau suivant :



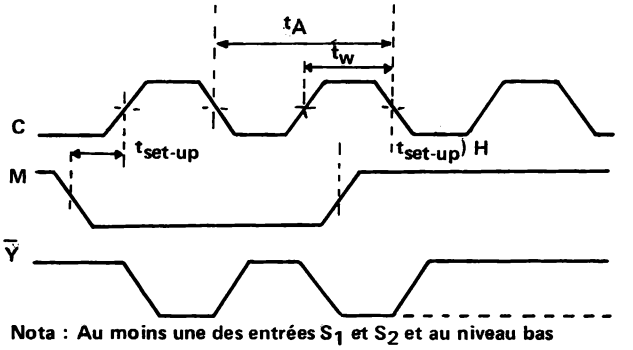
Note : Les entrées M et R sont au niveau bas, l'entrée S non utilisée est au niveau haut.

Fig. 5a : Commande d'un train d'impulsions par S



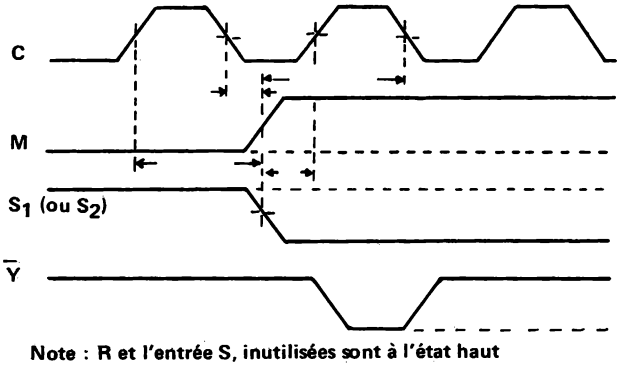
Note : L'entrée M est au niveau bas, l'entrée S non utilisée est au niveau haut.

Fig. 5b : Commande d'un train d'impulsions par S et R



Nota : Au moins une des entrées S_1 et S_2 et au niveau bas

Fig. 5c : Commande d'un train d'impulsions par M



Note : R et l'entrée S, inutilisées sont à l'état haut

Fig. 5d : Commande d'une impulsion unique

1.4 - Caractéristiques mécaniques et électriques :

Le brochage du circuit SN 54/74120 qui contient deux synchronisateurs d'impulsion identiques est indiqué sur la figure 6. Chaque synchronisateur consomme typiquement 127 mW. Le circuit SN 74120 est caractérisé pour fonctionner de 0°C à 70°C et le SN 54120 de -55°C à 125°C.

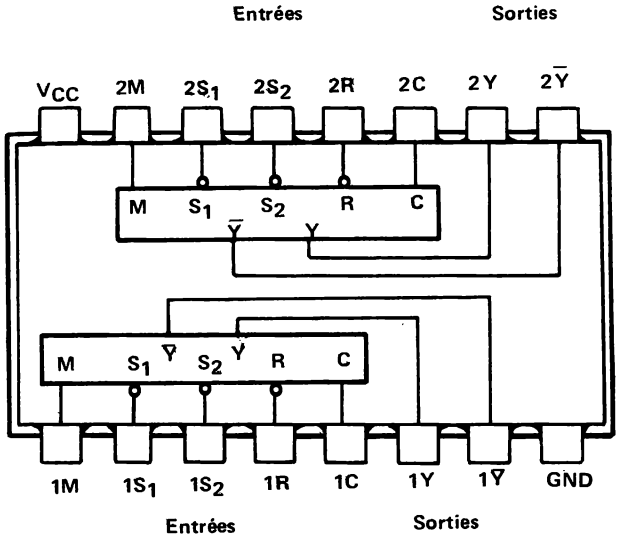


Fig. 6 : Brochage du SN 54/74120

II. APPLICATIONS TYPIQUES

2.1. - Commande d'un train d'impulsions par la bascule RS_1 (fig. 7 et 8) :

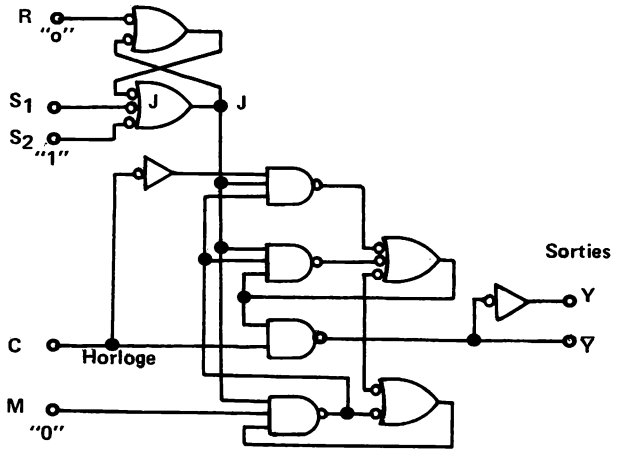


Fig. 7 : Commande d'un train d'impulsion par RS_1

Dans ce mode d'utilisation, la bascule RS_3 (fig. 1) n'est pas utilisée et l'entrée M est maintenue à "0". La bascule RS_1 est commandée par les entrées R, S_1 et S_2. Les impulsions de C passent vers Y tant que la sortie J de la bascule RS_1 est au niveau haut. Cette bascule peut être commandée de deux manières différentes:

1er cas : La porte J est utilisée comme un inverseur : R doit être au niveau zéro pour n'avoir aucune action sur la porte J. Le passage des impulsions est autorisé pendant toute la période où S_1 (ou S_2) est à zéro.

2ème cas : Les entrées S_1 (ou S_2) et R sont utilisées. Le passage des impulsions est autorisé entre la mise à zéro de S_1 (ou S_2) et celle de R.

Ces deux possibilités sont représentées sur les figures 7A, 7B et 7C pour le 1er cas et les figures 8A et 8B pour le deuxième cas. Les temps de "set up" et de "hold" à respecter sont représentés sur les figures 5A et 5B.

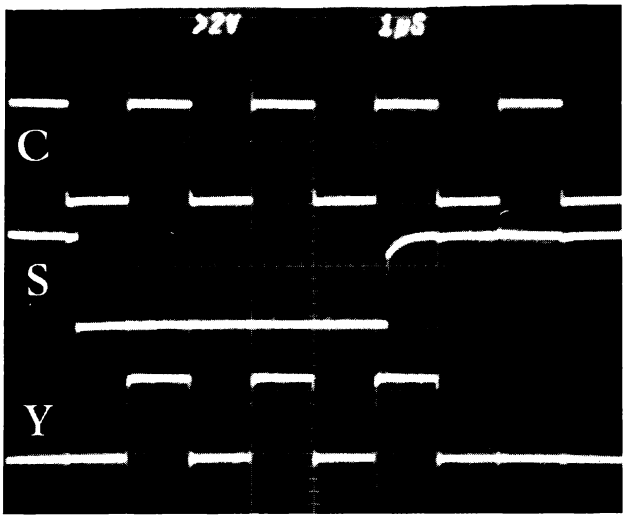


Fig. 7 A

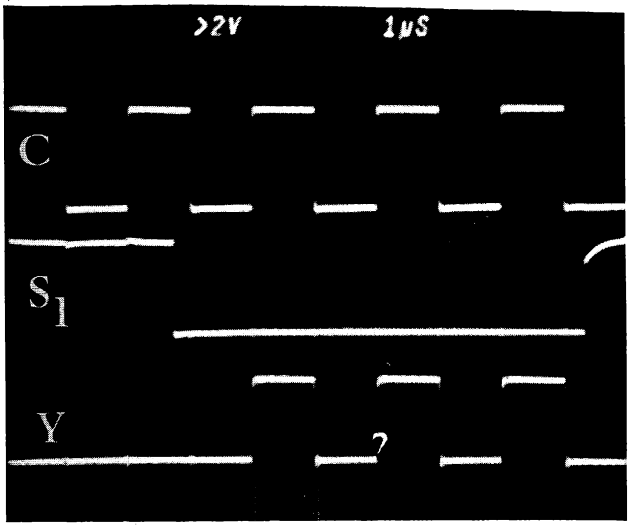


Fig. 7 B

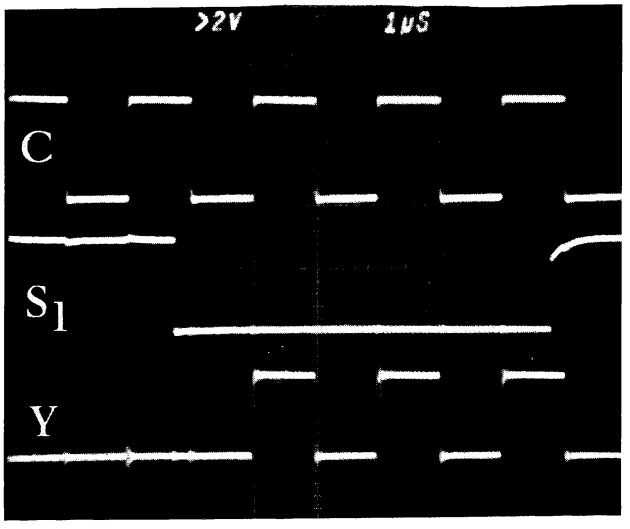


Fig. 7C

La première impulsion entière après la transition négative de S_1 ou S_2 est transmise vers $\overline{Y}$ (voir figures 7 et 8). Une impulsion d'horloge entamée à la transition positive de S_1 ou S_2 (fig. 7C), ou négative de R (fig. 8A), ne sera pas tronquée.

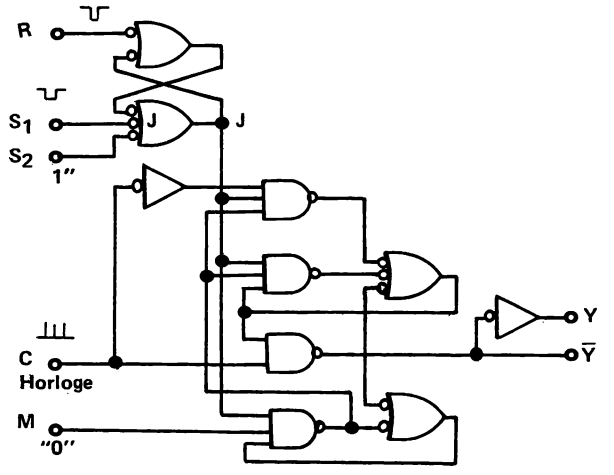
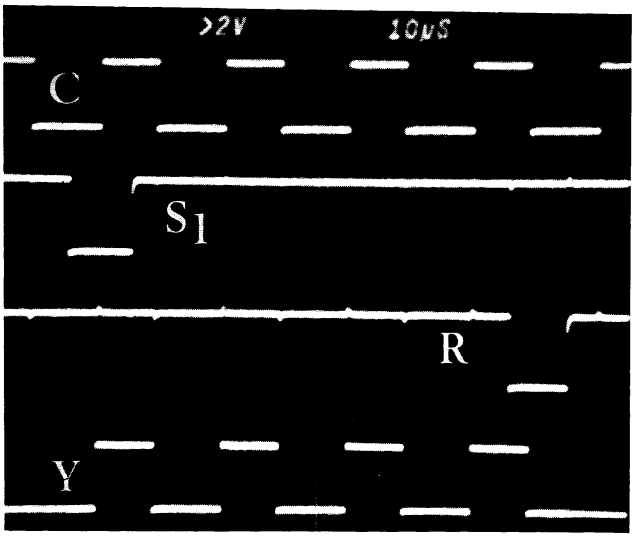
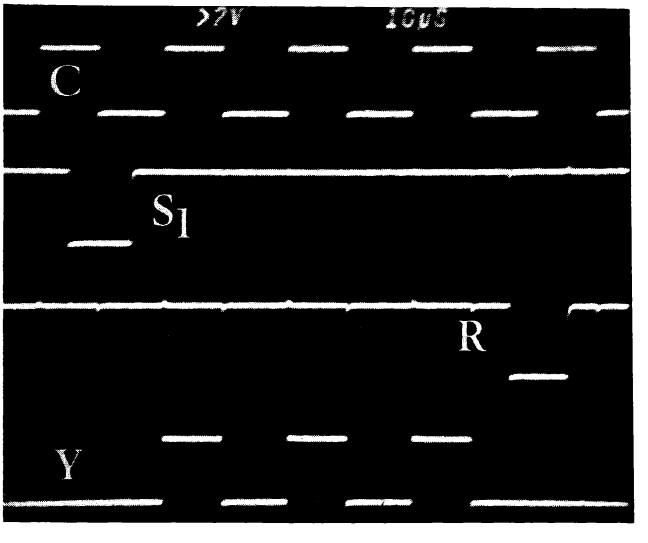


Fig. 8





FONCTIONNEMENT DETAILLE :

Le fonctionnement est identique pour les deux cas; la correspondance entre les deux utilisations est indiquée sur la figure 9 en a et b.

A la transition négative de S, la sortie de la porte J est au niveau haut (fig. 1) tandis que, dans l'exemple de la figure 9, C = 1. Puisque A = J.$\overline{C}$.F., la sortie de la porte A reste à 1 tant que l'horloge C n'est pas au niveau zéro.

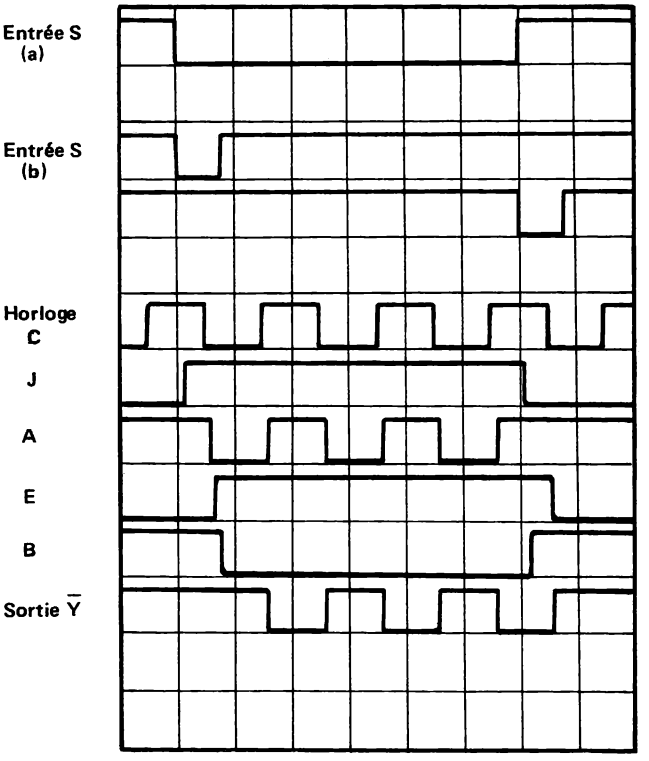


Fig. 9

Lorsque C = 0, A passe à "0" puisque J.F = 1 (M = 0 dans ce mode d'utilisation). La bascule RS_2 formée par les portes E et B change d'état : E, qui était initialement à l'état bas, passe à "1", maintient un "0" en B et autorise le passage des impulsions de C vers $\overline{Y}$ ou Y.

La transition négative de S aurait pu se produire pendant une période où C = 0. Dans ce cas, la bascule RS_2 aurait basculé immédiatement après le retard apporté par A.

A la transition positive de S ou négative de R suivant le cas, J passe à "0" et les portes A et B sont bloquées. La bascule RS_2 n'est plus maintenue par la porte B, mais par D (ou $\overline{Y}$) tant que l'horloge C = 1. Si cette transition arrive lorsque C = 0, $\overline{Y}$ passe à 1 et la bascule RS_2 revient à son état initial (E = 0) dès la transition négative de S.

2.2. - Commande d'un train d'impulsions par M, S et R (Figure 10) :

Dans ce cas, les 3 bascules RS_1, RS_2 et RS_3 sont utilisées.

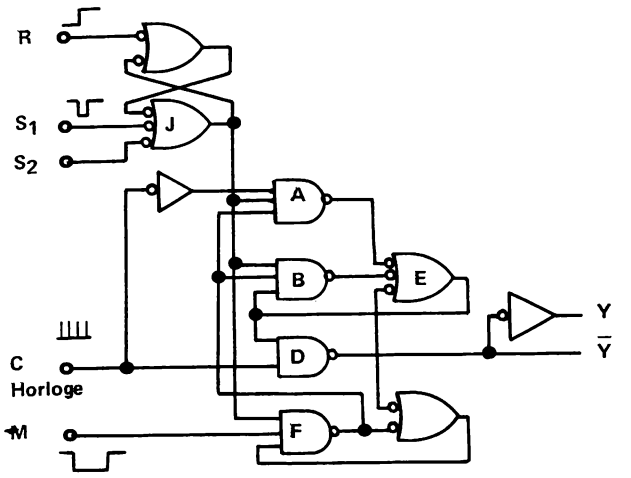


Fig. 10

Le train d'impulsions est initialisé par S_1 ou S_2 de la même manière que précédemment, alors que l'arrêt des impulsions en sortie est déterminé par l'entrée M (figures 10 A et 10 B). Les temps de "set up" et de "hold" qui doivent être respectés sont indiqués sur la figure 5 C.

La première impulsion complète qui apparaît en sortie est obtenue comme décrit au paragraphe 2.1 : elle suit la transition négative de S_1 (ou S_2). Si la remontée de M se fait durant la période TA (fig. 5C), la dernière impulsion de sortie sera celle contenue dans TA (figures 10 A et 10 B).

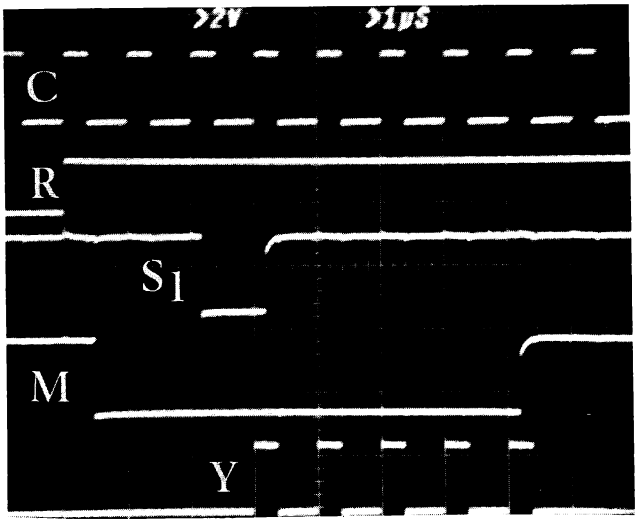


Fig. 10 a

Fonctionnement détaillé :

Le fonctionnement est identique au cas précédent (2 - 1) pour le début du train d'impulsion de sortie, dans la mesure où M = 0 lorsque S_1 ou S_2 est actif (fig. 11), Pendant la période comprise entre la première impulsion en $\overline{Y}$ et la remontée de M, la porte F est bloquée, la porte G se comporte comme un inverseur; après cette période, la bascule RS_3 redevient une bascule RS.

A la transition positive de M, si $\overline{Y}$ est au niveau haut, la bascule ne change pas d'état et F = 1. Dès que $\overline{Y}$ =0, RS_3 change d'état (G passe à 1) car, à cet instant, $F = \overline{G.M.J.} = 0$. Les deux portes A et B sont bloquées et la bascule RS_2 est maintenue par la porte D tant que $\overline{Y}$ est au niveau zéro.

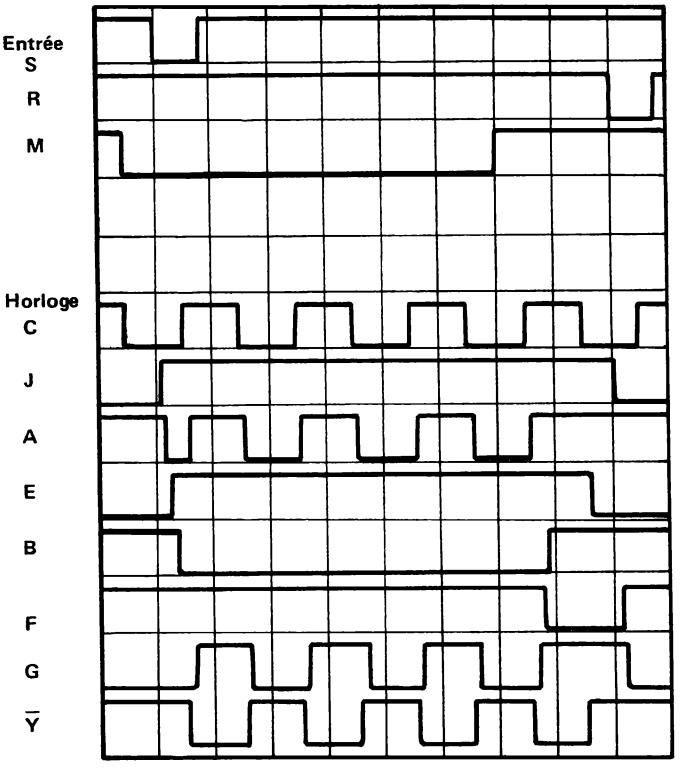


Fig. 11

Si, par contre, $\overline{Y} = 0$ à la transition positive de M, la bascule RS_3 change d'état immédiatement, les portes A et B sont bloquées, la bascule RS_2 est maintenue par la porte D tant que Y = 0, c'est-à-dire tant que l'impulsion n'est pas terminée.

2.3. - Génération d'une impulsion unique (figure 12):

Cette utilisation du circuit SN 54/74120 est identique au cas précédent, si ce n'est que la transition négative de S_1 (ou S_2) et la transition positive de M se font en même temps. Il est alors possible de générer une impulsion unique de différentes façons :

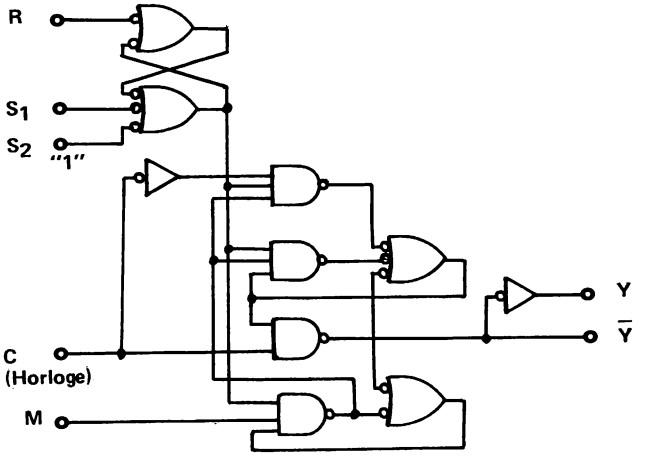
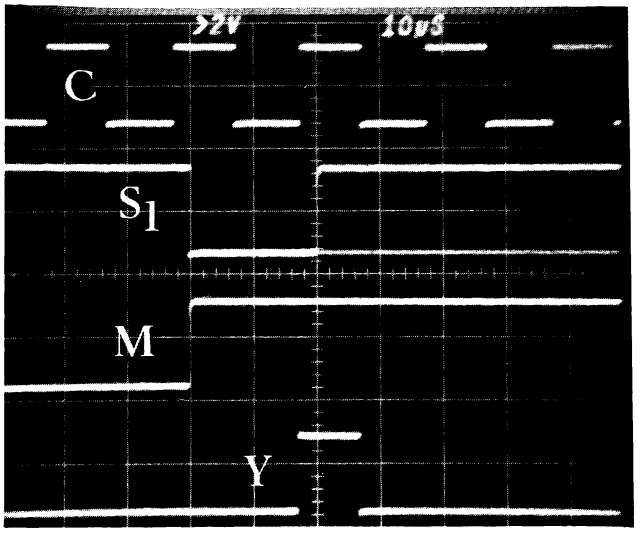
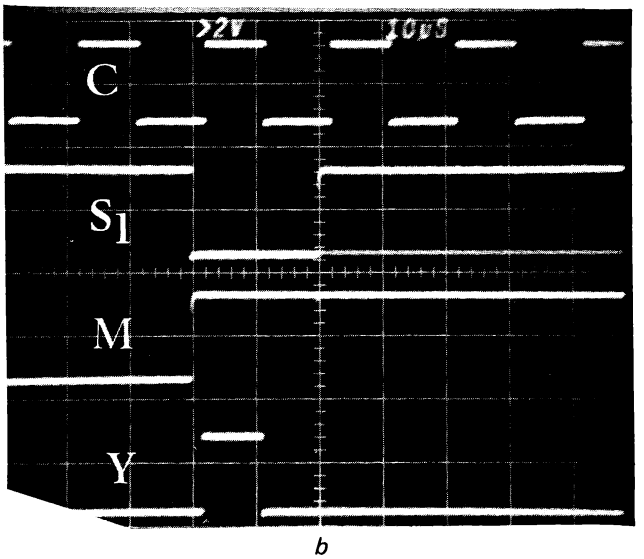


Fig. 12

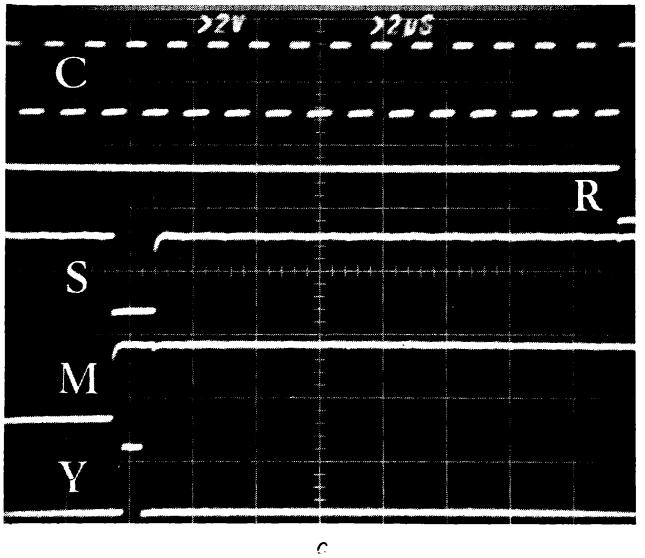
a) figures 12 A et 12 B : R est au niveau bas. Les transitions négatives de S_1 ou S_2 et positives de M sont synchrones. Dans ce cas, la durée de S_1 doit être supérieure à 1,5 T_A, T_A étant la période de l'horloge C.



a



b



c

b) figure 12 C : ici, la bascule RS_1 est remise à zéro par une impulsion sur R après la génération du 1 unique par les entrées S et M, comme indiqué en 2.3.a.

c) une dernière possibilité consiste à maintenir la commande M à l'état "1", le reste du cycle se ramenant aux cas précédents.

Les temps de "set up" et de "hold" à respecter sont indiqués sur la figure 5 D.

Fonctionnement détaillé :

Le diagramme des temps de la figure 13 décrit en détail l'utilisation mentionnée en 2 - 3 - b (figure 12 c). Il est facile de voir que le fonctionnement interne correspondant aux deux autres possibilités est identique.

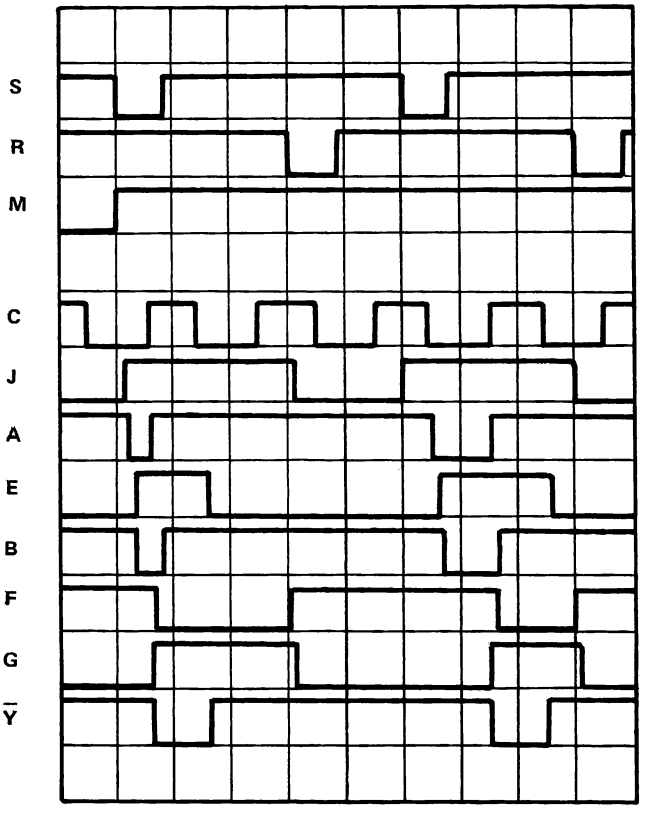


Fig. 13

E et G sont initialement à l'état "0". Lors de la transition négative de S, les portes A et B sont libérées et A est amené à "0", ce qui force E à l'état "1", amène B en "0" (B = E.J.F), maintenant un "1" en E.

La porte D se comporte alors comme un inverseur et $\overline{Y} = 1$. A la transition positive de C, A passe à "1", Y à 0 donc G prend l'état "1", F l'état "0" et E n'est maintenu à 1 que par $\overline{Y}$. Enfin, quand l'horloge passe à "0", $\overline{Y}$ remonte à "1", donc E est à "0", bloquant ainsi tout passage d'impulsion à travers D. Pour générer une nouvelle impulsion, les bascules RS_1 et RS_3 devront être remises à zéro par l'entrée R.

III. CONCLUSION

Les quelques exemples vus précédemment montrent la grande flexibilité de ce circuit et l'intérêt qu'il présente pour l'ingénieur de projet lors de la réalisation de :

- générateur de séquence.
- base de temps
- synchronisateur d'impulsions.

A titre d'exemple, la figure 14 montre l'utilisation du circuit SN 54/74120 dans un synchronisateur pour base de temps d'oscilloscope. L'inverseur 1 permet de faire le choix entre une impulsion unique ou un train d'impulsions. En position train d'impulsions, le départ est commandé par le bouton poussoir 2 et l'arrêt par le 3. En impulsion unique, l'inverseur 1 force un zéro sur l'entrée R et chaque fois que l'on utilise le bouton poussoir 2, le circuit génère une impulsion unique.

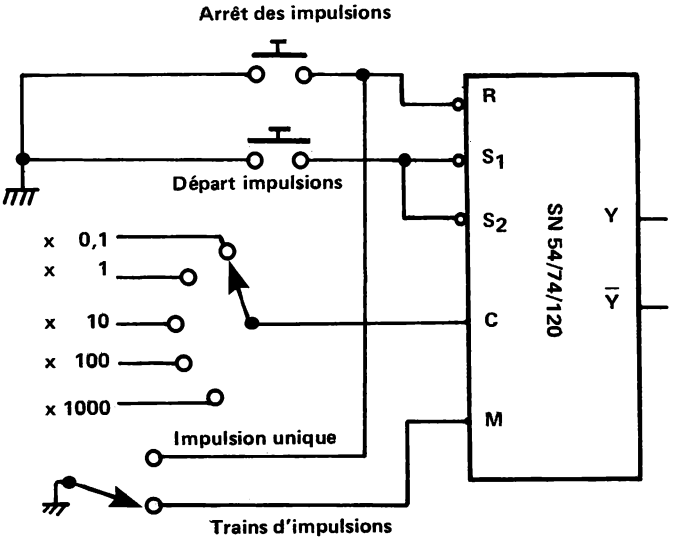


Fig. 14

ANNEXE
ANALYSE DU SYNCHRONISATEUR
SN 54/74120

La figure A donne le schéma du circuit SN 54/74120 en mettant en évidence les 3 variables secondaires G, E et Y; la bascule RS_1 n'a pas été dessinée sur ce schéma, son action étant représentée par le signal J.

L'équation logique de G, E et Y est :

$$G = y + JMg$$
$$E = y + J.(\overline{M} + \overline{g}).(\overline{C} + e)$$
$$Y = e.C$$

Lorsque J = 0, ces équations deviennent : Si J=1, il vient:

$$E = G = y \qquad G = y + M.g$$
$$Y = e.C \qquad E = y + (\overline{M} + \overline{g}).(\overline{C} + e)$$
$$Y = e.C$$

Dans ces conditions, il est possible de tracer la table de transition correspondant à ces équations, comme indiqué sur la figure B.

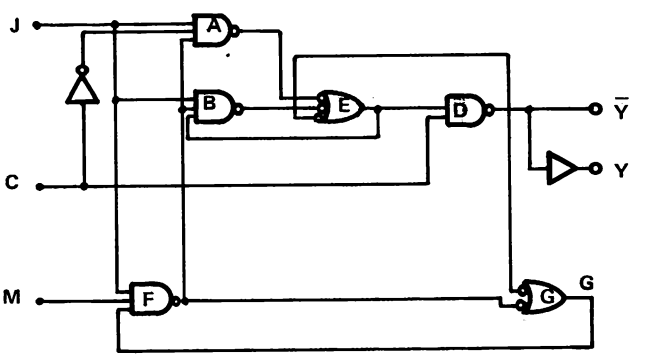
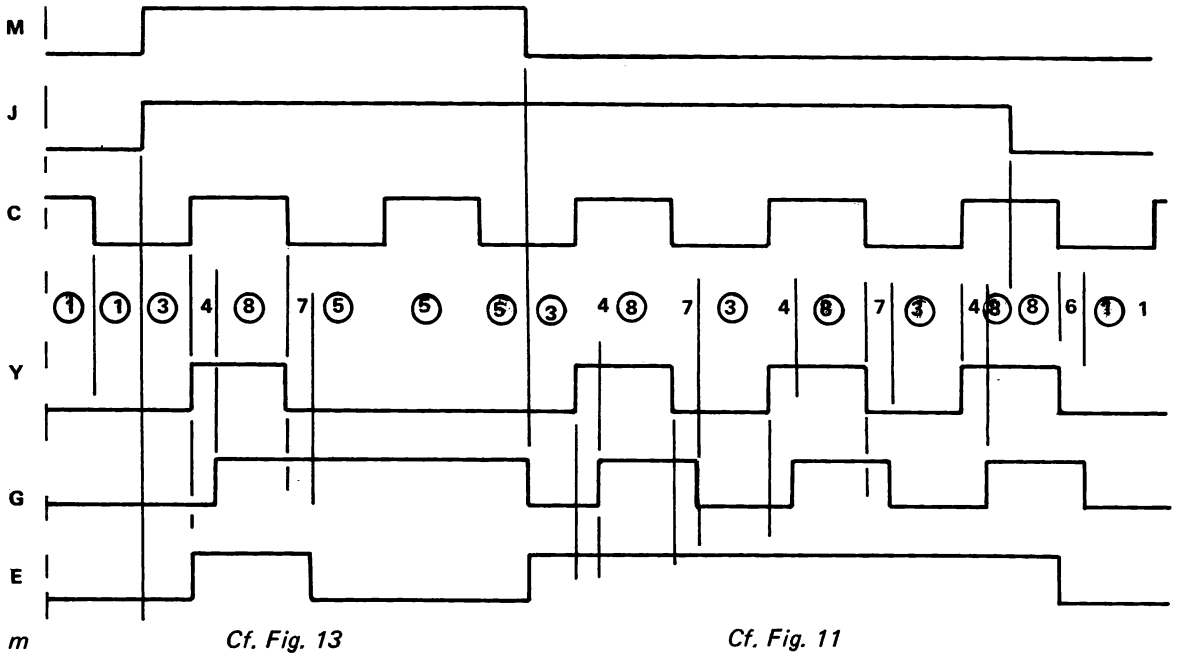


Fig. 15

La figure C donne un exemple d'utilisation de cette table pour une séquence arbitraire. Sur cette figure est indiquée la succession d'états stables ou instables pris par les variables secondaires.

ETATS		J = 0		J = 1			
		CM 0 0	CM 1 0	CM 0 0	CM 0 1	CM 1 1	CM 1 0
1	[0 0 0]	[0 0 0]	[0 0 0]	0 1 0	0 1 0	[0 0 0]	[0 0 0]
2	0 0 1	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0
3	[0 1 0]	0 0 0	0 0 1	[0 1 0]	[0 1 0]	0 1 1	0 1 1
4	0 1 1	1 1 0	1 1 1	1 1 0	1 1 0	1 1 1	1 1 1
5	[1 0 0]	0 0 0	0 0 0	0 1 0	[1 0 0]	[1 0 0]	0 0 0
6	1 0 1	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0
7	1 1 0	0 0 0	0 0 1	0 1 0	1 0 0	1 0 1	0 1 1
8	[1 1 1]	1 1 0	[1 1 1]	1 1 0	1 1 0	[1 1 1]	[1 1 1]
	g e y	G E Y	G E Y	G E Y	G E Y	G E Y	G E Y

Il est, bien sûr, possible d'utiliser le tableau de transition pour d'autres séquences.



Cf. Fig. 13

Cf. Fig. 11

Applications of the schmitt trigger SN 7413 N

(B 81)

CHARACTERISTICS AND APPLICATIONS OF THE SN7413N DUAL SCHMITT TRIGGER

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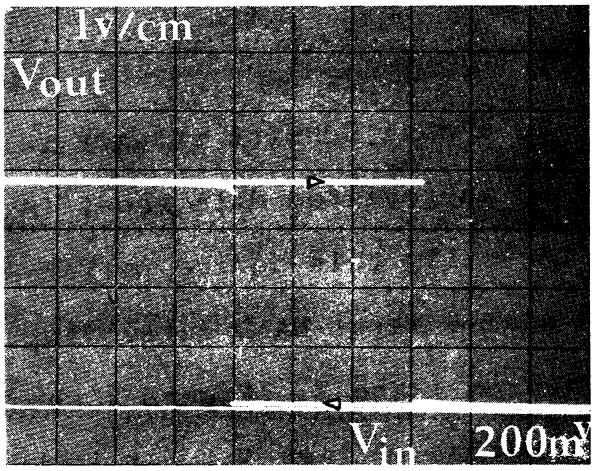


Fig. 1

1. INTRODUCTION

There has long been a requirement for a device that would interface between slow systems and TTL. There is also a need for a simple clock generator that would cover a wide frequency range with a minimum of components.

Up to the present time the only satisfactory solution to both these problems has been to use discrete components. The SN7413N has been designed to meet both these needs.

2. DESCRIPTION

The SN7413N is a dual Schmitt trigger fully compatible with standard TTL. An abbreviated data sheet is given at the back of this report. Logically this device performs the same function as the SN7420N dual 4 input NAND gate. Input-output characteristics are shown in Figures 1 and 2. Figure 1 shows input voltage V_{in} plotted against output voltage V_{out} at 100kHz. The logical '1' and '0' output levels are identical to those of standard TTL. Although propagation delay from input to output is typically 16ns, only 6ns is required to switch the Schmitt section from one state to the other.

Figure 2 shows input current, I_{in}, plotted against V_{in}. For negative values of V_{in} greater than 0.5 V the internal clamp diodes conduct. This current should be limited to 5mA per input.

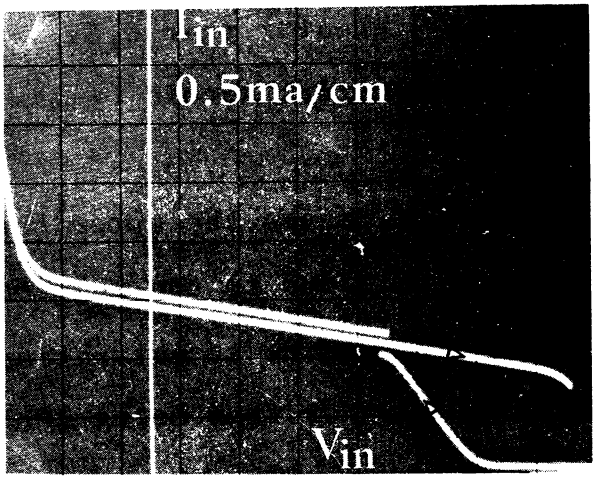


Figure 2

As the input voltage passes the upper threshold the input current decreases rapidly due to the multiemitter input transistor saturating. This then remains in saturation until the lower threshold is passed, the input current then being determined by the input characteristics of a normal TTL gate, i.e. slope impedance of 4kΩ in series with a diode.

3. APPLICATIONS

3.1. Sine to square wave conversion

This is one of the simplest applications of the Schmitt and is shown in Figure 3.

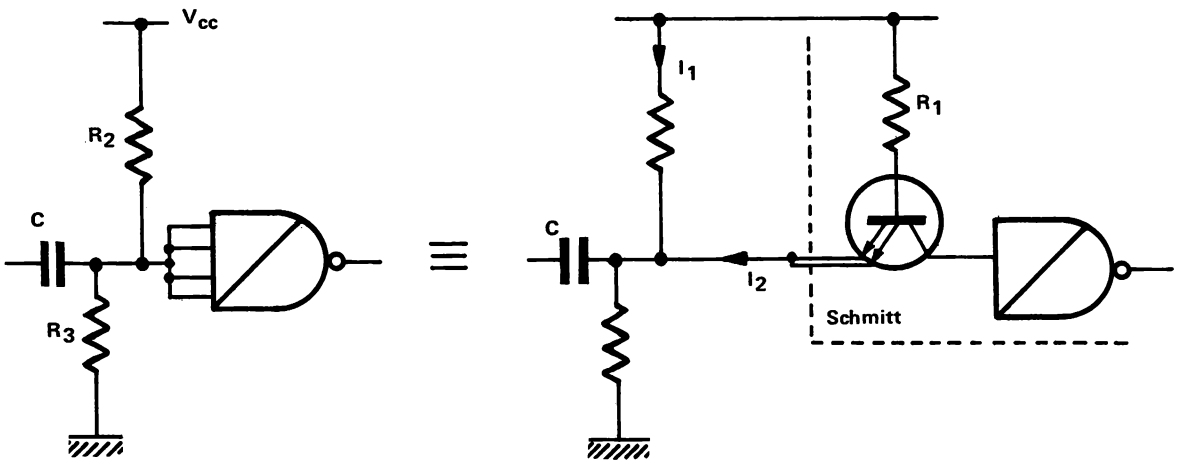


Figure 3

The resistive divider R2 and R3 biasses the Schmitt input midway between the upper and lower thresholds. This gives a 1 : 1 mark-space ratio with sinusoidal inputs. The values of resistors R2 and R3 may be determined as follows.

The voltage at the multiemitter input

$V1 = (I1 + I2).R3$

where

$V1 = (V_{T1} + V_{T2})/2$

V_{T1} and V_{T2} being the upper and lower Schmitt thresholds

$$\therefore \quad V1 = (V_{CC} - V1)/R2 + (V_{CC} - V1 - V_{BE})/R1 \; . R3$$

$$\therefore \quad R3 = V1./\,(V_{CC} - V1)/R2 + (V_{CC} - V1 - V_{BE})/R1 \qquad \ldots (1)$$

$$\text{and} \quad R2 = (V_{CC} - V1).R3/\;R1.V1 - R3.(V_{CC} - V_{BE} - V1) \qquad \ldots (2)$$

Typical values for the variables in equations (1) and (2) are

V_{T1}	=	1.7V
V_{T2}	=	0.9V
V_{CC}	=	5.0V
R1	=	4.0kΩ
V_{BE}	=	0.75V

Thus choosing resistor R3 = 470Ω, from equation (2) R2 = 1.83kΩ, i.e. R3 = 470Ω and R2 = 1.8kΩ in preferred values.

If R2 = 00 then equation (1) becomes

$R3 = R1[2.\,(V_{CC} - V_{BE})/(V_{T1} + V_{T2}) - 1]$

substituting values in this equation gives

R3 = 1.76kΩ i.e. 1.8kΩ

This shows that the device can be operated in a self biased mode.

The circuit of Figure 3 is suitable for use up to 8MHz with sinusoidal inputs. The value of capacitor C should be such that its reactance at the operating frequency is $\ll$ R2.R3/(R2 + R3).

Typical operating waveforms obtained with the self biassed mode at 1MHz are shown in Figure 4.

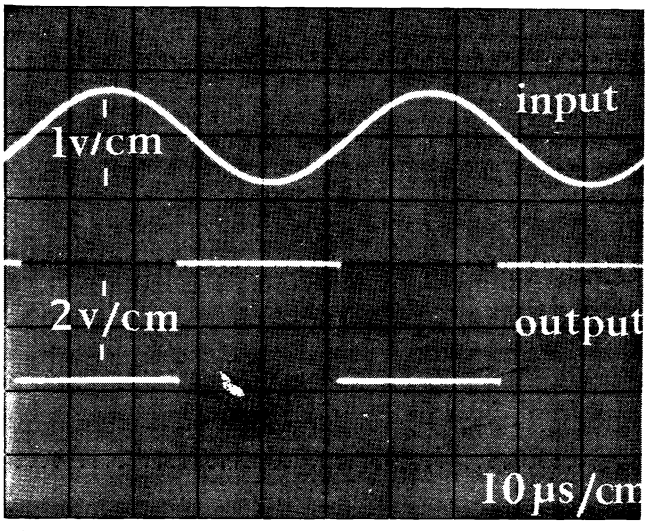


Fig. 4

3.2. Pulse Shaper

There are many instances where available input signals are not compatible with TTL. For example, a data waveform might have rise and fall times of > 60ns but TTL requires edges < 50ns for reliable operation. The circuit shown below, Figure 5, enables TTL to be driven from such sources.

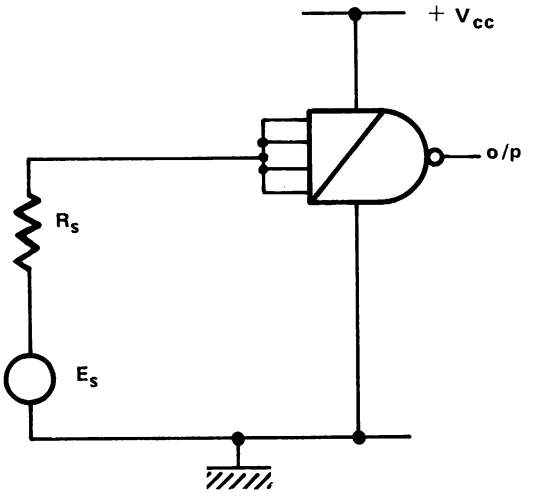


Figure 5.

The maximum permissible value of source resistance, R_S, is determined by the maximum input current when the input is at a logical "0", i.e. below the lower threshold voltage. To ensure a noise margin of 300mV the input current is measured at V_{in} = 400mV. A maximum value of 1.6mA at V_{in} = 0.4V is guaranteed on the data sheet.

$\therefore R_{S(max)} = V_{in}/I_{in(max)} = 400/1.6 = 250\Omega$

For noise margins other than 300mV, i.e. V_{in} = 0.4 the minimum value of internal base resistor R1 must be calculated in order to determine a maximum value of resistor R_S. Figure 6 illustrates the variable determining the value of resistor R1.

For V_{in} = 0.4V $\quad V_{CC(max)} = 5.25V$

$R1_{min} = (V_{CC(max)} - V_{BE}) / I_{max}$

$R1_{min} = (5.25 - 0.75) / 1.6\ k\Omega$

R1 min = 2.56kΩ

For a noise margin, E, the maximum value of resistor R_S in Figure 7 is given by

$R_{S(max)} = (V_{T(min)} - E).\ R1/\ (V_{CC} - V_{BE}) - (V_{T(min)} - E$

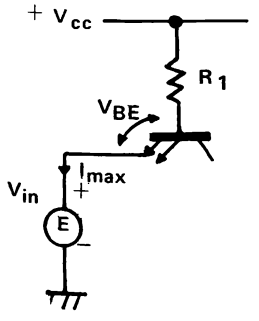


Figure 6

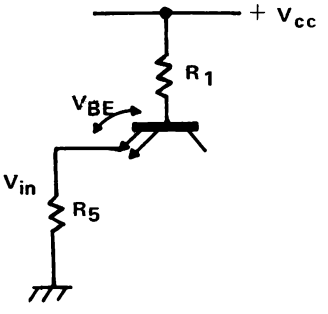


Figure 7.

For a noise margin E of 100mV and V_{CC} = 5.0V

$R_{S(max)} = (0.7 - 0.1)\ 2.56 \times 10^3 / (5.0\text{-}0.75) - (0.7 - 0.1).$

$R_{S(max)} = 421\Omega$

3.3 Pulse stretcher

This circuit (Figure 8) uses the internal 4kΩ base resistor of the Schmitt multiemitter input transistor as one of the timing components (see figure 9).

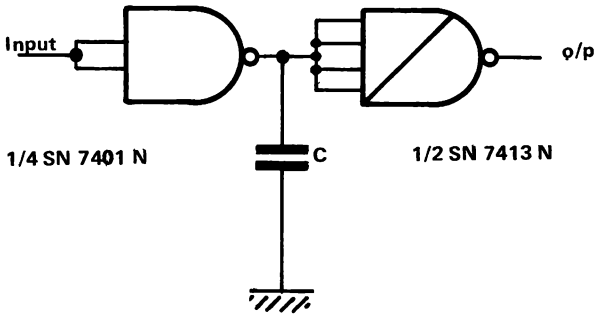


Figure 8

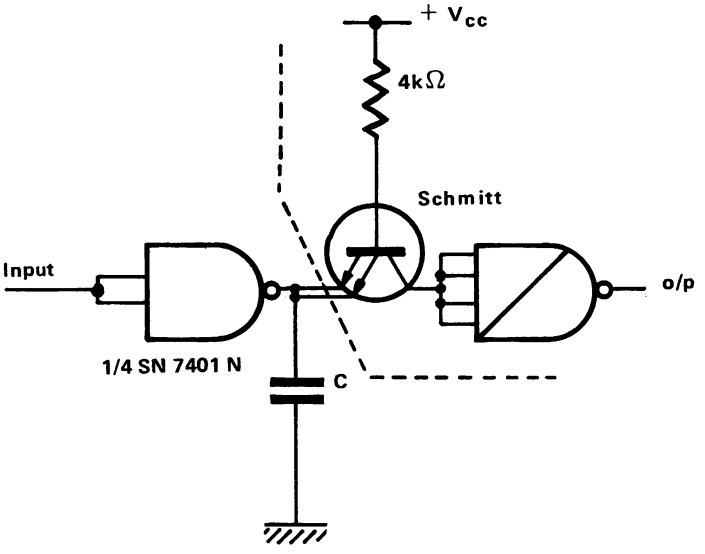


Figure 9.

There is a small delay between the leading edges of the input and output pulses, due to the time taken to discharge capacitor C through the saturation resistance of the output transistor of the SN7401N and the series current limited resistor.

For high repetition rates and large values of capacitor C the mean dissipation in the SN7401N output stage should be limited to 10mW by inclusion of a series resistor between its output and capacitor C.

Typical operating waveforms for this circuit are shown in Figure 10.

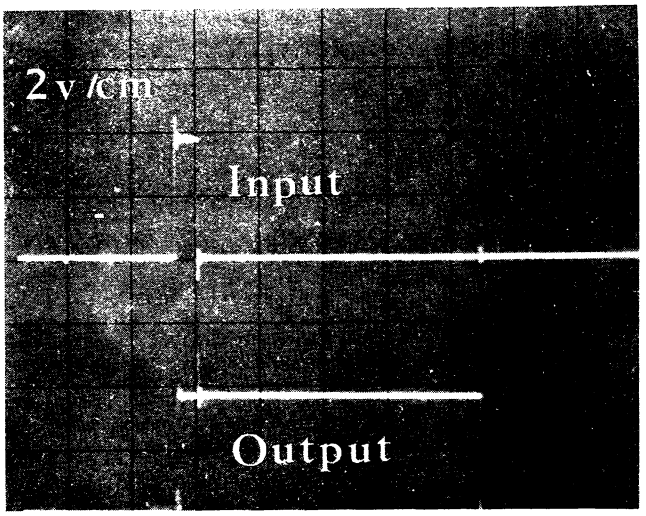


Figure 10.

3.4. Low pass filters - simple CR

The filter shown in Figure 11 is all that is needed, in the majority of cases, to eliminate noise associated with input signals. To maintain noise immunity at the Schmitt input the maximum value of resistor R should be limited as outlined in the section on pulse shaping. This, therefore, determines the value of capacitor C for a given 3dB cut-off frequency, f_o, of the filter, i.e. $C = 1/2\pi Rf_o$. The rate of attenuation past the cut-off frequency is 6dB/octave. For larger rates of attenuation and faster response times multipole Chebyshev filters should be used as described in the next section. Since the input to the Schmitt is always positive with respect to ground capacitor C may be a large value electrolytic.

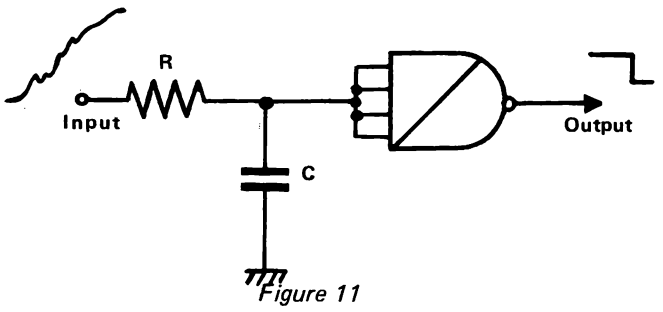


Figure 11

3.5. Low pass filter - Chebyshev

These filters should be used when digital equipment is required to operate under conditions of extreme electrical noise. (Such conditions can occur in industrial systems where induced voltages on signal lines may be as large as 1kV at 500kHz).

The Chebyshev filter is characterised by an amplitude frequency response that "ripples" in the pass band and falls off rapidly past the cut-off frequency f_o. The general form of this type of filter is shown in Figure 12.

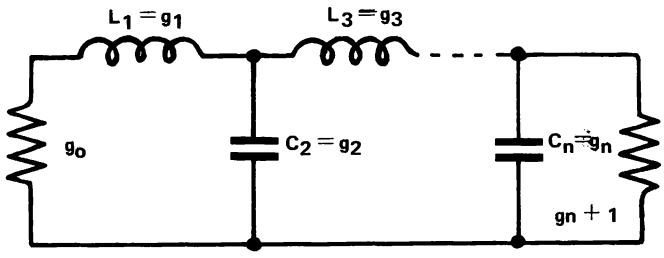


Figure 12

The amplitude frequency response of such a filter is shown in Figure 13.

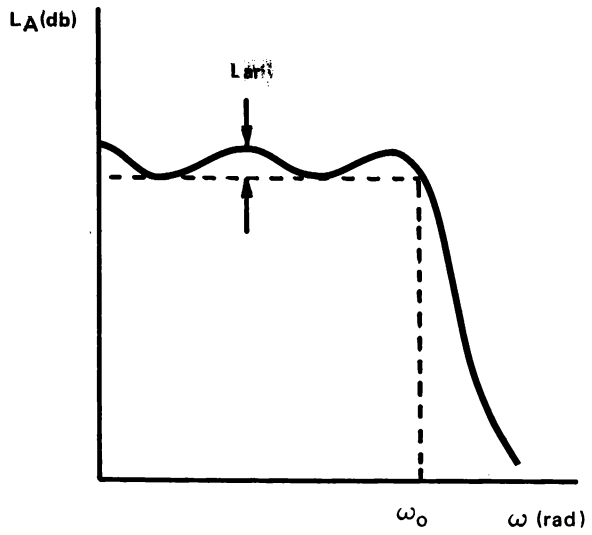


Figure 13.

The circuit form is well suited to mechanical construction since the capacitive elements can be lead through capacitors. The required DC operating conditions for the Schmitt trigger are easily satisfied since the filter has almost zero impedance at D.C.

A compromise has to be made between the rate of attenuation and the number of elements required.

In practice a 4 element filter that has an attenuation of 60dB at $4\omega^o$ (where ω^o is the angular cut-off frequency) is useful.

The load resistance R_{n+1} is determined by the nominal 4kΩ input impedance of the Schmitt trigger. This then determines the source impedance g_o. For a 4 element filter with 1dB ripple in the pass band $g_o \equiv 1.5k\Omega$

The table in Figure 14 gives element values against f_o for the circuit shown in Figure 15.

Element values for 4 element filter with L_{ar} = 1dB a and L_A = -60dB at $4\omega^{\circ -}$

The frequency response of a filter with f_o = 100kHz L_{ar} = 1dB R_S = 1.5kΩ and operating into a SN7413N load is shown in Figure 16, curve 2.

In many applications the signal is obtained from a low impedance source. The filter of Figure 12 can be modified for this mode of operation. This is shown in Figure 17.

In the circuit of Figure 17 R_L is again 4.0kΩ and the source conductance g_S is = oo (short circuit).

A practical form of this circuit is shown in Figure 18.

Table 2 gives element values for the filter of Figure 18.

Element values for 4 element filter with L_{ar} = 1dB and L_A = -60dB at $4\omega^{\circ}$

The response of a filter of the type shown in Figure 18 is shown in Figure 16, curve 1. (Note this filter has been designed for L_{ar} = 3dB not 1dB as given in tables).

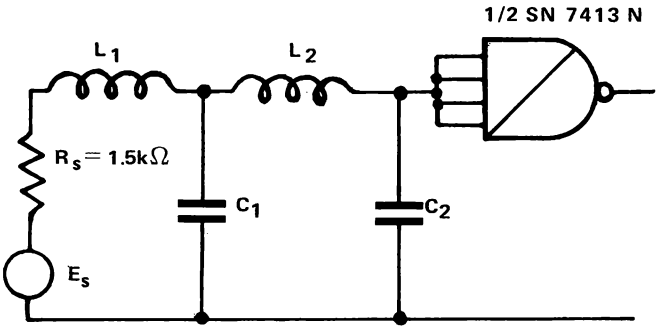


Figure 15.

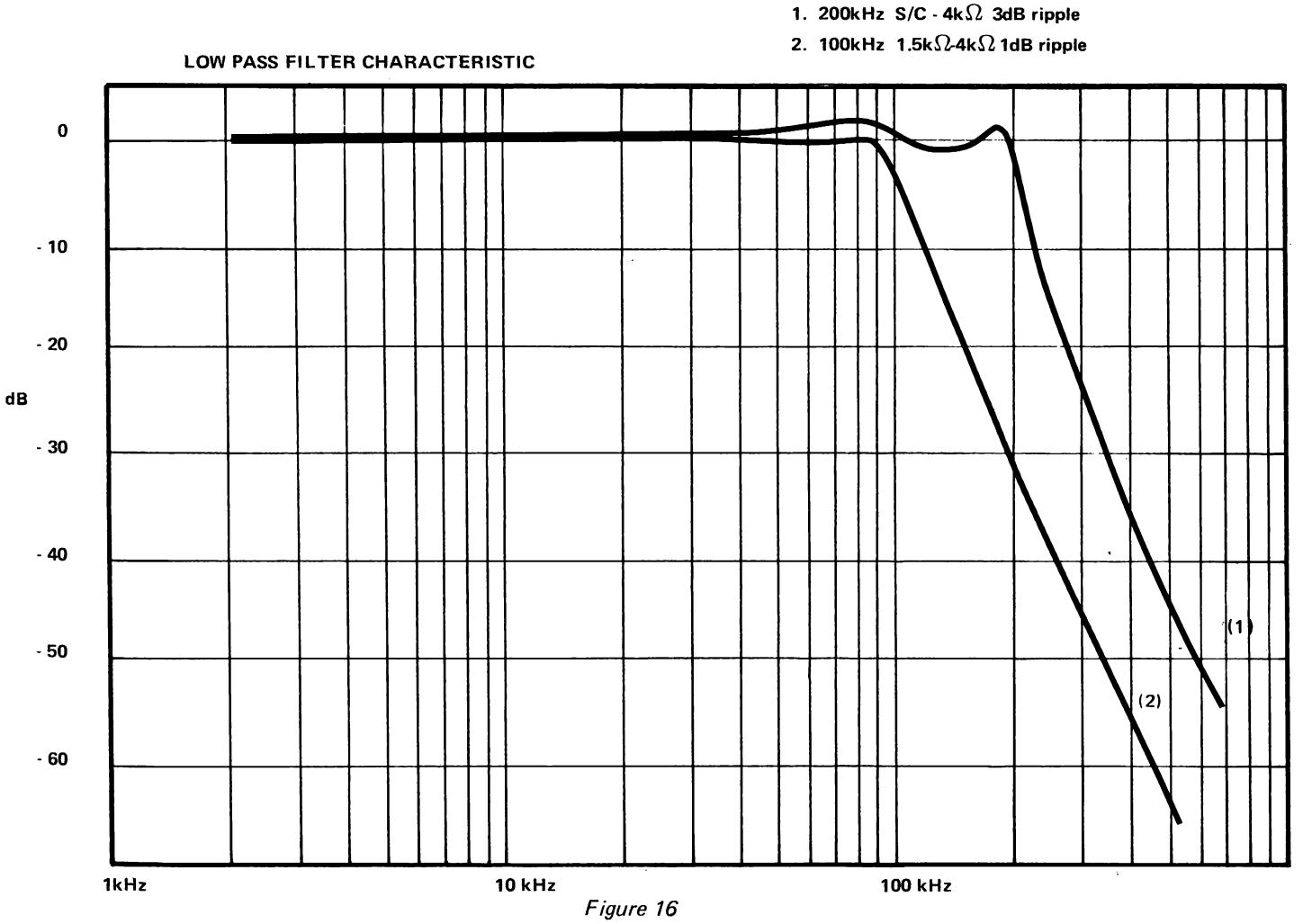


Figure 16

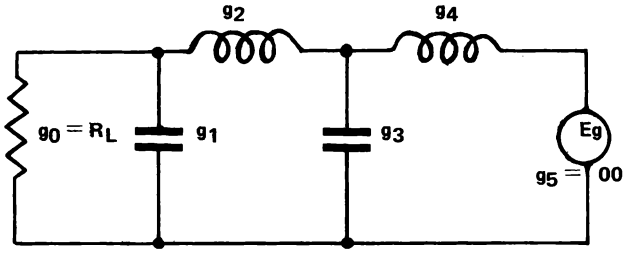


Fig. 17. Filter driven from zero source impedance

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	50	80
3	6	125	200
4	11	175	280
5	19	250	400
6	28	325	520

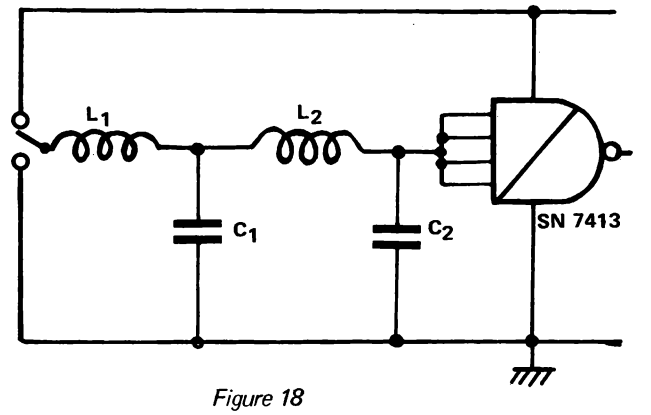


Figure 18

Since the inductive and capacitive components are ∞ 1/f element values for any cut-off frequency f_0 may be calculated from the tables given. Additional components may be added to the circuit of Figure 18 to enable it to handle very large voltage surges at the filter input. (See Figure 19).

Diodes D1 and D2 clamp the input to the Schmitt trigger to within (V_{CC}-V_F) and $-V_F$. They should be situated after inductor L1 so that the rate of rise of voltage across diodes D1 and D2 is limited.

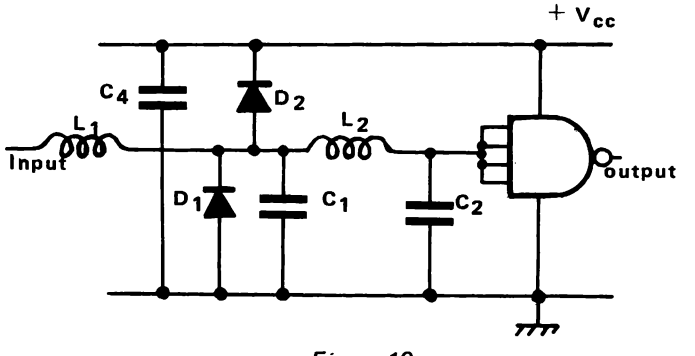


Figure 19

The filters described in the previous sections can be constructed as shown in Figure 20; this gives a large degree of isolation between various elements.

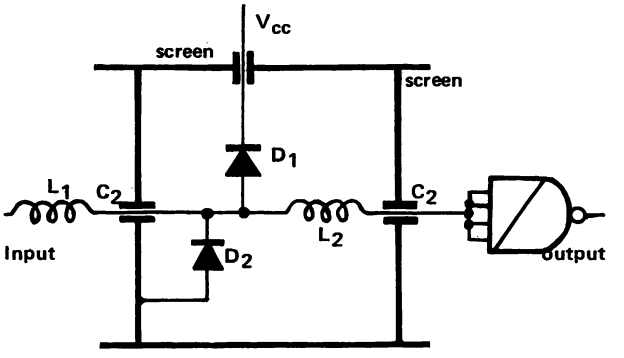


Figure 20

3.6. CR Multivibrator

The circuit of Figure 21 forms the basis of a versatile wide frequency range clock pulse source.

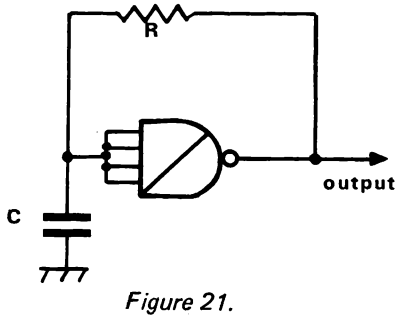


Figure 21.

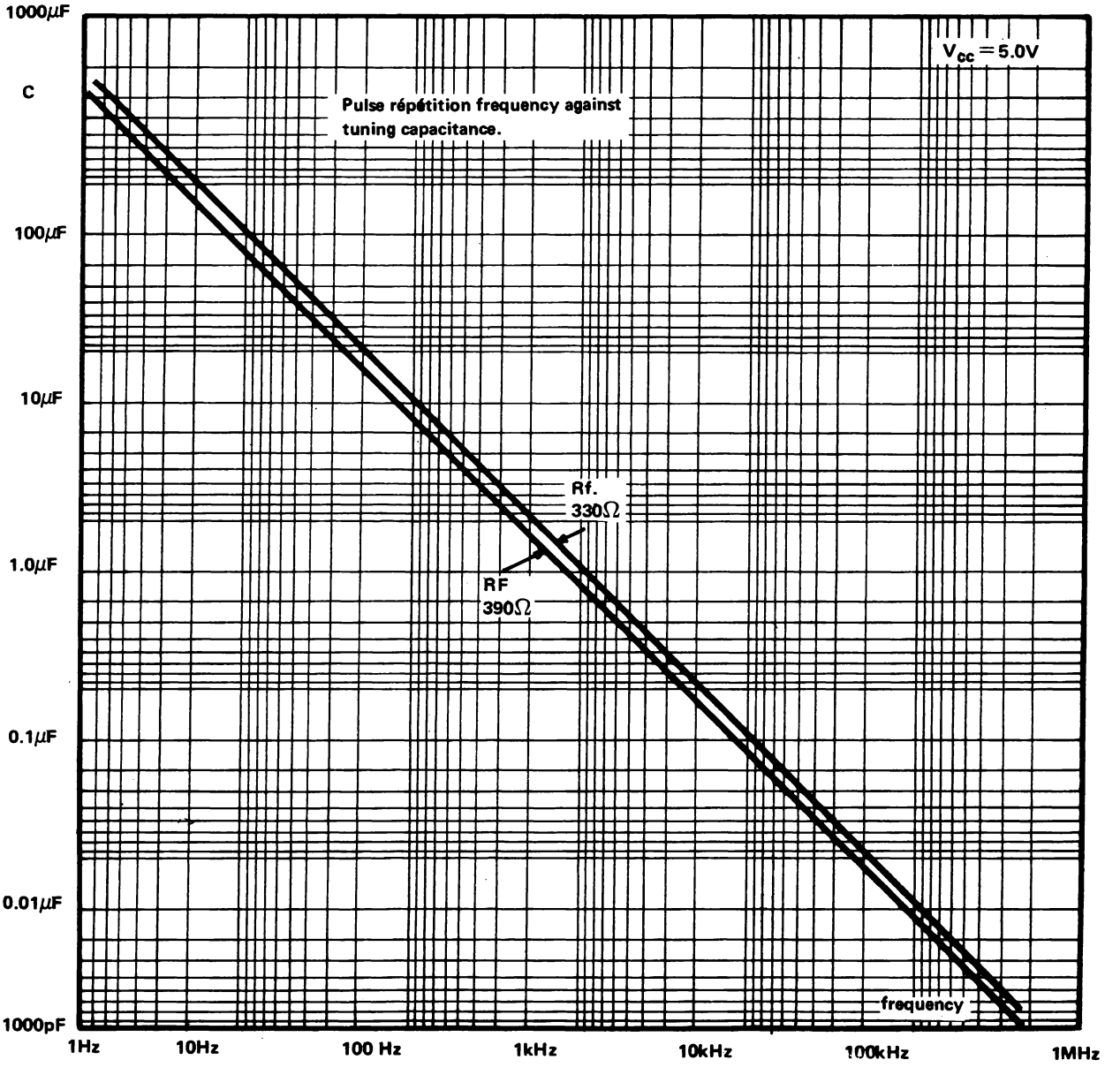
The circuit is self-starting and maintaining, a frequency range of 8 decades is possible by changing the value of capacitor C. Circuit operation is as follows. Initially capacitor C is discharged and the Schmitt output is at a logical "1". Capacitor C then charges towards (V_{CC} - V_{BE}) through resistor R until the upper threshold voltage is reached. The output then changes to a logical "O" and capacitor C discharges to the lower threshold voltage trhough resistor R. The cycle then repeats.

The limiting values of resistor R are determined by the voltage dropped across it when the input is approaching the lower threshold and the output is at a logical "O". The lower value is determined by the output impedance of the Schmitt in the logical "1" state. The output voltage should be sufficient to ensure a logical "1" at the input of succeeding stages when the input to the Schmitt is at the lower threshold voltage. The calculation of the resistors optimum value for a given load is lengthy and results of this will just be stated.

For a fan out of 2 over the full temperature range resistor R should be 390Ω.

Figure 22 is a graph of pulse repetition frequency against the value of capacitor C.

Figure 22



Typical waveforms associated with this circuit are shown in Figure 23.

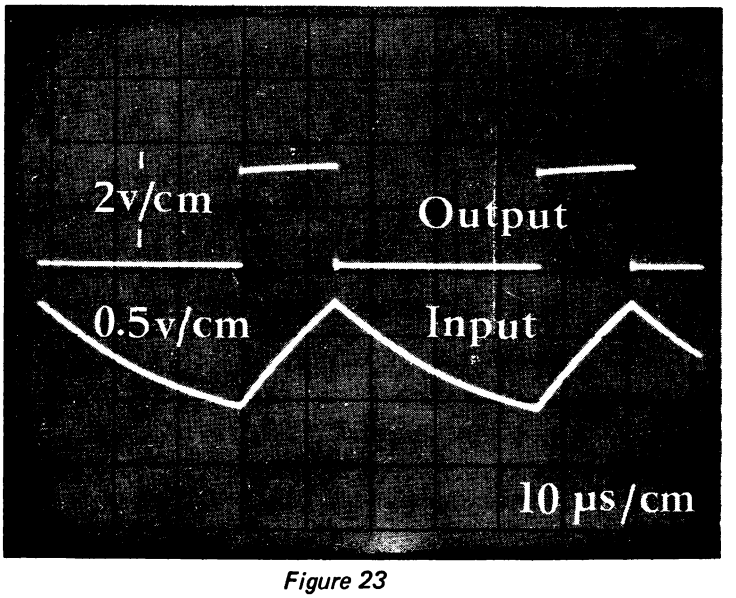


Figure 23

The mark to space ratio is not 1 : 1 due to the internal 4kΩ resistor on the base of the input multiemitter transistor acting as a current source. If a 1 : 1 mark space ratio is required the circuit may be modified as shown in Figure 24.

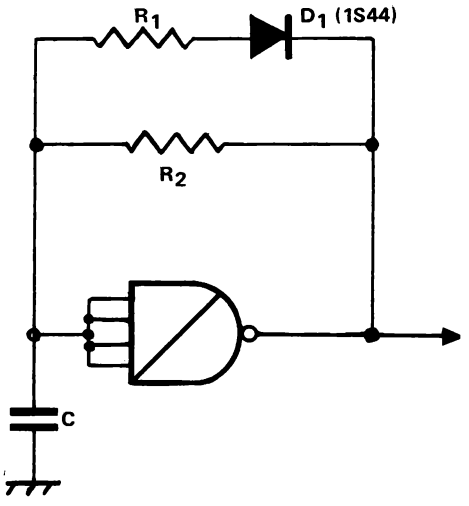


Figure 24

Here the ratio of the discharge time constant to charging time constant is reduced by approximately 1 + R1/R2 by including the additional feedback path formed by resistor R1 and diode D1 in parallel with resistor R2.

For a 1 : 1 mark/space ratio with R2 = 390Ω R1 should be 120Ω. The waveforms associated with this circuit are shown in Figure 25.

3.7. Gated Oscillator

The circuits of Figures 21 and 24 may be modified to function as gated multivibrators by the addition of an SN7401N open collector NAND gate as shown in Figure 26.

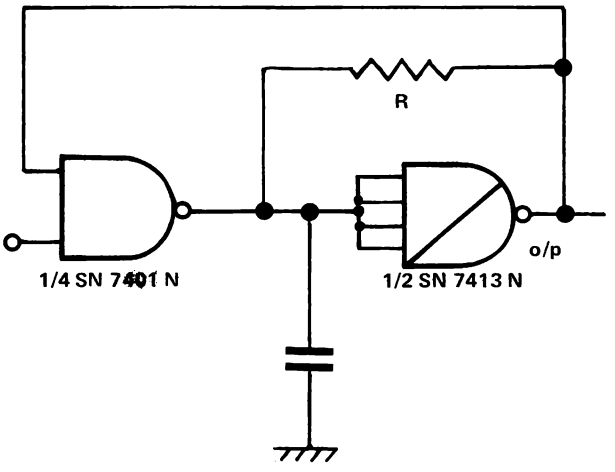


Figure 26.

An additional feedback path from the output of the Schmitt to the input of the SN7401N prevents the gate signal from acting until the output of the SN7413N is at a logical "1". This ensures that the oscillator always produces an integral number of cycles.

Since the capacitor C has to charge from ground potential to the upper Schmitt threshold before an output is produced, there is a delay between the positive going edge of the start pulse and the beginning of the output pulse train. Figure 27 is a graph giving this time delay against value of capacitor C for R = 390Ω.

Typical operating waveforms associated with this circuit are shown in Figure 28.

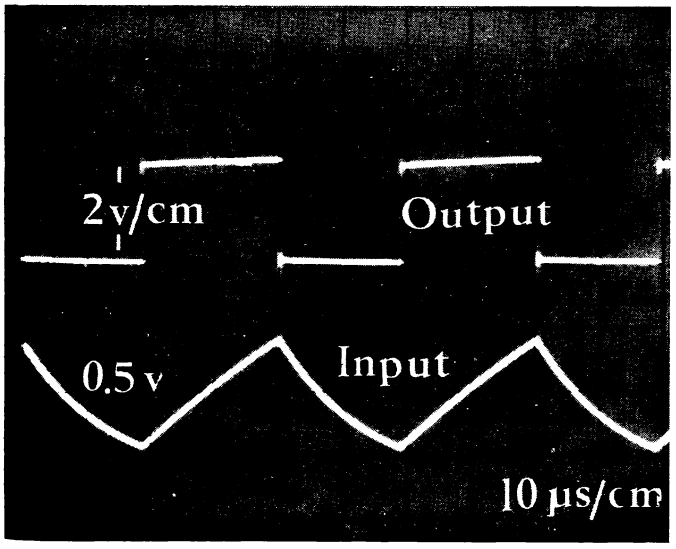


Figure 25

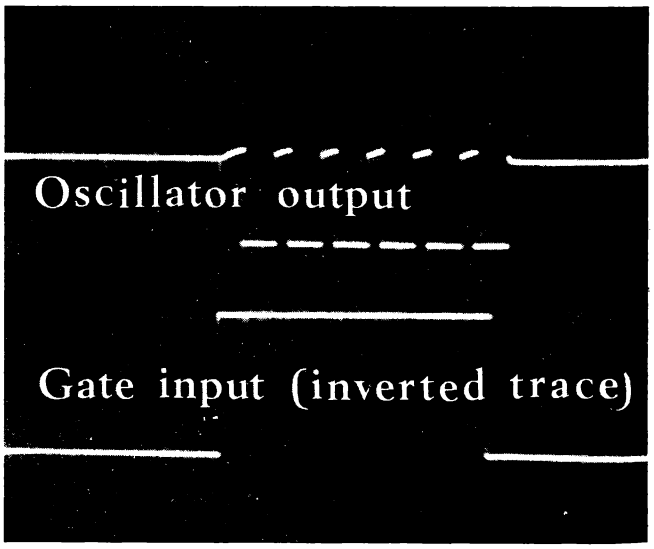


Figure 28

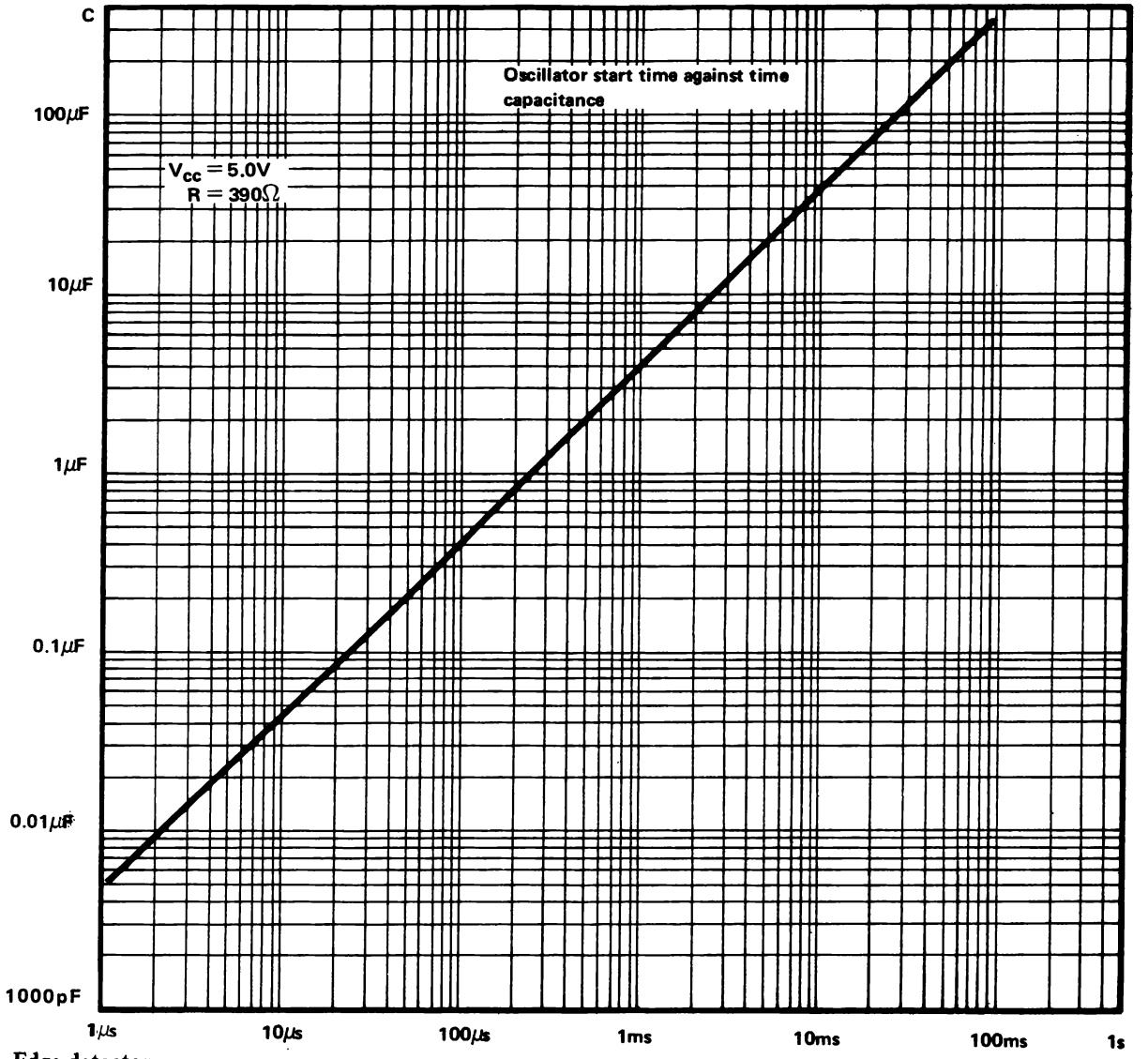


Figure 27

3.8. Edge detector

A useful digital circuit is the edge detector or pulse differentiator. The SN7413N can perform this function with a minimum of external components. The circuit shown in Figure 29 has been, in the past, implemented with standard TTL but suffered from poor noise immunity and high frequency instability.

Figure 30 shows the operating waveforms associated with the circuit of Figure 29.

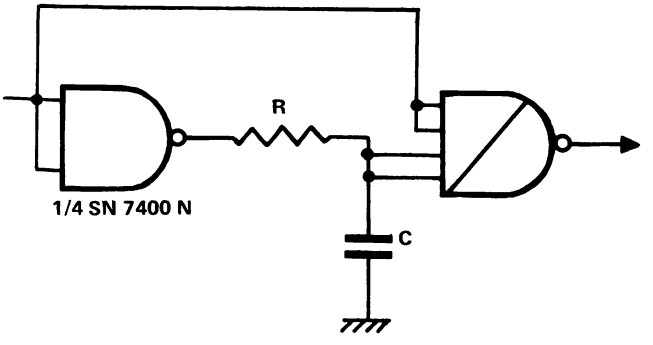


Figure 29

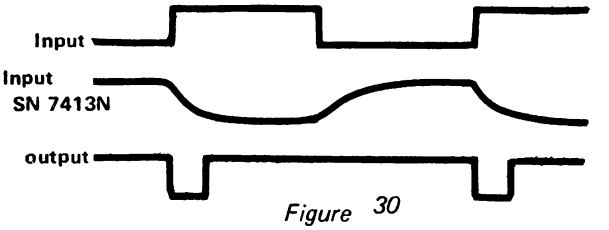


Figure 30

Figure 31 indicates the range of pulse widths obtainable with this circuit.

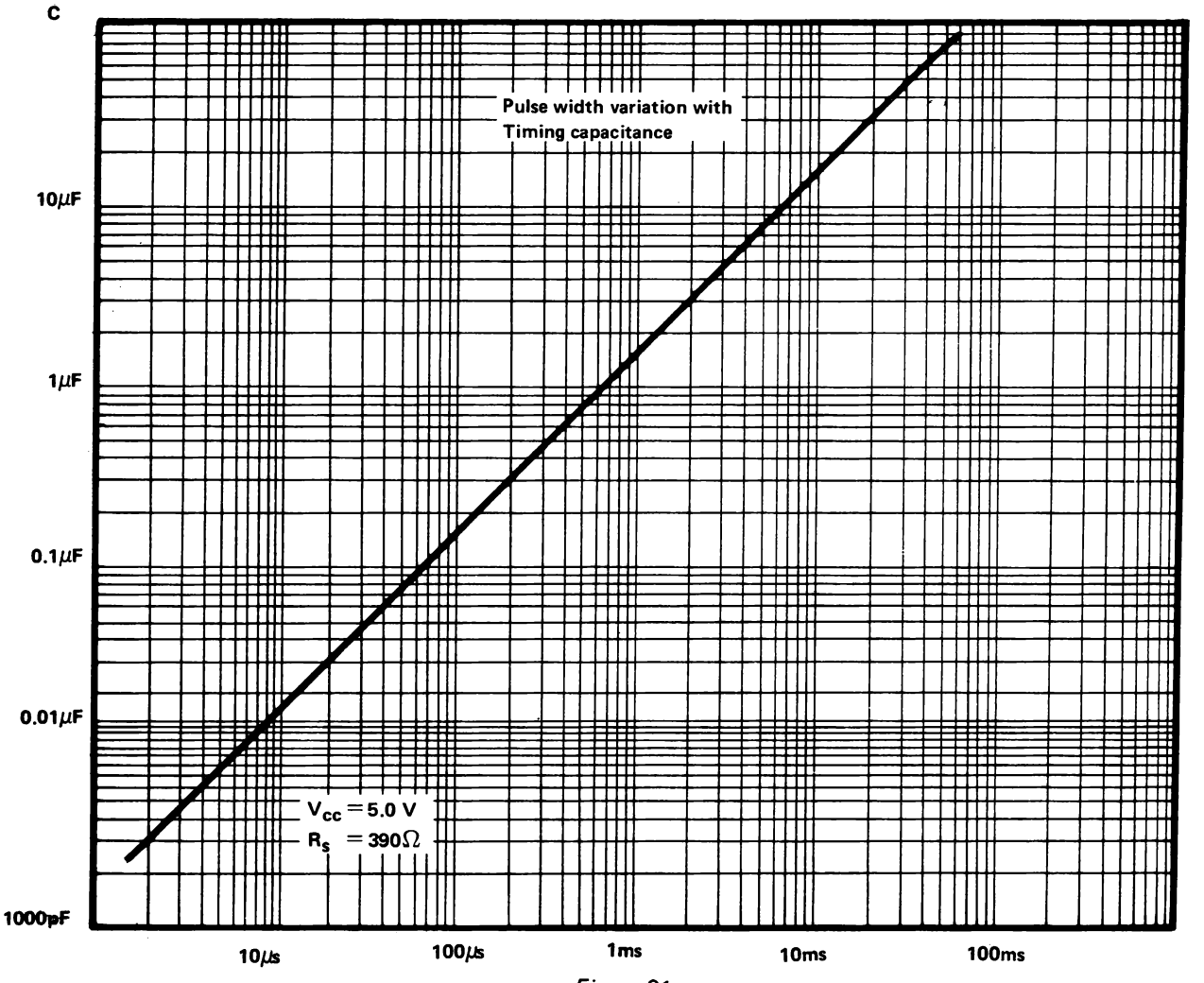


Figure 31

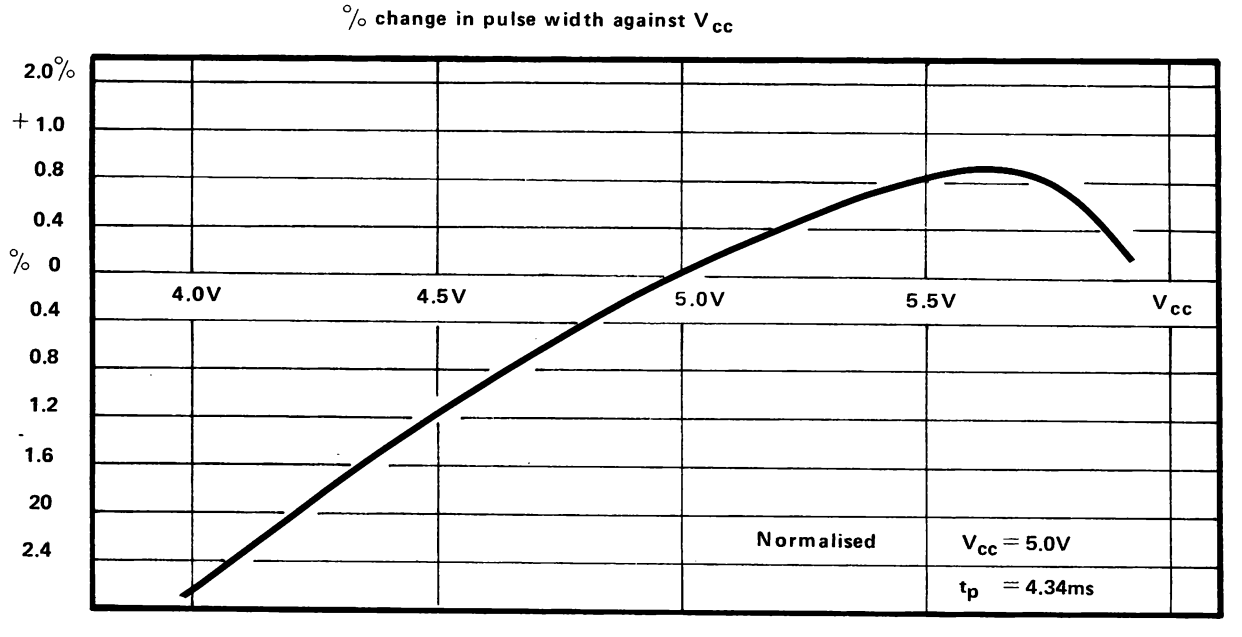


Figure 32

Figure 32 shows the percentage change in pulse width against supply voltage V_{CC}. A simple circuit, but of lower noise immunity is shown in Figure 33.

This circuit operates on a logical "1" to "0" transition.

The input Schmitt is biassed at the upper threshold voltage by resistor R. The input current at the upper threshold is $\triangleq$ 0.5mA giving a minimum value of resistor R = 4.3kΩ for an upper threshold voltage of 1.7V. Operating waveforms are shown in Figure 34.

The multiemitter inputs of the Schmitt should be strapped together in order to prevent emitter to emitter breakdown since the input can rise above V_{CC}.

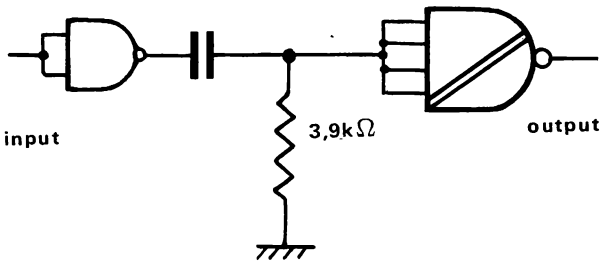


Figure 33

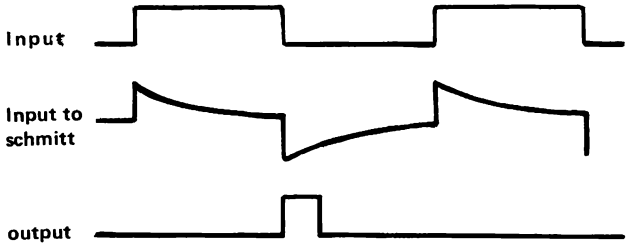


Figure 34

Use of TTL IC in Industrial Noise Environments (B 90)

USE OF TTL INTEGRATED CIRCUITS IN INDUSTRIAL NOISE ENVIRONMENTS

By Bob Parsons

INTRODUCTION

Noise in electrical systems can be a difficult and elusive problem to define. This report has been written to act as a guide to users of TTL. Noise may be loosely defined as undesired electrical signals present in any electrical system. By careful design most noise problems can be alleviated before a system is built. Similarly, by systematic investigation, problems can be removed from pre-production equipment.

Noise considerations in digital systems may be summarised as shown in Figure 1.

Each topic shown cannot be considered in isolation, but must take into consideration the influence of other factors, for example, internal noise only becomes important if it is significant compared with data levels.

INTERNAL NOISE GENERATION

High frequency signal components due to fast transition times at the outputs of logic elements are the main source of internally generated noise. These components are still present when data rates are low, demanding that high frequency techniques should be used no matter what the pulse repetition rate.

As device logic levels change, circuit currents flowing also change. These changes are due to:–

(i) Different currents required to maintain the new logic level.

(ii) Transients due to lines charging and discharging.

(iii) Conduction overlap of the transistors in a TTL output stage.

Figure 2 shows the stray circuit elements associated with these transients.

Capacitance C_S is the capacitance to ground and surroundings of the output connection from gate G1 to the input of gate G2. L_S and L_g are the self inductances of the ground and supply lines respectively.

When the gate output changes from a logical '0' to a logical '1' capacitance C_S must be charged through inductance L_S from the supply. The charging current I_S being C_S. V/t_r where V is the voltage difference between the logical '1' and '0' levels and t_r is the voltage rise time at the gate output. For standard TTL with typical rise and fall times of 7ns or less, interconnection charging currents can be greater than 8mA per output. This together with conduction overlap in the output stage indicates that care should be taken with system layout so as to minimise supply line impedance and interconnection inductance.

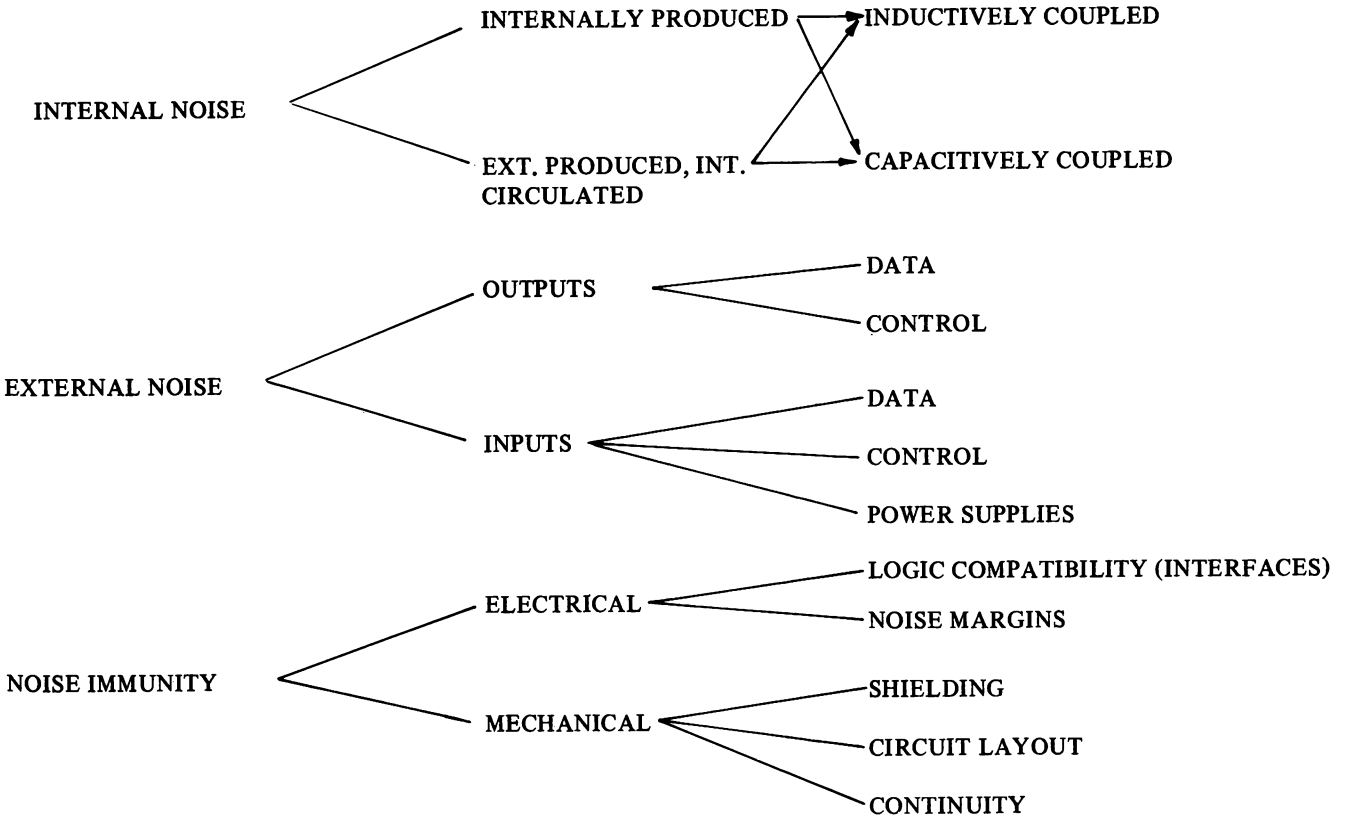


FIGURE 1

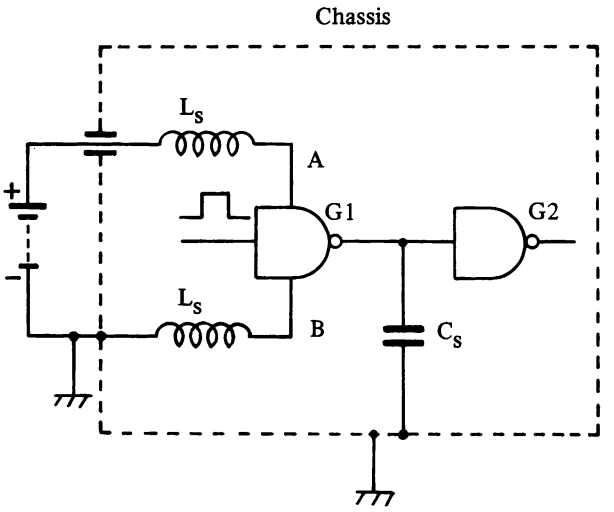


FIGURE 2

In a practical system the following steps should be taken to minimise the generation of internal noise.

(i) The power supply distribution system should be of low impedance. This can be achieved by two methods:

(a) A low impedance transmission line formed by a stripline above a ground plane – or line.

(b) Medium impedance line with decoupling to ground at regular intervals by discrete R.F capacitors, e.g. disc ceramics. Decoupling should be carried out every 8 to 10 packages. Use 0.01 µF to 0.1 µF or 200pF per totem pole output, whichever is the greater value. These should be distributed throughout the circuit,not lumped together. Both ends of a long ground bus-bar should be returned to a common point.

(ii) Gates that drive lines must be decoupled at the package. The decoupling capacitor and transmission line ground should be commoned as near to the driving device ground as is practical.

(iii) Power gates formed by paralleling gates should utilise a single package with its decoupling capacitor.

Noise that has gained entry to equipment as well as that which is internally generated can couple into adjacent signal and power lines. This can take place through common impedances or as shown in Figure 3.

Here two lines carrying signals, or signal and noise, are in close proximity to one another. Cross coupling exists between these two lines due to mutual capacitance and inductance C_m and L_m. In order to analyse this configuration, it is convenient to consider C_m and L_m forming a mutual impedance Z_m between the two lines. If the line impedances are Z_o, the gate output impedances are Z_1, the logic swing at the output of gate G1 is V_s, and the coupled component of V_s at the input of G4 is V_{in}, then, as shown in the Appendix:

$$V_{in} = V_s/(1.5 + Z_m/Z_o)(1 + Z_1/Z_o) \quad \ldots\ldots \quad 1$$

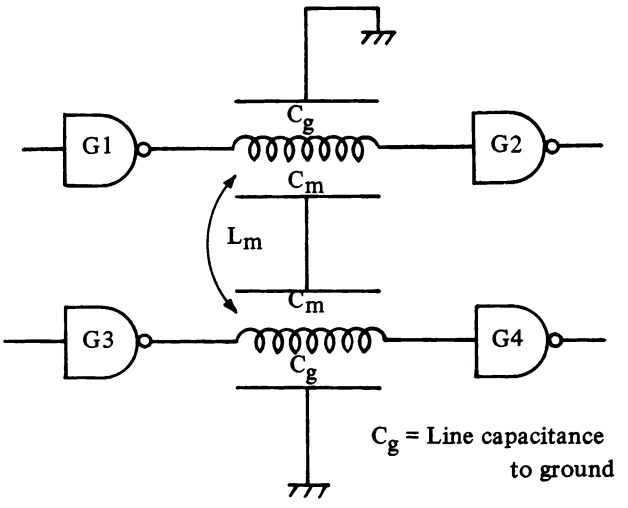


FIGURE 3

The following practical conclusions can be drawn from equation 1.

1. To minimise cross talk between two lines their mutual impedance should be as high as possible and the line impedance as low as possible.

2. Such lines should be coaxial cables with low impedances Z_o and very little external field giving a high Z_m.

In practice the line impedance cannot be too low or the logic swing at the receiving gate will be restricted and line reflections will be significant compared with logic levels.

Stripline conductors above a ground plane can have controlled impedances giving excellent crosstalk properties.

Single wires, whilst being inexpensive and convenient, have poor cross-talk and reflection characteristics limiting their usable length to 25cm or less with standard TTL.

For lines less than 5m in length twisted pairs with Z_o between 50Ω and 150Ω are satisfactory provided that the sending gate is restricted to line driving. (This is explained in more detail in the section on driving transmission lines).

EXTERNAL NOISE

In any digital system provision must be made for the transmission of input and output data and control signals between the logic system and its peripherals. The current and voltage levels chosen for transmission are generally incompatible with TTL as they are dictated by considerations such as line impedance, noise environment, contact resistance, etc.

The influence of external noise on a TTL logic system is determined mainly by the type of interface circuits used to transfer signals into the logic system. These circuits cannot be designed effectively unless the input requirements of a TTL gate are understood.

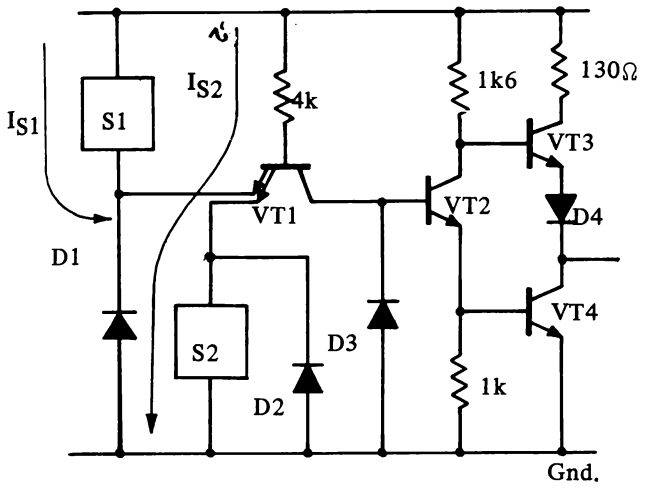


FIGURE 4

Figure 4 shows the circuit diagram of a standard TTL gate, where I_{S1} is the current to be 'sourced' and I_{S2} to be 'sunk' by the driver circuits S1 and S2.

Transistor VT1 is a multiemitter transistor with a 4kΩ base resistor to the supply voltage V_{CC}. If any input emitter is grounded base current flows out of the grounded emitter saturating transistor VT1 and turning 'off' transistor VT2 allowing its collector to rise towards V_{CC}. The output of emitter follower transistor VT3 is, therefore, a logical '1'. If all input emitters of VT1 are high, i.e. logical '1', then its base collector diode is forward biassed and transistors VT2 and VT4 are saturated. The collector of VT4 is therefore at $V_{CE(sat)}$, i.e. logical '0'. Since the input transistor is now operating in an inverse mode with the collector base diode forward biassed, an inverse emitter current, dependent upon inverse gain and base current, must flow into each emitter. The input voltage at which VT1 changes from normal to inverse mode of operation, i.e. the gate threshold voltage, is determined by its collector potential. This is defined by the V_{BE}s of VT2 and VT4, giving a typical threshold of 1.4V.

A typical transfer characteristic of the circuit of Figure 4 is shown in Figure 5.

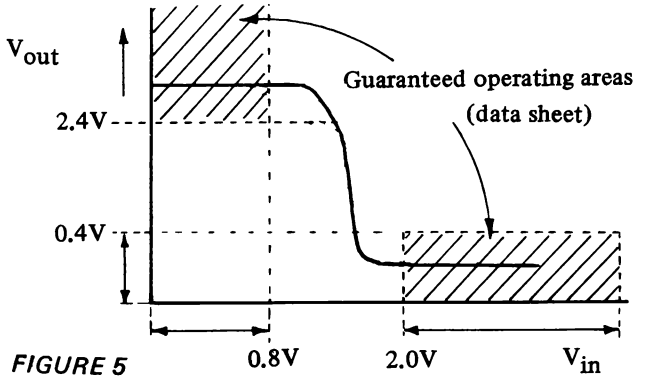


FIGURE 5

To obtain maximum noise immunity logical '0' and '1' input levels should be far removed from the gate threshold. This means that any interface circuit must be able to sink the base current of VT1 when in the logical '0' state and source the inverse emitter current when in the logical '1' state in order to maintain maximum noise immunity.

Interface Circuits

An interface circuit must perform the following operations:-

(i) Transform input logic levels to those of TTL. This must be achieved without loss of noise margin.

(ii) Filter out unwanted noise whose frequency components lie outside the signal frequency range. Noise that occurs within the signal frequency spectrum, i.e. comparable with data bit rate, can only be removed by logical means.

(iii) The interface circuit must take into consideration the transfer characteristics of the circuit that it is driving. The basic TTL gate is a saturating amplifier with a range of input voltages around its threshold where the gate will act as a high gain (> 55dB power gain at 10MHz.) high frequency linear amplifier.

The rise and fall times of data edges into TTL required for oscillation-free switching, are dependent upon a number of factors. These include the driving source impedance, gate loading, layout and supply decoupling. In practice, interface circuits should have rise and fall times (10 – 90%) <50ns between logical '0' and '1' levels.

Further problems arise if waveforms with slow edges are used to clock bistables such as the SN7474 dual D type. The clock noise immunity is degraded and the data hold time has to be increased to ensure correct data transfer.

Interface Filters

Suitable interface circuits consist of a low pass filter followed by an impedance converter. The low pass filter can be single or multiple section CR or LC. The impedance converter has to satisfy the conditions outlined above. An ideal converter is the SN7413N Schmitt trigger. Logically this device performs the same logic function as the SN7420 dual 4 input NAND gate but the upper and lower input thresholds are 1.7V and 0.9V typically.

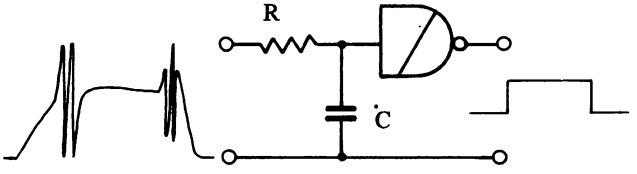


FIGURE 6

The filter shown in Figure 6 is all that is needed, in the majority of cases, to eliminate noise associated with input signals. To maintain noise immunity at the Schmitt input the maximum value of resistor R should be limited to 250Ω when being driven from standard TTL.

This, therefore, determines the value of capacitor C for a given 3dB cut-off frequency, f_o, of the filter, i.e. $C = 1/2\ \pi.\ R.f_o$. The rate of attenuation past the cut-off frequency is 6dB/octave. For larger rates of attenuation and faster response times multipole Chebyshev filters can be used. Since the input to the Schmitt is always positive with respect to ground, capacitor C may be a large value electrolytic.

Low pass filter, Chebyshev

These filters should be used when digital equipment is required to operate under conditions of extreme electrical noise. The Chebyshev filter is characterised by an amplitude frequency response that ripples in the pass band and falls off rapidly past the cut-off frequency f_o. The general form of this type of filter is shown in Figure 7.

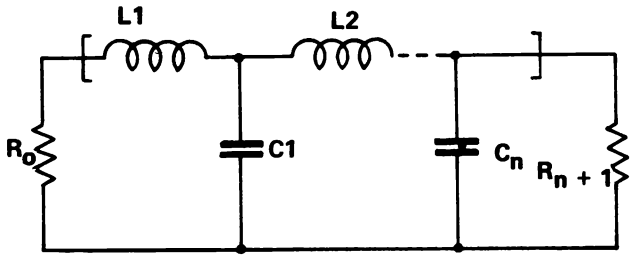


FIGURE 7

The amplitude frequency response of such a filter is shown in Figure 8.

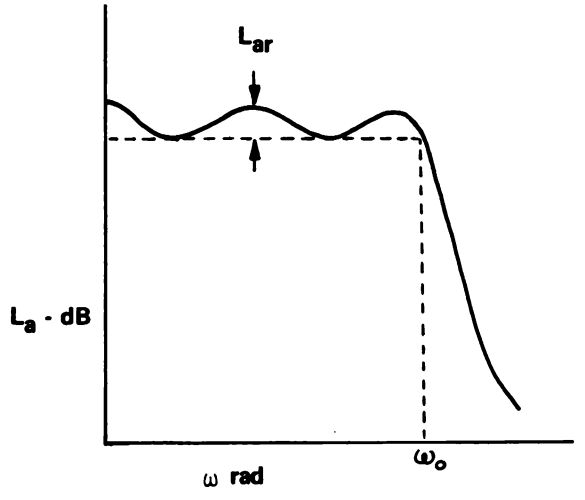


FIGURE 8

This circuit form is well suited to mechanical construction since the capacitive elements can be lead throughs. The required D.C. operating conditions for the Schmitt trigger are easily satisfied since the filter has almost zero impedance at D.C.

A compromise has to be made between the number of elements and the rate of attenuation past the cut-off frequency. In practice, a four element filter that has an attenuation of 60dB at 4 ω_o is usually satisfactory. The load impedance R_{n+1} is determined by the input impedance of the Schmitt trigger, which in turn determines the filter source impedance R_o. For this reason it is more practical to use a different filter design which will match a low source impedance to the input impedance of the Schmitt trigger (4kΩ approx.)

Such a design is shown in Figure 9 and component values are tabulated in Figure 9A for various cut-off frequencies.

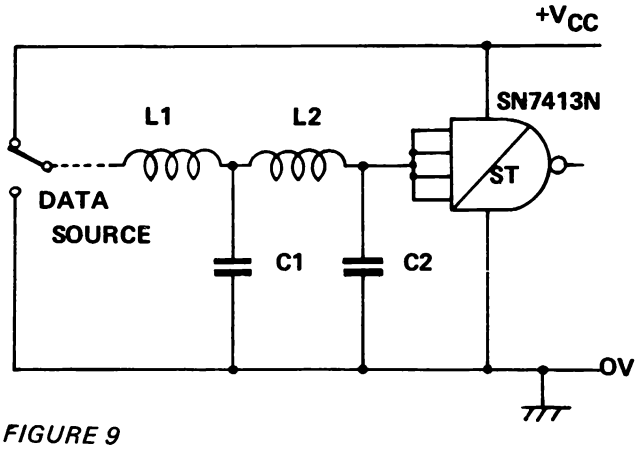


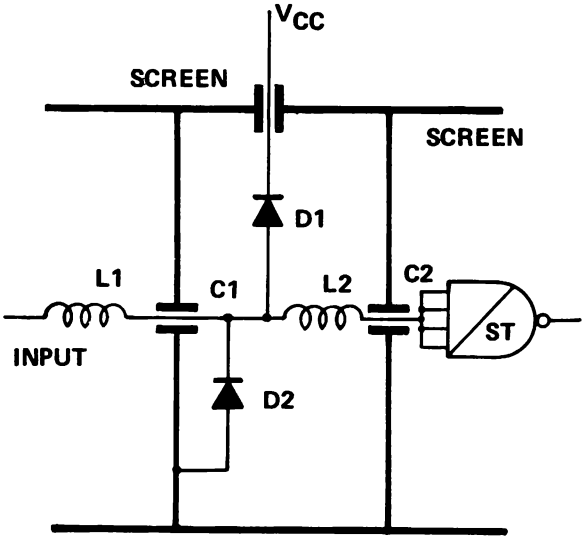
FIGURE 9

Element values for 4 element filter with L_{ar} = 1dB and L_a = −60dB at 4 ω_o.

f_o(kHz)	L1(mH)	C1(pF)	L2(mH)	C2(pF)
100	9.0	420	8.2	760
200	4.5	220	4.1	380
500	1.8	84	1.6	150
1000	0.9	42	0.8	76

FIGURE 9A

Since the inductive and capacitive components are $\propto .1/f_o$. element values for any cut off frequency f_o may be calculated from the tables given. Additional components may be added to the circuit of Figure 9 to enable it to handle very large voltage surges at the filter input as shown in Figure 10



Constructional Form

FIGURE 10

Diodes D1 and D2 limit the input swing into the Schmitt trigger. they should be situated after inductor L1 so that the rate of rise of voltage across diodes D1 and D2 is limited.

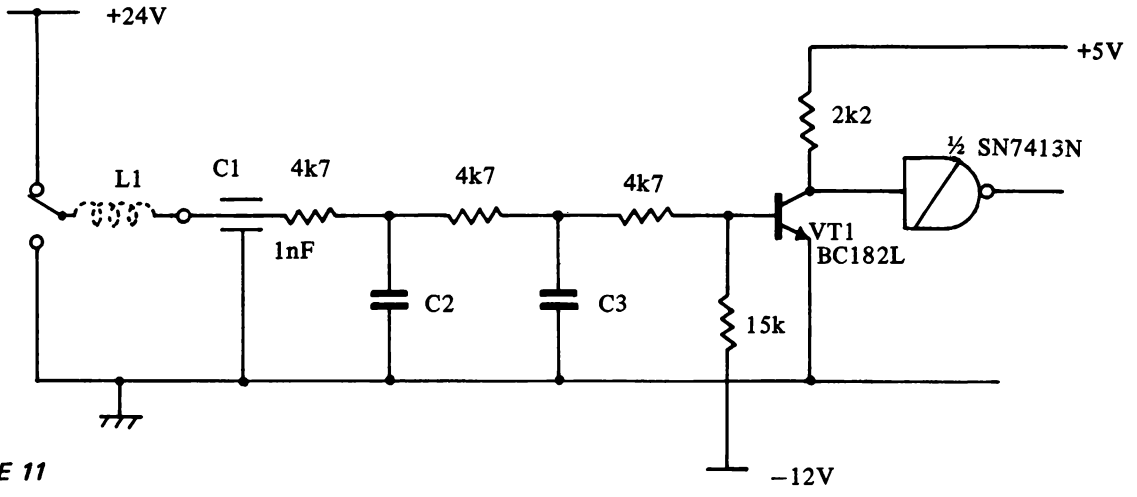


FIGURE 11

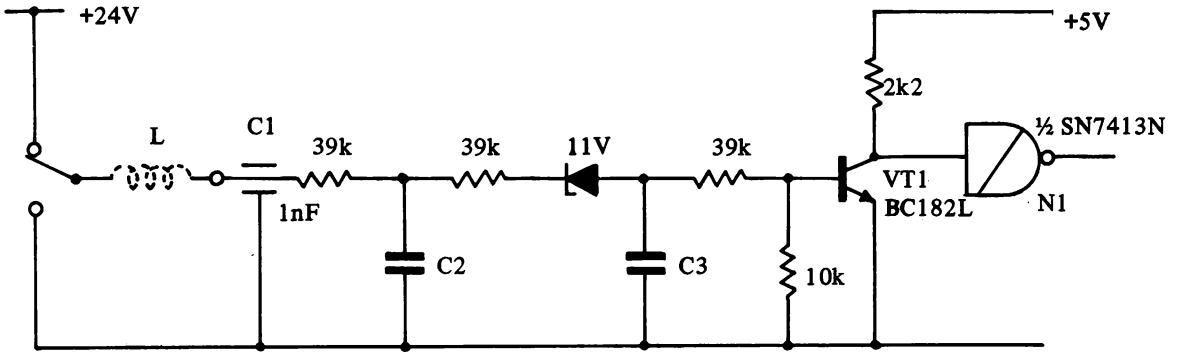


FIGURE 12

The previous filter circuits have logical threshold voltages that are the same as TTL. In many systems it is advantageous to have higher thresholds in order to overcome voltage drops down lines and contact resistance etc. Such circuits are shown in Figures 11 and 12.

Both circuits consist of CR low pass filters followed by a transistor buffer and a Schmitt trigger. Capacitor C1 is a lead through ceramic. This, together with L (lead inductance), forms a low pass filter removing high frequency components that would otherwise, due to layout, be very difficult to remove. The logic threshold for the circuit of Figure 11 is arranged to be 12V midway between the input logic levels, 0 and 24V. The values of C1, C2 and C3 should be chosen to give the required frequency response.

Both circuits have a series resistor between capacitor C3 and transistor VT1. This limits the rate of discharge of C3 through the base emitter diode of transistor VT1.

Optical Interfaces

In many industrial systems it is possible for very large transient common mode voltages to exist between equipments. In cases such as these an isolated coupler such as reed relays, transformers or optical devices must be used in order to transmit data. An alternative is to attenuate the signal and common mode offset until the common mode voltage is sufficiently low to be acceptable. The signal is then detected by a high gain differential comparator. This system does, however, have poor noise rejection unless common mode paths are carefully balanced.

An economical method giving a high degree of isolation (>1kV) and reasonable speed is the optical coupler, as shown in Figure 13.

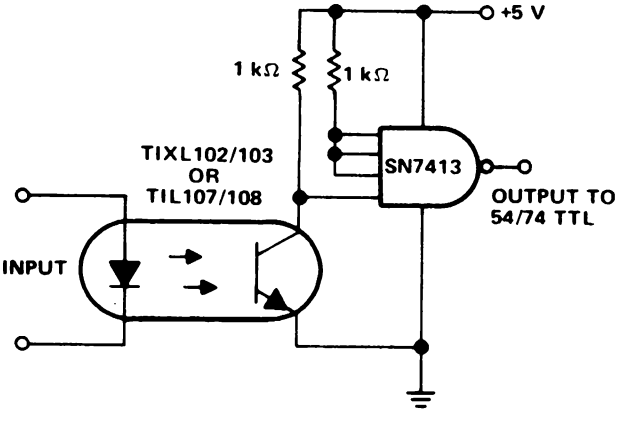


FIGURE 13

The optical isolator consists of an infrared emitter and receiver diode electrically isolated from each other, but maintained in the same package. The emitter diode forward current is in the order of 15mA to obtain a receiver current of 2mA (TIL108). A suitable buffer between the diode output and TTL input must be provided which in the simplest form would be a TTL Schmitt trigger. A maximum bit rate of approximately 60kHz can be obtained with the circuit of Figure 13. If higher bit rates are required then the TIL 107/8 should be followed by a wideband operational amplifier such as the SN7511 operated in the virtual earth mode.

DRIVING TRANSMISSION LINES

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections occur because most TTL interconnections are not terminated in their characteristic impedance. Reflections cause reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyse these reflections. Basic transmission line equations are applicable but unwieldy, since neither the gate's input nor output impedance is constant. Transmission-line characteristics of TTL interconnections can best be analysed by a simple graphic technique using Bergeron Diagrams.

Figure 15 shows a typical TTL interconnection. Open wires will usually have characteristic impedances of 150 to 200Ω depending upon the amount of capacitive coupling to ground. To evaluate a logical '1' to '0' transition, Figure 16 is used. The line $-1/Z_0$ ($Z_0 = 200\Omega$) which represents the transmission line is superimposed on the output characteristic curves. Since evaluation of a logical '1' to '0' transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logical '1' condition; this point is labeled t_s. The slope $-1/Z_0$ then proceeds towards the logical '0' output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the output 0 curve ($\simeq +0.25$ V). The transmission-line slope now becomes $+1/Z_0$ and is drawn

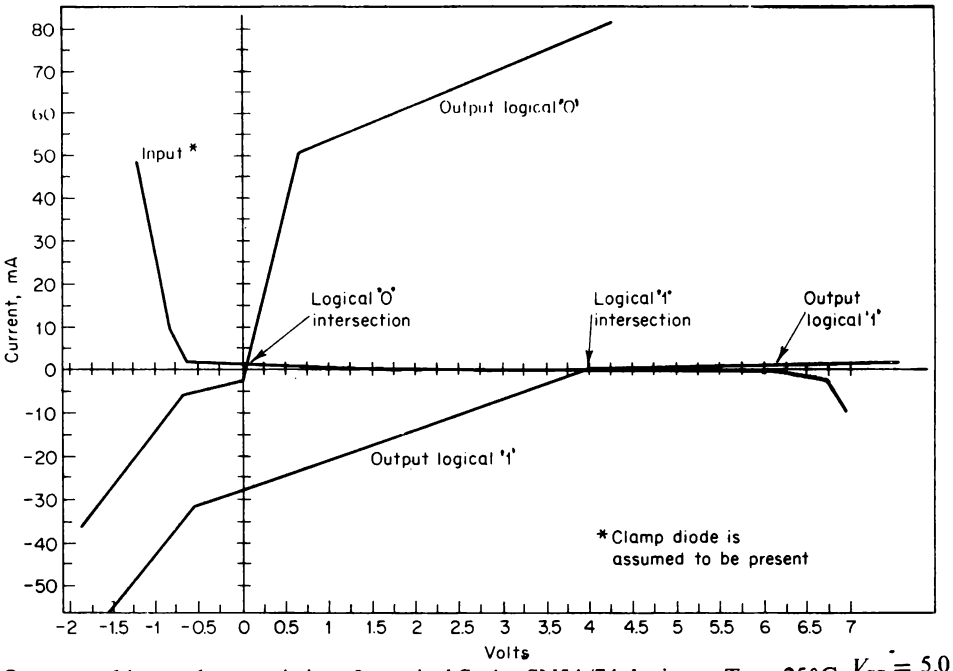


FIGURE 14 Output and input characteristics of a typical Series SN54/74 device at $T_A = 25°C$, $V_{CC} = 5.0$ V.

Figure 14 shows plots of a gate input and both (logical '0' and '1') conditions of the output for a typical SN54/74 device. The output curves are plotted in the normal way with positive slopes, but the input characteristic is inverted, since it will be at the receiving end of a transmission line. The logical '0' and '1' intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line.

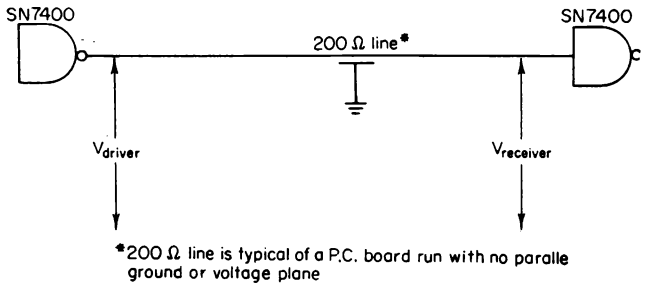

SN7400
SN7400
200 Ω line*
Vdriver
Vreceiver
*200 Ω line is typical of a P.C. board run with no parallel ground or voltage plane

FIGURE 15

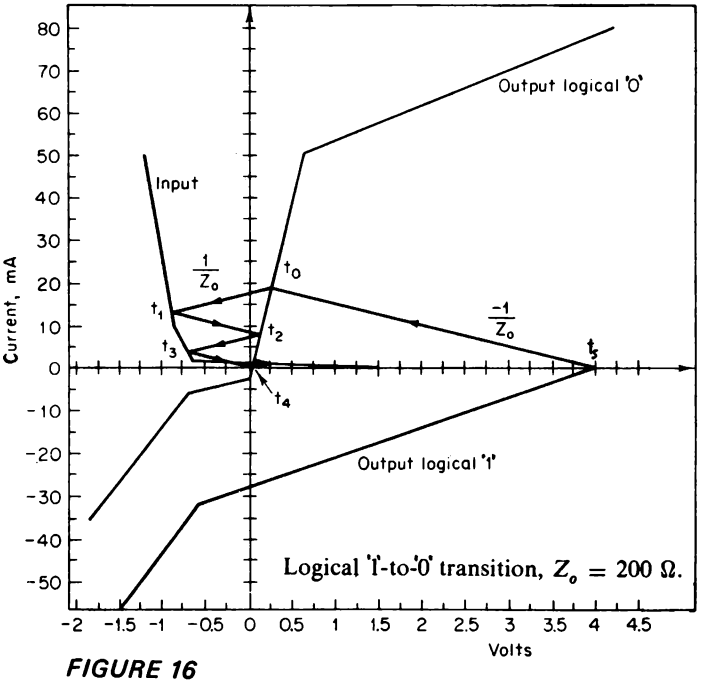
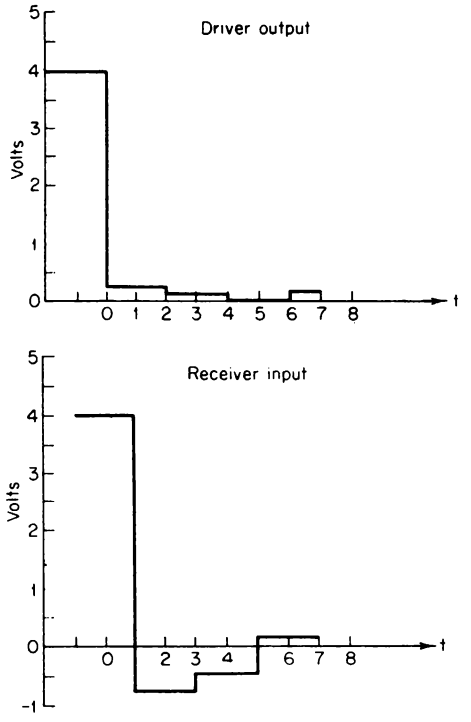


FIGURE 16

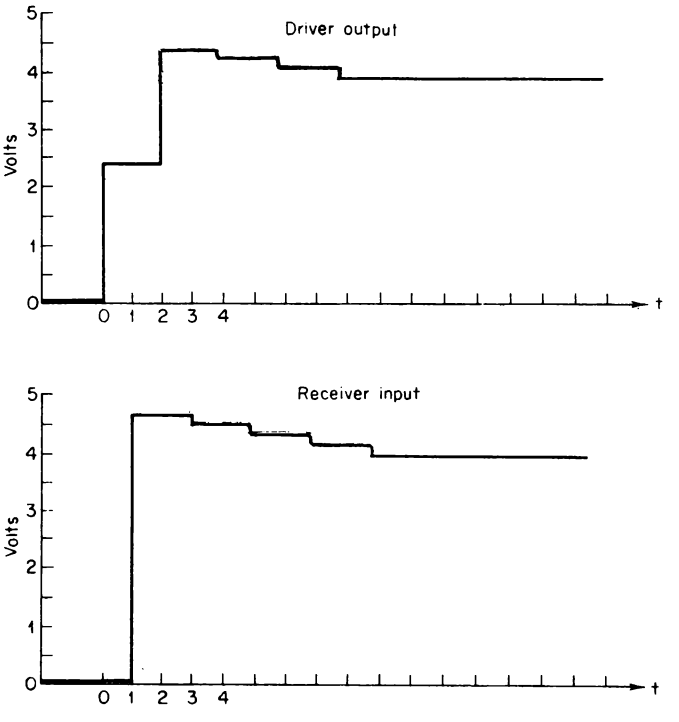
toward the input curve. At time t_1 ($t_{n+1} - t_n$ = time delay of line), the receiving gate sees −0.75V. Now the line slope changes back to $-1/Z_o$, and the graph continues until the intersection of the input and output curves for a logical '0' is approached. Figure 17 plots driver and receiver voltages versus time in this case.



Z_o = 200 Ω - logical '1'-to-'0' transition.

FIGURE 17

A logical '0' to '1' transition is treated in the same manner (Figure 18). The line $-1/Z_o$ now starts at the intersection for a logical '0', t_s. At time t_o the driver's output rises to +2.4V and at time t_1, the receiving gate's input goes to + 5.0V. Reflections then occur on the line because both ends are now terminated in a high impedance. This ringing decreases in amplitude as a steady-state condition is approached, see the insert of Figure 18. Both the output and input voltages are plotted in Figure 19 for this case.



Z_o = 200 Ω logical '0'-to-'1' transition.

FIGURE 19

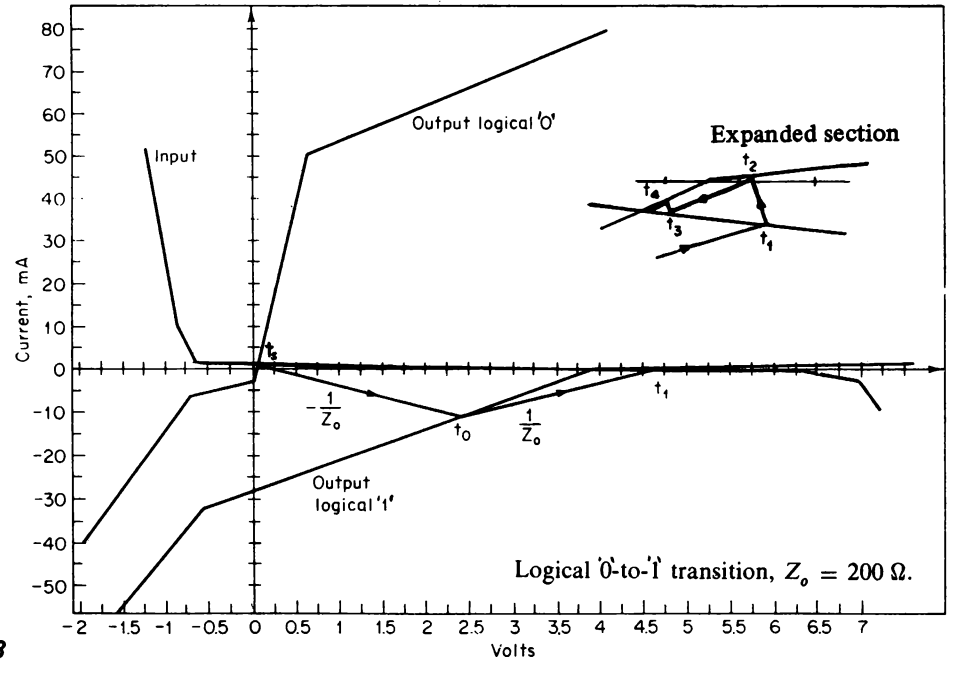


FIGURE 18

In Figures 20 to 27 a similar analysis is applied to 50Ω and 100Ω transmission lines. Notice that a decrease in line impedance does not significantly change the logical '1' to '0' transition characteristics. This is due to the low driver output impedance in the '0' state and the presence of an integral clamping diode on the input of the receiving gate.

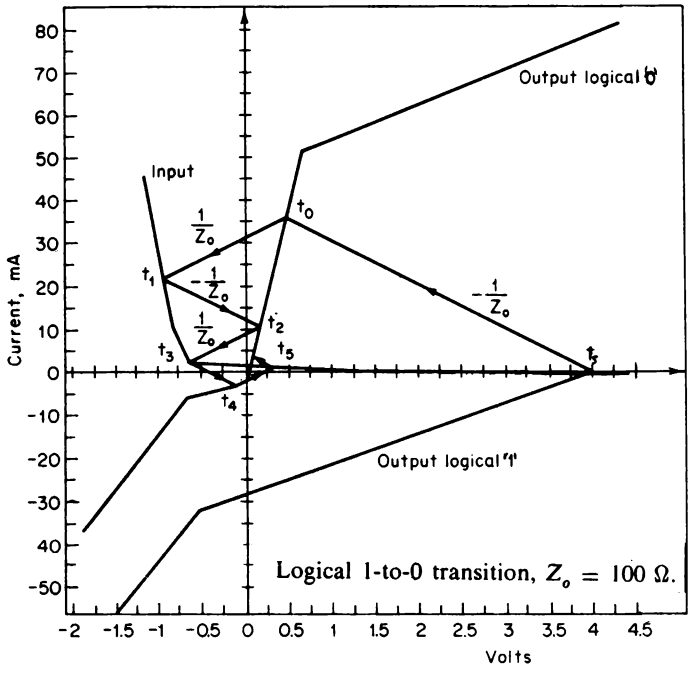


FIGURE 20

Line impedance does, however, significantly alter the '0' to '1' transition characteristics. As the line impedance increases, overshoot at the receiving end also increases. This overshoot should be limited to no more than +5.5V to avoid emitter to emitter breakdown of the receiving gate. It is advisable to connect all emitters of a receiving gate together if an overshoot > 5.5V is expected, i.e. use one receiving gate per line.

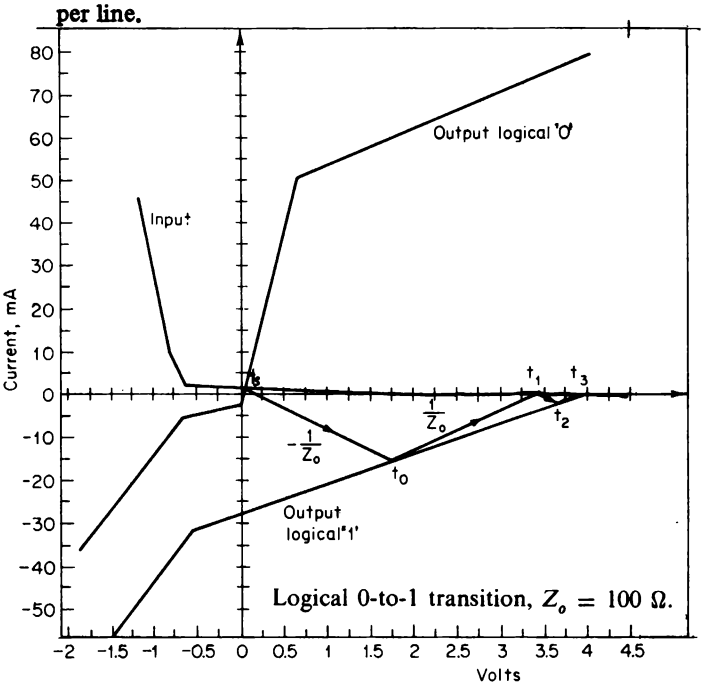
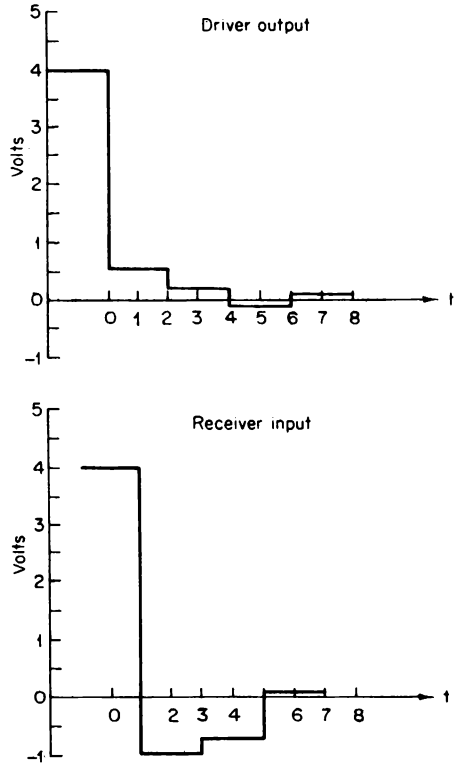
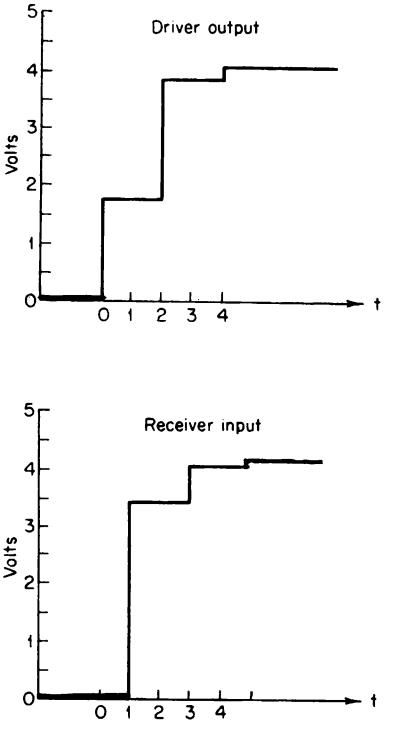


FIGURE 22



Z_o = 100Ω – logical '1' to '0' transition

FIGURE 21



Z_o = 100Ω – logical '0' to '1' transition

FIGURE 23

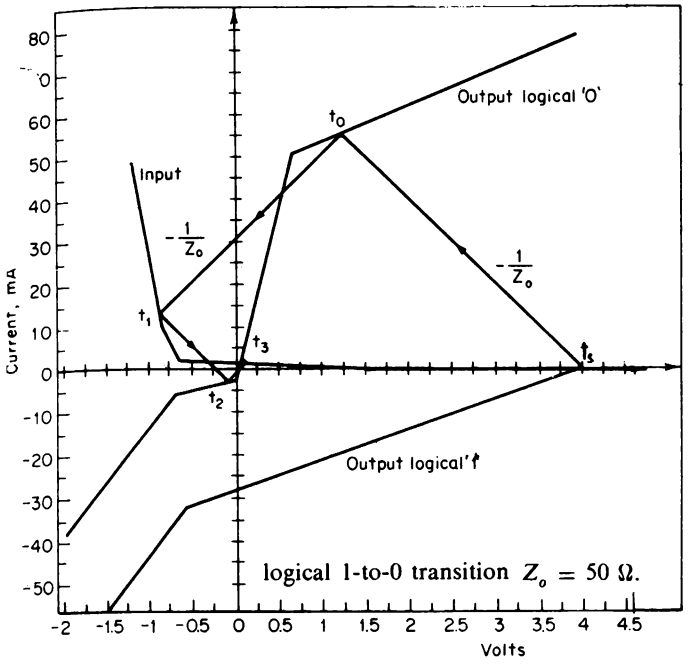


FIGURE 24

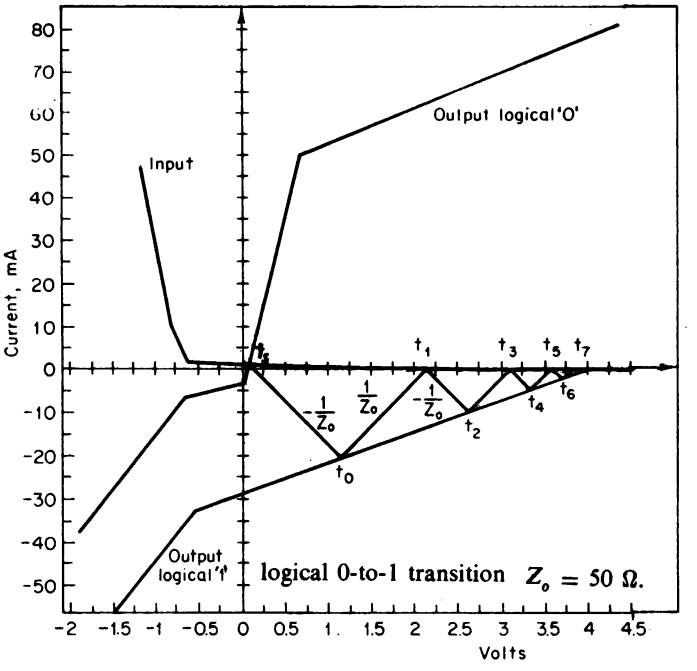
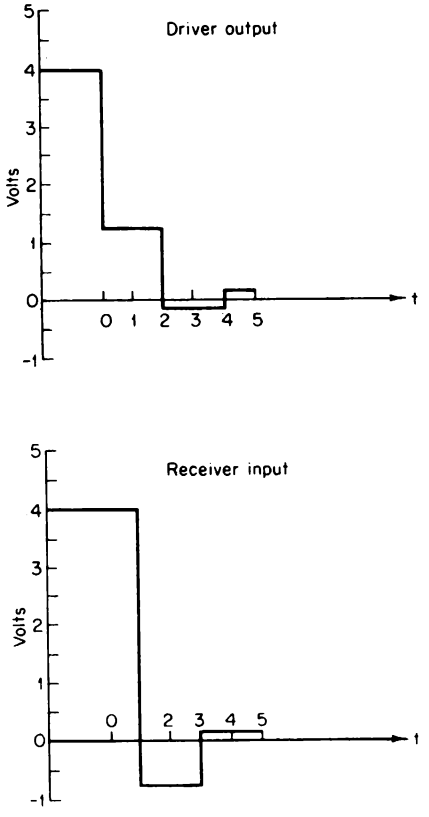
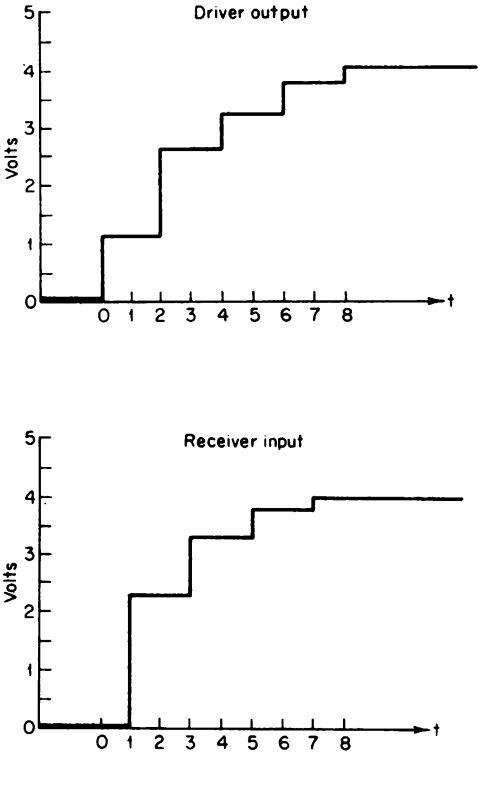


FIGURE 26



Z_o = 50Ω – logical '1' to '0' transition

FIGURE 25



Z_o = 50Ω – logical '0' to '1' transition

FIGURE 27

Low impedance lines significantly affect noise margins of gate B placed as shown in Figure 28. Note that receiver B will see only +1.25V for two times delays of the transmission line.(Figure 25). Its output can therefore not be guaranteed until time t_2, or two transmission line delays.

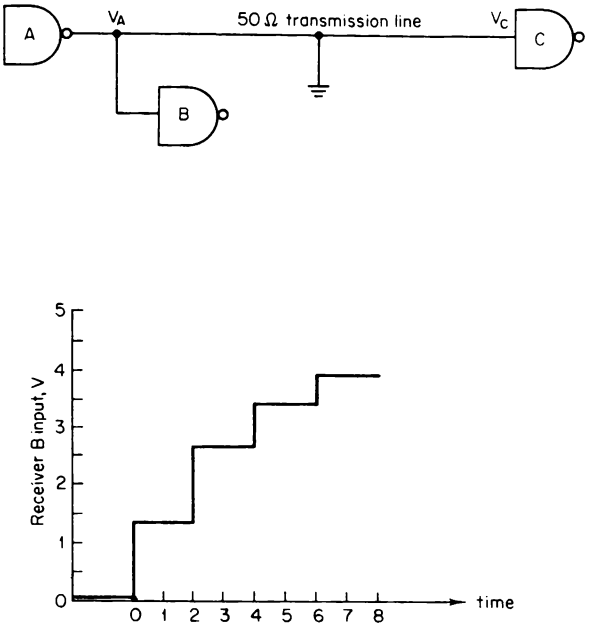


FIGURE 28

The oscilloscope photographs of Figure 29 show the effectiveness of the graphical techniques. In most cases, the calculated and experimental values of voltage steps agree very well. The ringing that appears for the open wire is not immediately obvious, but this is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for the graphical analysis, it is difficult to predict beyond the first few reflections. However this method of analysis does provide useful information. It should, of course, be remembered that the characteristics have been approximated by straight line sections. Accurate plots can be easily obtained by means of a curve tracer such as the Tektronix Type 576.

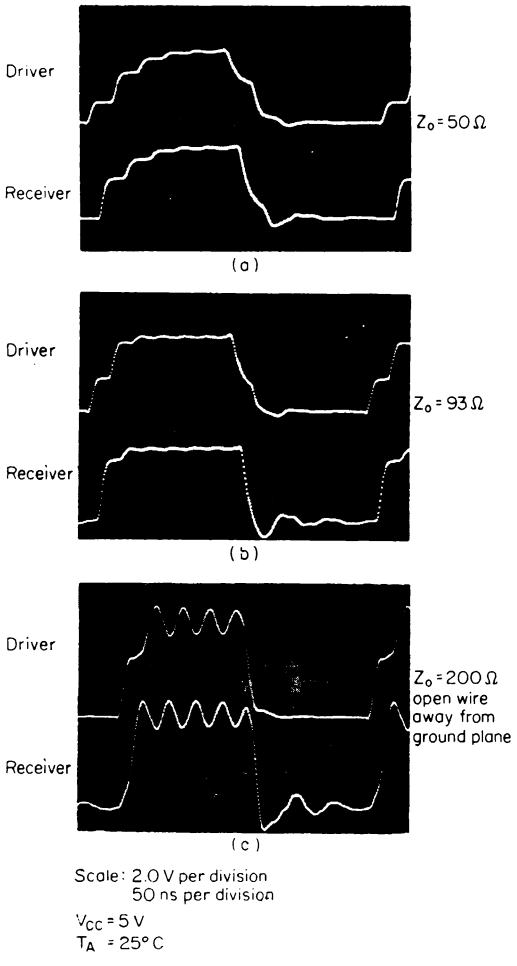


FIGURE 29

DESIGN RULE SUMMARY

The following rules have been established for the minimization of transmission-line effects in TTL systems.

1. Use direct wire interconnections that have no specific ground return for lengths up to about 10in. only. A ground plane is always desirable.

2. Direct wire interconnections must be routed close to a ground plane if longer than 10 in. and should never be longer than 20 in.

3. When using coaxial or twisted-pair cables, design around approximately 100Ω characteristic impedance. Coaxial cable of ≃ 100Ω impedance is recommended. For twisted pair. No. 26 or No. 28 S.W.G. wire with thin insulation twisted about 30 turns per foot works well. Higher impedances increase cross talk, and lower impedances are difficult to drive.

4. Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends.

5. Connect reverse termination at driver output to prevent negative overshoot.

6. Decouple line-driving and line-receiving gates as close to the package V_{CC} and ground pins as practical, with a 0.1 μF capacitor.

7. Gates used as line drivers should be used for that purpose only. Gate inputs connected directly to a line-driving output could receive erroneous inputs due to line reflections, long delay times introduced, or excessive loading on the driving gate.

8. Gates used as line receivers should have all inputs tied together to the line. Other logic inputs to the receiving gate should be avoided, and a single gate should be used as the termination of a line.

9. Any device that derives internal feedback from its outputs should not be used for line driving. Such devices are bistables, shift registers and monostables.

GENERAL RULES

Further rules have been established for general use of TTL in systems:

1. Power supply. Ripple <5% and regulation <5%. RF filter the primary supply.

2. Decouple every 5 – 10 packages with low inductance disk ceramics of value 0.01 to 0.1 μF.

3. A ground plane is desirable when the printed circuit board contains a large number of packages. If no ground plane is used the ground line should be as wide as possible and the area around the board periphery used as a distribution system.

4. Data rise and fall times into TTL devices should be <50ns except in the case of Schmitt triggers.

5. Unused inputs of ALL TTL devices should be tied to guaranteed logic levels, e.g. inputs of NAND/AND gates may be tied to V_{CC} where V_{CC} is guaranteed to ALWAYS be <5.5V. Otherwise tie to V_{CC} through a series resistor, several inputs may share a common resistor.

6. Increased fan out can be obtained by paralleling devices in the same package.

7. Gate expanders should lie as close as possible to the gate being expanded. This avoids capacitive loading and noise pick-up.

8. Input data to master slave JK flip flops should not be changed when the clock is high.

APPENDIX

Deviation of Crosstalk between lines

Gates 1 and 3 have output impedances Z_1. For simplicity, consider the inputs of gates 2 and 4 to be open circuits. The lines, whose transition times are longer than the rise time of the pulse edges, both have a characteristic impedance Z_o, and a mutual coupling impedance Z_m, as in Figure 30. Let the logic swing be V_s.

Now consider Figure 31. The swing V_s produces a step V_L which travels down the line. It is coupled by the impedance Z_m into the other line. The voltage induced travels to the gate input where, on being reflected by the open circuit, it is doubled. Therefore, the voltage at the gate $V_{in} = 2V_1$.

$$V_1 = (V_L.Z_o/2)/(Z_m + Z_o.3/2) \quad V_L = V_s.Z_o/(Z_1 + Z_o)$$

Therefore:–

$$V_{in}/V_s = 1/(1.5 + Z_m/Z_o).(1 + Z_1/Z_o)$$

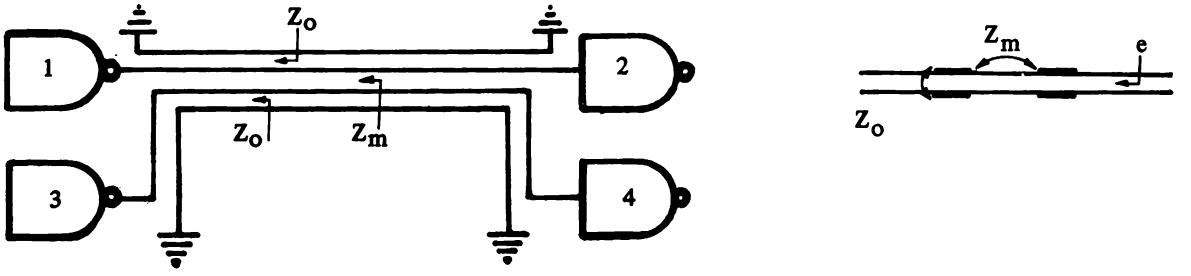


FIGURE 30

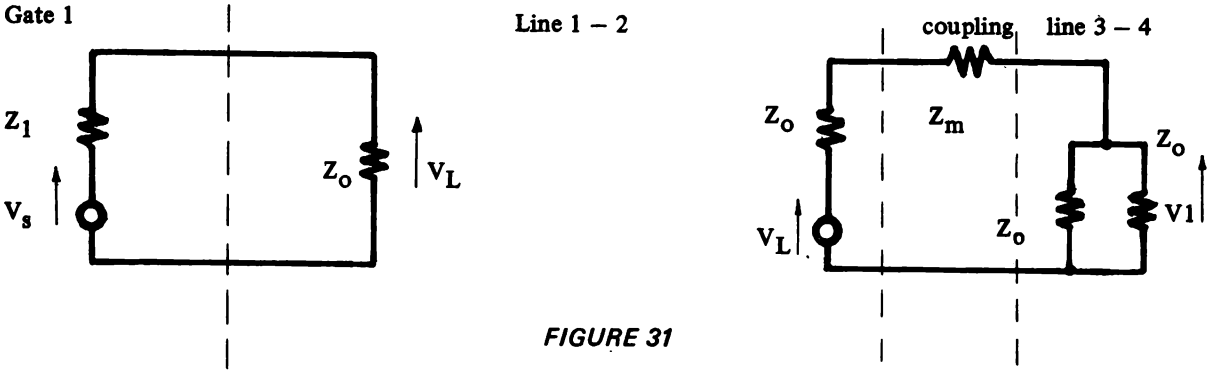


FIGURE 31

Decoder / Demultiplexer
SN 54/74154
(CA 143)

SN54/74154 DECODER/DEMULTIPLEXER

Arden Douce
Applications/Design Department

This application report discusses internal logic design and performance capabilities of the Texas Instruments SN54/74154 Decoder/Demultiplexer. The SN54/74154 MSI device is a 4-line to 16-line Decoder or 1-line to 16-line Demultiplexer with Series 54/74 TTL characteristics. A 24-pin device, it has four inputs which are decoded internally to address one of sixteen outputs. Enable and Data inputs permit input data to be transferred to the addressed output upon application of an enable signal. Use of this device leads to increased reliability due to reduction in package count, number of interconnections and wiring complexity.

Applications of the SN54/74154 as a decoder, minterm generator, code decoder and demultiplexer are also discussed.

DEVICE CHARACTERISTICS

Logic Description

A block diagram of the SN54/74154 is shown in Figure 1. Figure 2 is a SN54/74154 logic diagram. In Figure 2, four binary-coded address inputs A, B, C, and D are decoded internally to address only one of sixteen mutually exclusive outputs. Outputs with decimal names 0, 1, 2, ..., 15 correspond to the binary-weighted input code at the address inputs for $A = 2^0$, $B = 2^1$, $C = 2^2$, and $D = 2^3$. For example, if A = D = 1 and B = C = 0, gate 9 is addressed.

From the truth table, Figure 3, it can be seen that all 16 outputs will be at logical "1" unless both Enable and Data inputs are at logical "0". When Enable and Data inputs are 0, the SN54/74154 operates as a mutually exclusive sixteen-line NAND-gate decoder of the four input address lines. The addressed output gate will be at logical "0" while all other outputs are at logical "1".

The SN54/74154 can be used as a one-line to sixteen-line demultiplexer by setting Enable = 0 and connecting binary information to the Data input. This information at the Data input will be routed unchanged to the output selected by the address inputs. For example, if A = D = 1, B = C = 0 and Enable = 0, then Output 9 = Data. All other outputs are logical "1".

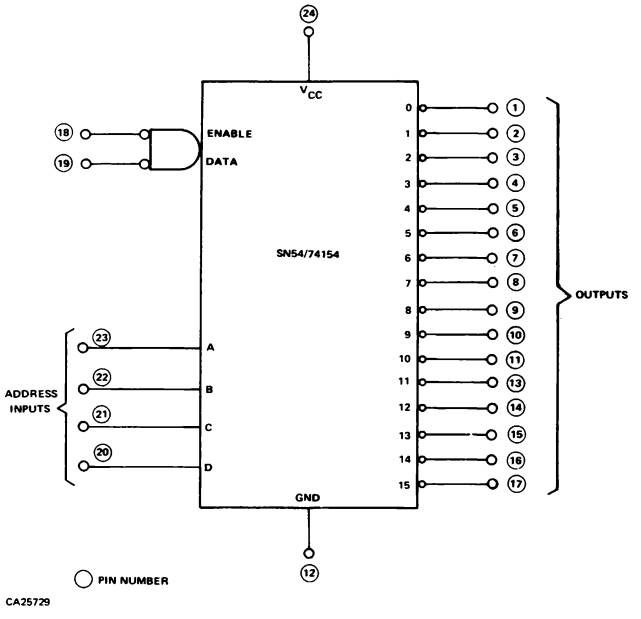


FIGURE 1. Block Diagram of SN54/74154

If Enable = 1 when the address inputs are changed, the possibility of decoding spikes and/or more than one output being momentarily logical "0" is eliminated. Since the *internal strobe* line (See Figure 2) is logical "0", address data is locked out causing all outputs to be logical "1". After switching transients have subsided, the Enable input can be returned to logical "0" to return control to the address inputs and the Data input.

Due to the symmetry of the positive AND gate with inverted inputs (positive NOR gate) used, Enable and Data functions are interchangeable. The names *Enable* and *Data* given these functions are arbitrary. Likewise, the four address inputs may be interchanged and the SN74154 will still produce the correct output when the output pins are relabelled. This may be convenient for printed circuit board layouts.

DC Characteristics

The SN54/74154 MSI device consists of several interconnected SN54/74 type gates and has Series 54/74 input and output characteristics. Each address input (A,B, C,D) as well as, the Enable and Data inputs are buffered to

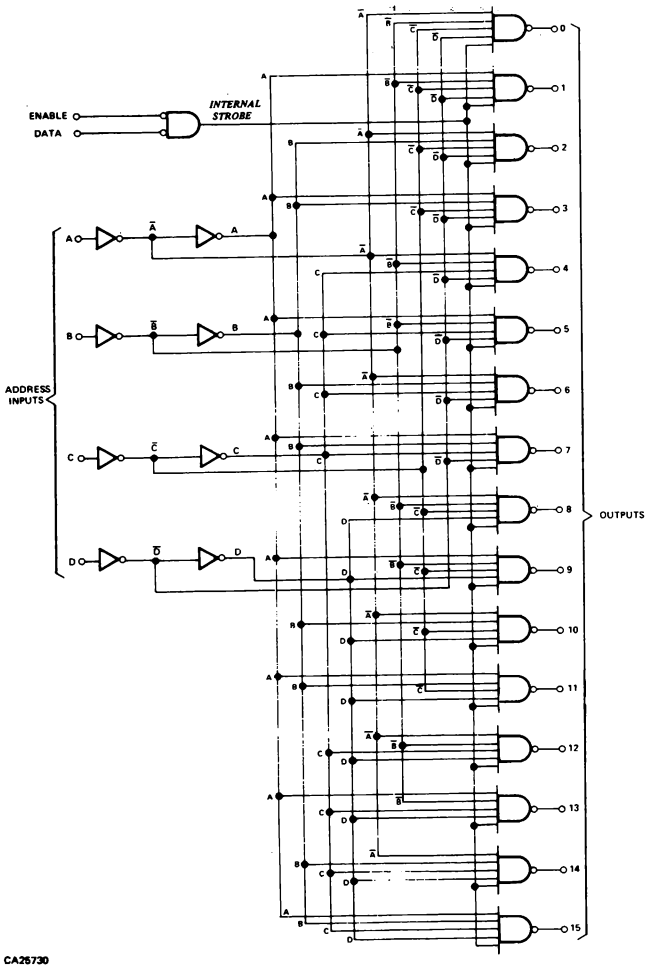


FIGURE 2. Logic Diagram of SN54/74154

INPUTS						OUTPUTS														
Enable	Data	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

X = Logical "1" or Logical "0"

CA25731

FIGURE 3. Truth Table For SN54/74154

present one normalized (N=1) TTL load to a driving gate. (See Figure 2). One normalized input load has the following characteristics:

$$I_{in(0)} \geq -1.6 \text{ mA at Vin} = 0.4 \text{ V}$$

$$I_{in(1)} \leq 40\ \mu\text{A at Vin} = 2.4 \text{ V}$$

The maximum fan-out available from each of the 16 outputs is 10 normalized SN54/74 loads in the logical "0" state and 20 SN54/74 loads in the logical "1" state. Thus, up to 20 inputs can be connected to any SN54/74154 output if the effective logical "0" load is limited to 10 or less.

Limiting is generally accomplished by logical "0" load sharing; that is, more than one input sharing a common load in the logical "0" state. For example, consider an SN7400 two-input NAND gate with both inputs tied together. The circuit input presents a load of one in the logical "0" state and a load of two in the logical "1" (the logical "0" current of −1.6 mA is shared by the two gate inputs). Ten of these configurations can be tied to any output of an SN54/74154.

These circuits are compatible with other TTL and DTL circuits. Power supply requirements are $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ for the SN54154 and $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ for the SN74154.

An SN54154 can be operated over the full military temperature range of −55°C to 125°C; whereas, the SN74154 can be operated from 0°C to 70°C. Maximum power dissipation is 269 mW for the SN54174 and 294 mW for the SN74154. Both devices typically dissipate 170 mW. An output should not be short circuited to V_{CC} or more than one output short circuited to GND at any time because excessive power dissipation may occur.

Input clamping diodes are provided at all inputs to minimize transmission line effects. An input may go negative if the current is limited to −10 mA steady state. In fact, −30 mA is permissible for short periods of time.

To minimize effects of noise pickup, unused inputs should not be left floating. Unused inputs should be connected to a voltage between 2.4 V and 5.5 V to obtain a logical "1" voltage level. If there is a possibility of exceeding 5.5 V, current must be limited such that peak power at the input junction does not exceed 5.5 mW. One method to avoid the floating input problem is to GND the unused input and rearrange the outputs of the decoder.

Switching Characteristics

Propagation delay times between input and the appropriate output at data sheet test conditions are tabulated in Figure 4. The maximum propagation delay time through the device is 37 ns (25 ns typical) for an output going to logical "1". For an output going to logical "0", the maximum propagation delay time is 33 ns (22 ns typical).

If the Enable input is not used and the address inputs do not change simultaneously ($T_{skew} \neq 0$), logical "0"

decoding spikes may occur. For instance, Figure 5(a) illustrates a spike occurring at output 3 as the inputs switch from A = 1, B = 0 (output 1) to A = 0, B = 1 (output 2). Skewing of these edges causes A = 1, B = 1 (output 3) to be decoded momentarily. It was determined experimentally when T_{skew} is 5 ns or less, no logical "0" spikes occur on an SN54/74154 output. Figure 5 defines T_{skew}.

Differences in propagation delay time are inherent in a gating system of this type. Signals may propagate through either two or three logic levels from an input (See Figure 2) to an output. Also, t_{pd0} and t_{pd1} are not generally equal for a given gate. As shown in Figure 5(a), these differences in propagation delay time may cause more than one output of an SN54/74154 to be at logical "0" simultaneously (logical "0" overlap). This overlap condition is typically 5 ns under data sheet test conditions.

Logical "0" spikes or logical "0" overlap at the outputs of an SN54/74154 may be detrimental to the performance of a logic system. If the Enable is used as shown in Figure 5(b), the spikes and overlap are eliminated. Taking the Enable line to logical "1" prior to changing an address input and holding it at logical "1" for 6 ns ($\geqslant$[tpd1(L)−tpd0(E)]) after the change of an address input will eliminate overlap problems for a typical device.

Propagation delay time from Enable or Data inputs to a logical "0" output is typically 19 ns (28 ns maximum).

PARAMETER		MIN	TYP	MAX	UNITS
$t_{pd0(L)}$	Propagation delay time to logical 0 level at output from A, B, C, or D inputs through two logic levels. [Input(s) going low]		20	30	ns
$t_{pd0(H)}$	Propagation delay time to logical 0 level at output from A, B, C, or D inputs through three logic levels. [Input(s) going high]		22	33	ns
$t_{pd1(L)}$	Propagation delay time to logical 1 level at output from A, B, C, or D inputs through three logic levels. [Input(s) going low]		25	37	ns
$t_{pd1(H)}$	Propagation delay time to logical 1 level at output from A, B, C, or D inputs through two logic levels. [Input(s) going high]		17	26	ns
$t_{pd0(E)}$	Propagation delay time to logical 0 level at output from Data or Enable inputs. [Input(s) going low]		19	28	ns
$t_{pd1(E)}$	Propagation delay time to logical 1 level at output from Data or Enable inputs. [Input(s) going high]		20	30	ns

Test Conditions: V_{CC} = 5 V, T_A = 25°C, N = 10, R_L = 400 Ω, C_L = 15 pF.

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FIGURE 4. Switching Characteristics For SN54/74154

Propagation delay time from Enable or Data inputs to a logical "1" output is typically 20 ns (30 ns maximum).

APPLICATIONS

The following section outlines several functions the SN54/74154 can perform.

For purposes of simplicity, reference will be made only to the Series 74 devices. All statements in this section about Series 74 devices also apply to the Series 54 devices.

Decoder

The use of the SN74154 as a 4-line to 16-line decoder is illustrated in Figure 6. Since Enable and Data are at logical "0", the addressed output will be logical "0". This type of circuit is often referred to as a 1-of-16 decoder.

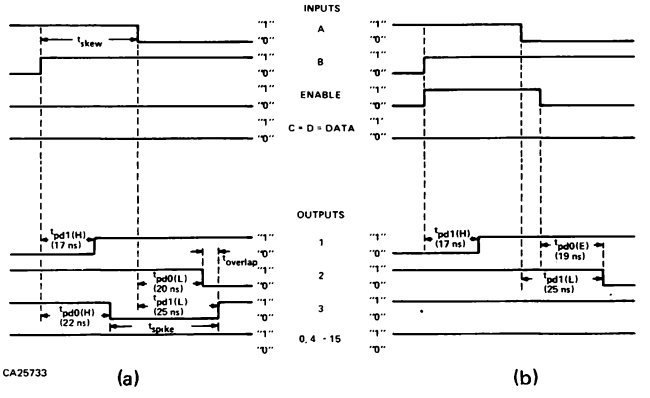


FIGURE 5. Typical Switching Waveforms Showing Effects Of Input Skew

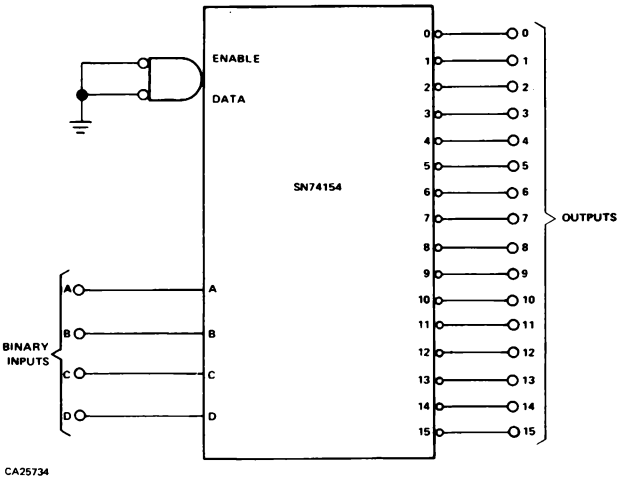


FIGURE 6. The 4-Line-to-16-Line Decoder

Figure 7 illustrates four SN74154 decoders used to decode 6 variables to 1 of 64 lines. Both Enable and Data inputs are used on the four devices to determine which device is activated. Since Enable and Data must be logical "0" to activate a device, proper decoding of the signals at these inputs is necessary to activate only one device at a time.

The above method can be extended to any number of variables with additional SN74154 devices. For instance an

8-line to 256-line (1-of-256) decoder can be constructed with seventeen SN74154 devices. As shown in Figure 8, one SN74154 decoder controls the Data inputs of sixteen others. By controlling the Enable line of device-16, all 256 outputs can be disabled simultaneously.

The 1-of-24 line decoder shown in Figure 9, demonstrates the use of the SN7442 4-to-10 line decoder with the SN74154. The full decoding capability of a second SN74154 is not necessary and a simpler decoder can be inserted in its place.

By using a SN7493 binary counter to drive the address inputs, a "Clock Time Generator" can be constructed. To obtain positive pulses from a particular output of the SN74154, an inverter must be inserted as shown in Figure 10. By using cross-coupled NAND gate latches,

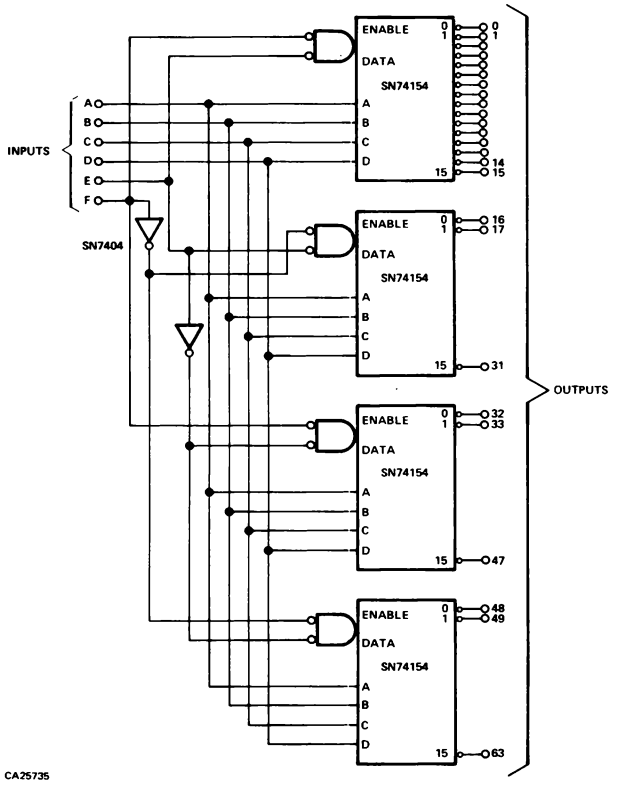


FIGURE 7. The 6-Line-To-64-Line Decoder

pulses can be extended over several clock pulse periods such as $T_{9\text{-}13}$, shown in Figure 10. The latch sets when output 9 goes low and resets when output 14 goes low. If the Data input is used as a strobe, decoding spikes may be eliminated from the output. This is especially important when an asynchronous counter such as the SN7493 is used on the address inputs.

Minterm Generator

When operated as a decoder, the SN74154 can function as a low active-output minterm generator producing 16 possible minterms from four variables. The desired minterms can be summed by a positive NAND (negative NOR) gate as illustrated for functions F_1, F_2, F_3, F_4, and F_6 in Figure 11.

Although limited to 10 outputs, the SN7442 4-line to 10-line decoder can be used in decoding applications similar to the SN74154 4-line to 16-line decoder. By use of NOR gates, an ANDing of input variables can be obtained from the outputs of the decoders as pictured for functions F_7, F_9, F_{11}, and F_{12}. The SN74154 AND-OR-INVERT gate is used as a 4-input NOR gate in Figure 11. Since H and I can be any variable, the outputs of other decoders can be used. Therefore, the number of variables ANDed together could far exceed the 9 variables listed for F_{12}.

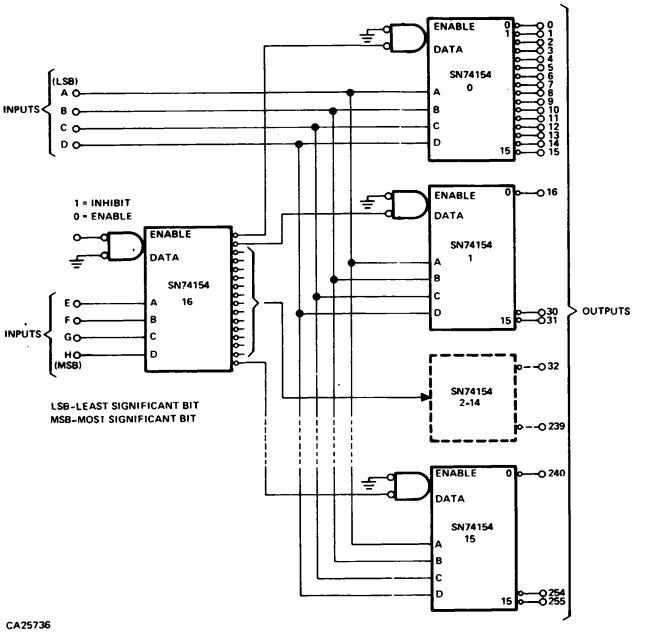


FIGURE 8. The 8-Line-to-Line Decoder with Inhibit Capability

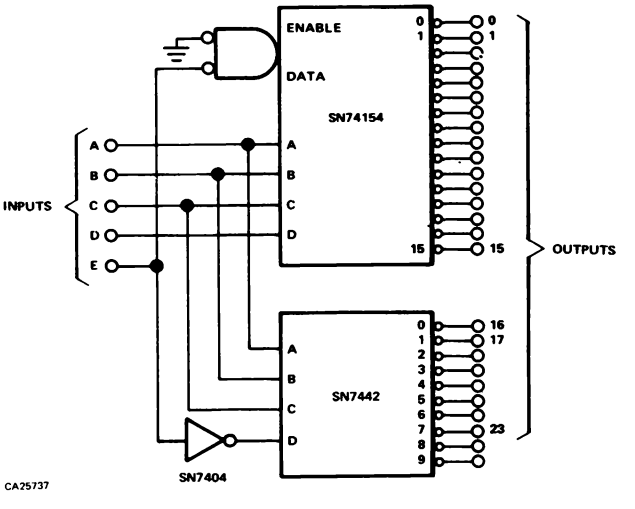


FIGURE 9. The 5-Line-to-24-Line Decoder

By using the SN7442 and SN74154 shown in Figure 11, any combination of the seven input variables A, B, C, D, E, F, and G can be obtained as an AND function by programming with only a two input NOR gate (F_9).

To illustrate the method used to obtain function F_5, refer to the Karnaugh maps in Figure 12. The function is mapped in Figure 12(a). As shown in Figure 12(b), the 1's are grouped to obtain the following minimal expression:

$$F_5 = \bar{B}CD + A\bar{C}D + \bar{A}BD$$

As illustrated in Figure 12(c), another method of grouping 1's is to encircle the group whose D is "1" and inhibit those individual cells within the group containing "0", i.e. $\bar{A}\bar{B}\bar{C}D$ and ABCD.

$$F = D \cdot \overline{(\bar{A}\,\bar{B}\,\bar{C}\,D)} \cdot \overline{(A\,B\,C\,D)}$$

$$F = \bar{B}CD + A\bar{C}D + \bar{A}BD = F_5$$

Note that F illustrated in Figure 12(c) is identical to F_5 when simplified. Since the inverted output exists for all 16 possible combinations of inputs, the latter method lends itself quite readily to use with the SN74154 decoder. A single three-input AND gate (SN74H11) or a NAND gate and an inverter will decode the complete expression from the SN74154 decoder. Figure 11 is only one example of how very complex logic operations can be implemented with only a few packages by using the SN74154 in combination with other MSI circuits (such as SN74150, -1, -2, -3, multiplexers and SN7442, -3, -4, and SN74155 decoders).

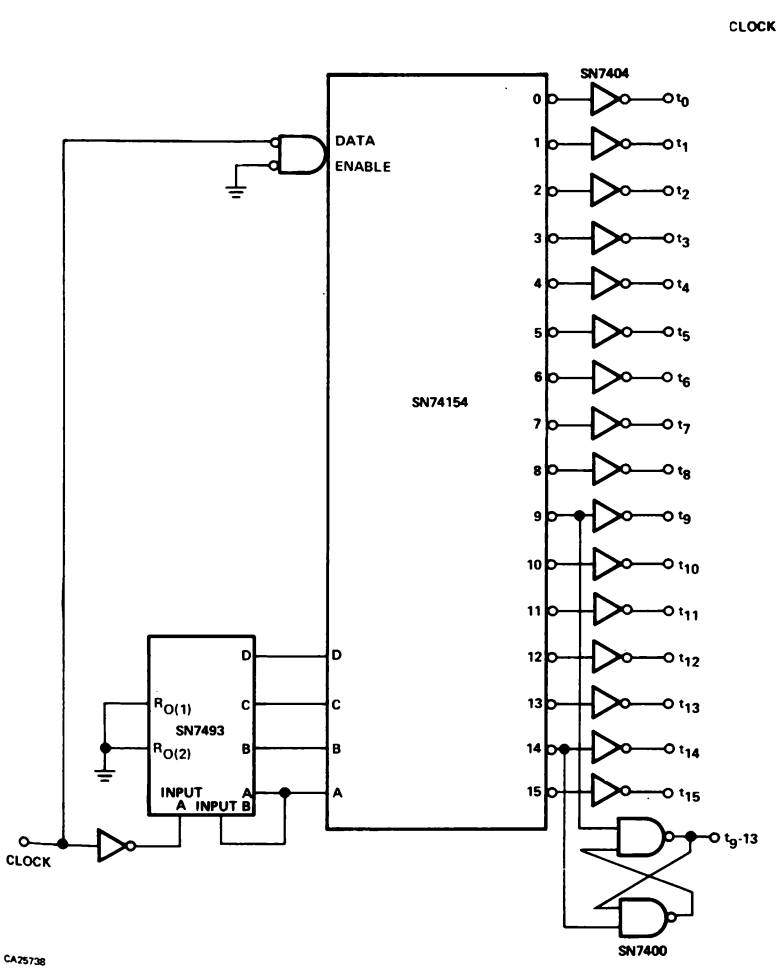
Code Decoders

Several special purpose 4-line to 10-line MSI decoders are available in the SN74 series. An SN7442 BCD-to-Decimal decoder is used for 8421 decoding. An SN7443 Excess 3-to-Decimal decoder decodes Excess-3 inputs directly. It also can decode the 2421 code if the D input is inverted and the outputs rearranged. Excess-3 Gray inputs are decoded by an SN7444 Excess-3 Gray-to-Decimal decoder.

Each special-purpose decoder above accepts only one specific four-bit code. But the SN74154 with strobe capability can decode *any* four-bit code if the appropriate outputs are selected in the desired sequence. For example, Figure 13(a) illustrates the output selection sequence necessary to completely decode the four-bit Gray code. And Figure 13(b) shows an output selection matrix by which the SN74154 can decode each of the four-bit decimal codes described above.

Demultiplexer

A typical application of the SN74154 used as a demultiplexer is illustrated in Figure 14. Parallel input data is converted to serial form by an SN74150 16-line to 1-line multiplexer. This serial information is then transmitted to the Data input of an SN74154. By operating the address inputs of the SN74150 and SN74154 synchronously,



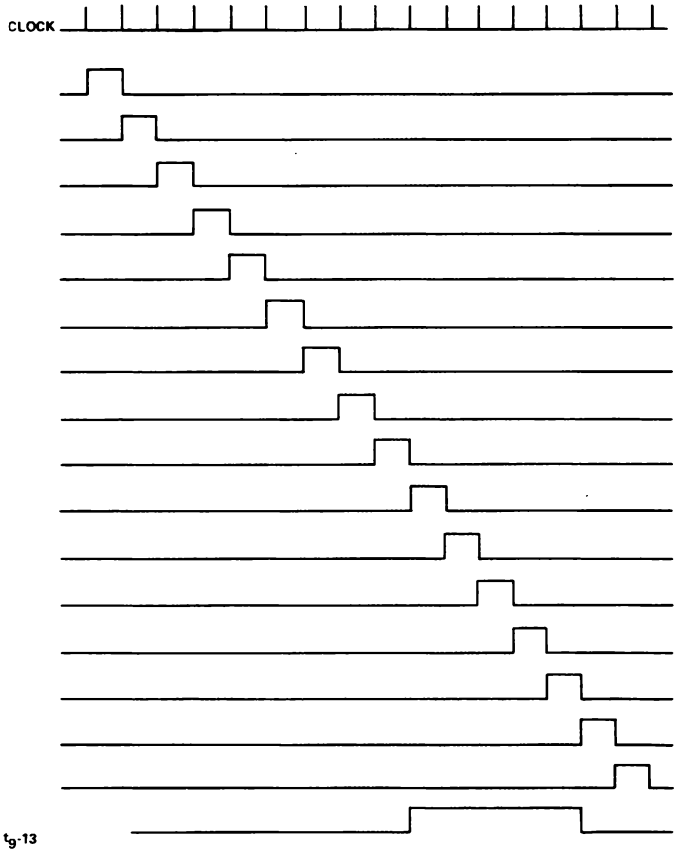


FIGURE 10. Clock Time Generator

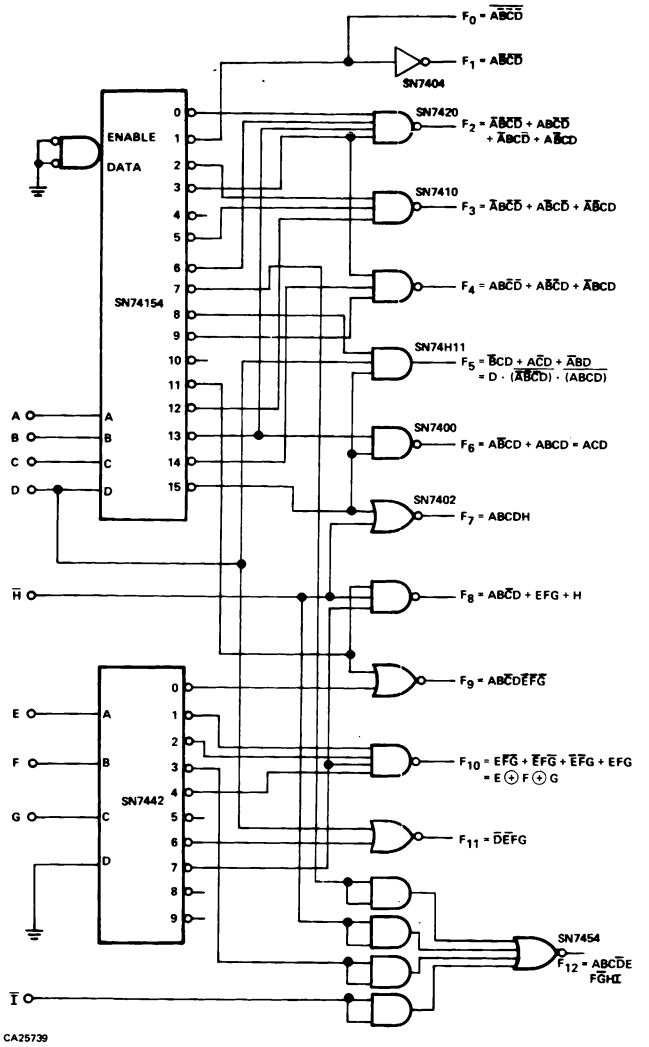


FIGURE 11. Minterm Generator

parallel information is transferred bit-by-bit from the parallel inputs of the SN74150 to the parallel outputs of the SN74154. Latches may then be used to store this data in parallel form.

Multiple bits of data may be transmitted from one parallel input of the SN74150 to the corresponding parallel output of the SN74154. When the system illustrated in Figure 14 is used in this manner, parallel storage latches at the output of the SN74154 are not necessary. Since the SN74150 inverts information, an inverter has been used at its output to re-invert the serial output data. No inversion occurs at the SN74154.

Often the digital data transmission system illustrated in Figure 14 is entirely adequate. However, transmission of error-free data over long lines in a noisy environment may require special transmission-line drivers and receivers and careful selection of a suitable transmission line. If necessary, the SN55107 series of Line Drivers and Line Receivers from Texas Instruments should be used to interface between transmission lines and TTL devices.

Figure 15 illustrates a method of obtaining a 32-line demultiplexer using two SN74154 devices. Since only two devices are involved, the complementary outputs of a

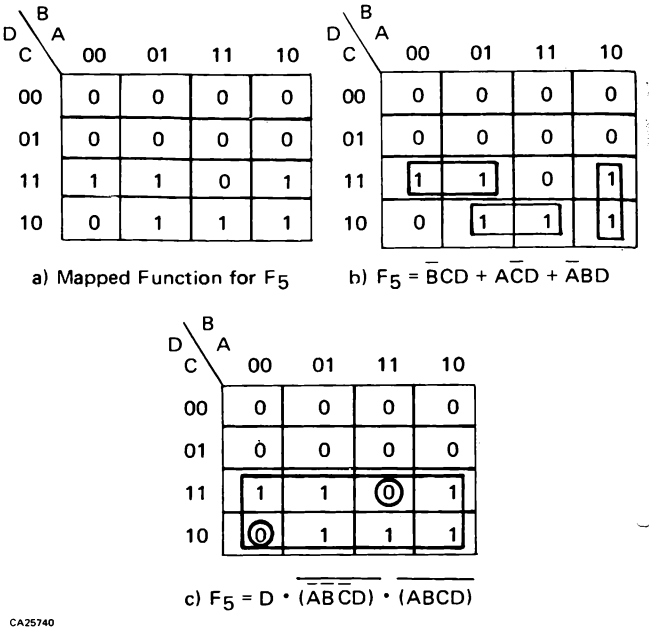
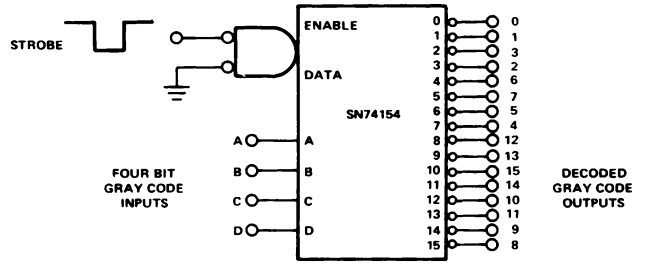


FIGURE 12. Mapping For Function F_5 Of Figure 11

flip-flop are used to select which device is activated. A strobe is gated with serial data to eliminate decoding spikes.

An SN74154 can be used for more complex demultiplexers than those illustrated above. For instance, the circuit illustrated in Figure 8 can be used as a 256-line demultiplexer simply by applying binary data to the Data input of device-16 and sequencing the address inputs.



a) Four-Bit Gray Code Decoder

Decimal Digit	SN74154 Output Selection			
	8421	Excess 3	2421	Excess 3 Gray
0	0	3	0	2
1	1	4	1	6
2	2	5	2	7
3	3	6	3	5
4	4	7	4	4
5	5	8	11	12
6	6	9	12	13
7	7	10	13	15
8	8	11	14	14
9	9	12	15	10

b) Output Selection for Decoding Four-Bit Decimal Codes

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FIGURE 13. Using An SN54/74154 To Decode Any Four-Bit Codes By Selecting Appropriate Outputs

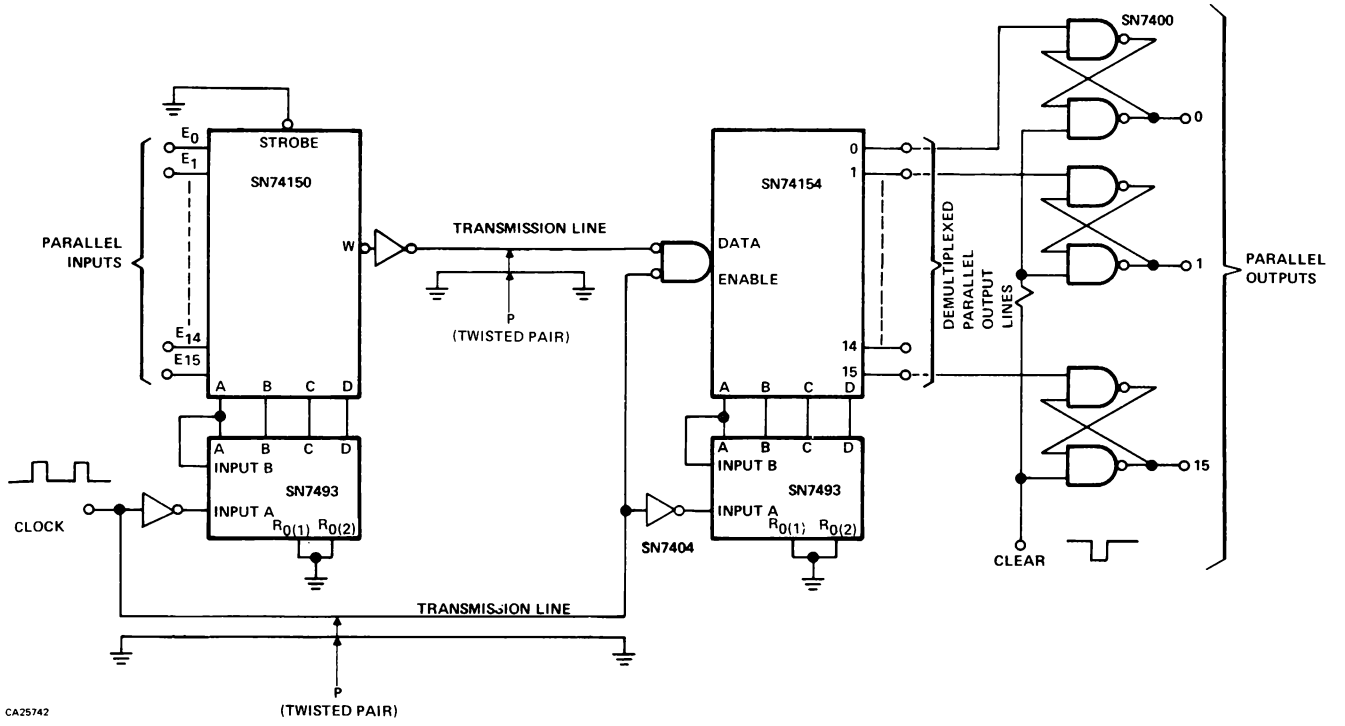


FIGURE 14. The 16 Line Parallel-To-Serial and Serial-To-Parallel Data Transmission System

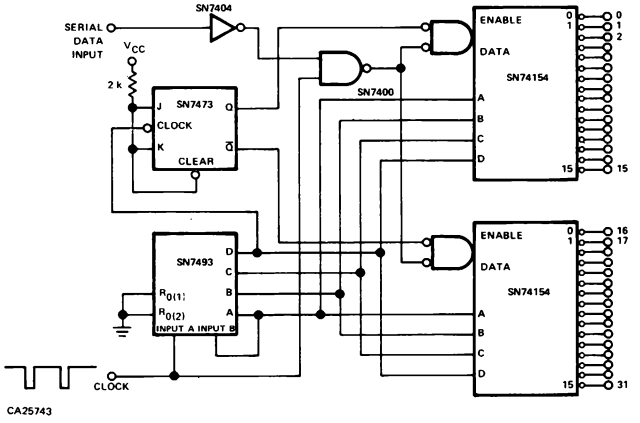


FIGURE 15. The 32-Line Demultiplexer

TTL Data Selectors
(CA 132)

TTL DATA SELECTORS

Sverre Wolff
Applications Design Department

INTRODUCTION

In digital systems, where information from multiple sources must be processed, stored, transferred, or handled in some other way, it is necessary to have circuits that provide selective access to information sources. Formerly, such selection circuits had to be implemented with separate logic gates which required several packages of integrated circuits. Now Texas Instruments Incorporated offers three types of integrated circuits in the 54/74 TTL series which act as data selectors or multiplexers. Use of these circuits leads to increased reliability due to a reduction in package count, number of interconnections, and wiring complexity.

These three types of circuits are available in both the industrial (74 series) and the military (54 series) temperature ranges and are compatible with other TTL and DTL circuits.

The circuits discussed here are:

SN54/74150 16-bit data selector with strobed inputs and inverted output. (Figure 1)

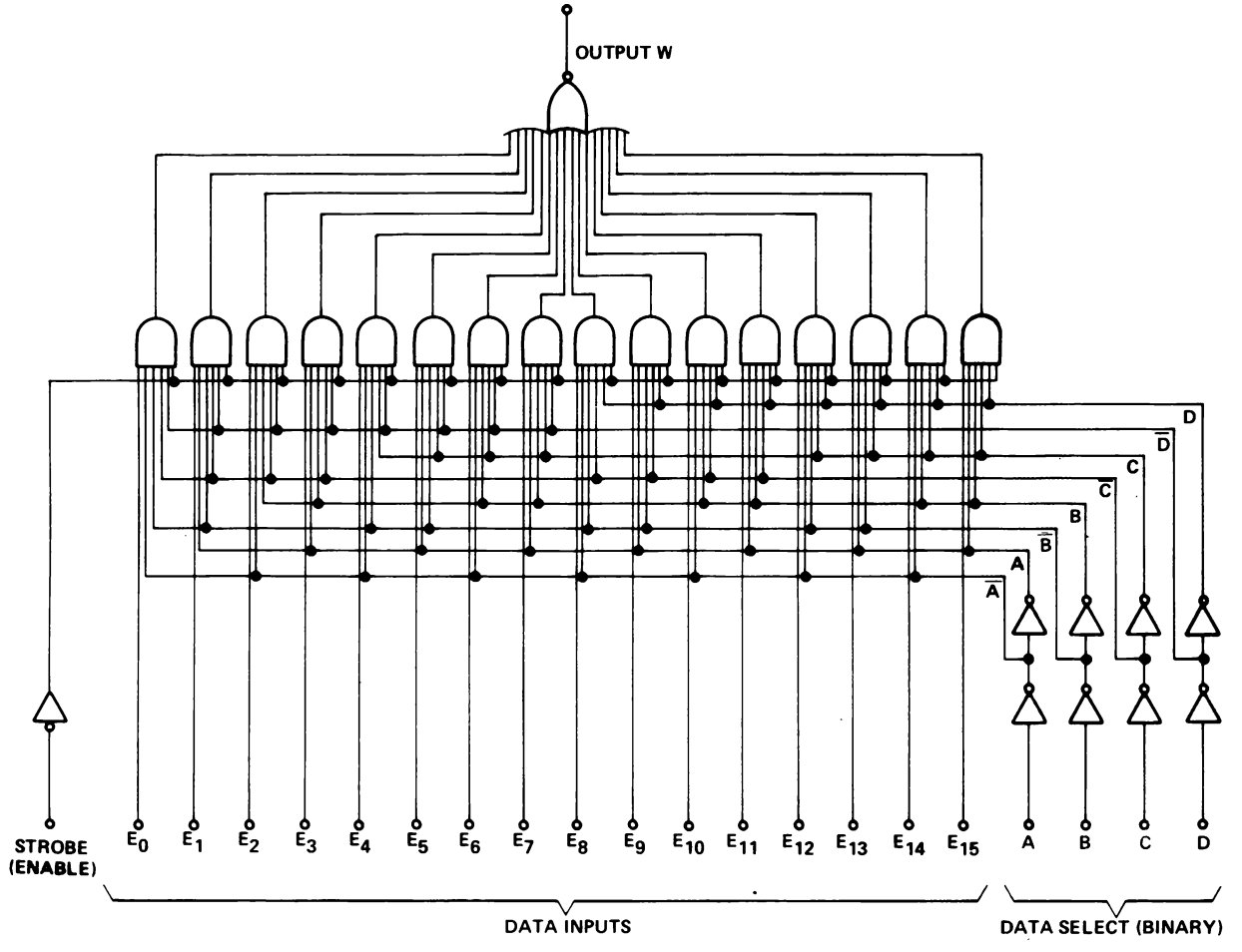


FIGURE 1. Functional Block Diagram of Data Selectors SN54/74150

SN54/74151 8-bit data selector with strobed inputs and complementary outputs. (Figure 2)

SN54/74152 8-bit data selector with inverted output. (Figure 3)

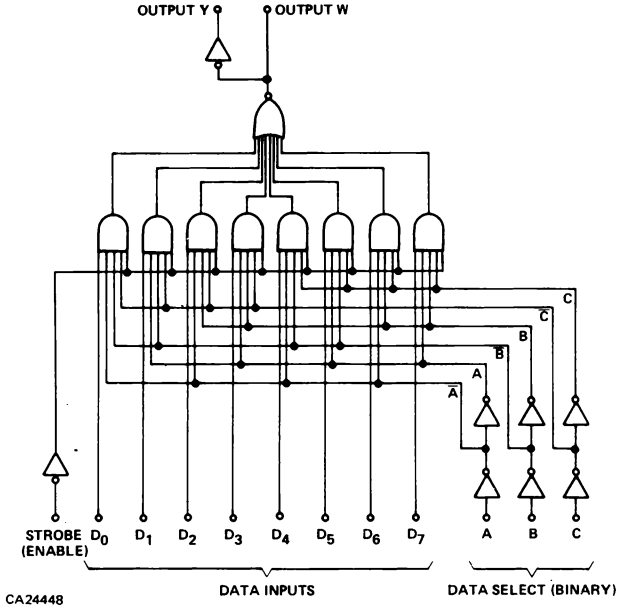


FIGURE 2. Functional Block Diagram of Data Selectors SN54/74151

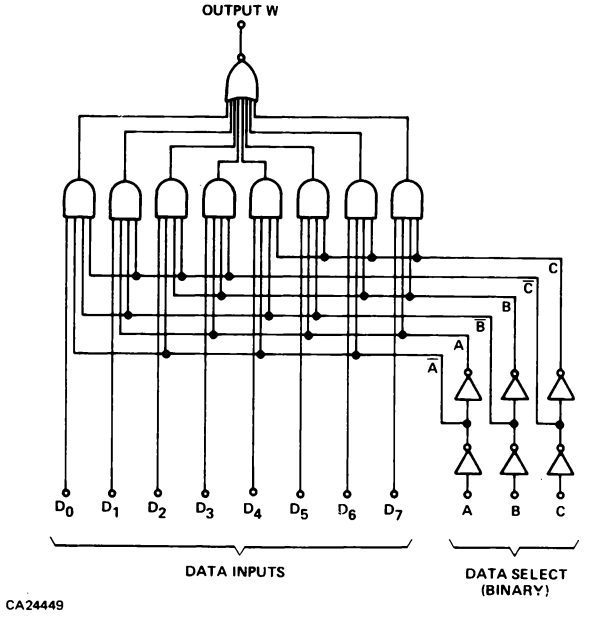


FIGURE 3. Functional Block Diagram of Data Selectors SN54/74152

This application report outlines the wide variety of functions these devices can perform and suggests applications for both the industrial and military series.

However for purposes of simplicity, reference will be made to only the 74 series. All statements in this report about the 74-series also apply to the 54-series.

DESCRIPTION AND CIRCUIT OPERATION

As shown in Figures 1 through 3, the TTL data selector circuit is basically an AND-OR-INVERT gate with a multiple number of OR branches. The SN74150 has 16 branches and the SN74151/152 have 8 branches each. Each AND-gate has its individual data input. E_0 through E_{15} are the inputs for the SN74150 and D_0 through D_7 are the inputs for SN74151/152. Any one of these inputs can be selected by applying the appropriate binary-coded address to the data-select terminals (A,B,C,D). The SN4150 and SN74151 have a strobe input (S), where a strobe signal can be applied concurrently with the address signal. A logical "0" at the strobe input enables the data present at the selected data-input to be coupled through to the output. On the other hand, logical "1" at the strobe input inhibits data transmission.

The SN74152 has no strobe-input terminal. It cannot be inhibited internally, with the result that there is always one data input coupled through to the output.

If the use of the SN74152 together with a strobe facility is mandatory, additional external logic circuitry must be used to create the enable/inhibit function.

LOGIC EQUATIONS: Logic operation of the data selector is characterized by the following logic equations:

SN74150:

$$W = \overline{\bar{S}(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7 + \bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})}$$

SN74151:

$$Y = \overline{W} = \overline{S}(\overline{A}\overline{B}\overline{C}D_0 + A\overline{B}\overline{C}D_1 + \overline{A}B\overline{C}D_2 + AB\overline{C}D_3 + \overline{A}\overline{B}CD_4 + A\overline{B}CD_5 + \overline{A}BCD_6 + ABCD_7)$$

SN74152:

$$W = \overline{\overline{A}\overline{B}\overline{C}D_0 + A\overline{B}\overline{C}D_1 + \overline{A}B\overline{C}D_2 + AB\overline{C}D_3 + \overline{A}\overline{B}CD_4 + A\overline{B}CD_5 + \overline{A}BCD_6 + ABCD_7}$$

CIRCUIT FEATURES: The following features have been incorporated in the data selectors:

1) The output NOR-gate is implemented with high-speed TTL (Series 54H/74H) circuitry which minimizes the capacitive effects of the paralleled phase-splitter transistors of the OR-branches, and thus reduces propagation delay time.
2) Clamping diodes to the substrate (ground) on all inputs limit negative input-voltage excursions and thus reduce the effects of line ringing.
3) The data selectors with strobed inputs (SN74150 and SN74151) are provided with internal strobe-pulse inverters. This reduces the loading of the external strobe–signal from eight or sixteen inputs to one input.
4) Each data-select input is connected with the appropriate AND-gate through two internal inverters in cascade. These inverters reduce external signal loading to one input and allow single–rail signal input.
5) The SN74151 has complementary outputs, which makes it extremely suitable for double– rail signal sourcing.

RANDOM DATA SELECTION

Data selectors can select at random one source out of a multitude of information sources, and couple the output of this source through to a single information channel or input. Data input can be selected by applying the appropriate binary-coded address to the data-select inputs (A, B, C or D).

The number of data inputs can be increased by using additional data selectors. A system using two data selectors is shown in Figure 4. When a strobed system is required, the control network of Figure 4a should be used with the network in Figure 4c. Use of the networks of Figures 4b and 4c results in a non-strobed system.

SEQUENTIAL DATA SELECTION

Sequential data selection can be performed with data selectors if the data-select address is taken from the outputs of a binary counter (SN7493), as in Figure 5. Operation of such a system resembles that of an electromechanical stepping switch. With each clock pulse, the binary counter switches to the next state, causing the data selector to select in sequence the information sources connected to its data inputs.

The number of data-inputs can be expanded by cascading data selectors and using appropriate control networks. A sequential data selection system with two data selectors and two alternative control networks is shown in Figure 6. A system with 'n' data selectors is shown in Figure 7.

In both the systems in Figures 6 and 7, two counters are used. Counter I supplies the binary-coded address. Counter II, followed by a decoding network, sequentially enables the data selectors.

In Figure 6, Counter II is a single flip-flop because only two data selectors are used.

If in the system of Figure 7, n is not an integral power of 2, conditioned resetting of Counter II is necessary. When the system is to be operated with a hold-off period, resetting of both Counter I and II is necessary. This mode of operation is described later.

In Figure 7, when hold-off signal H is a logical "1", conditioned reset is achieved in the following sequence:

1) The first undesired state of Counter II is decoded with NAND-gate 'a'.
2) Output of NAND-gate 'a' sets the reset-latch (cross-coupled NAND-gates b and c) in the "1" state.
3) Latch-signal Q resets Counter II (and if desired, also Counter I) to the all-zero state.
4) Counter II (and if applicable, also Counter I) remains in the all-zero state until a negative-going pulse appears at input H.

The inverted clock-pulse for Counter I may be used as signal H if the system is to repeat the selection cycles continuously. Such a mode of operation is possible if the change of incoming information for a data selector is made

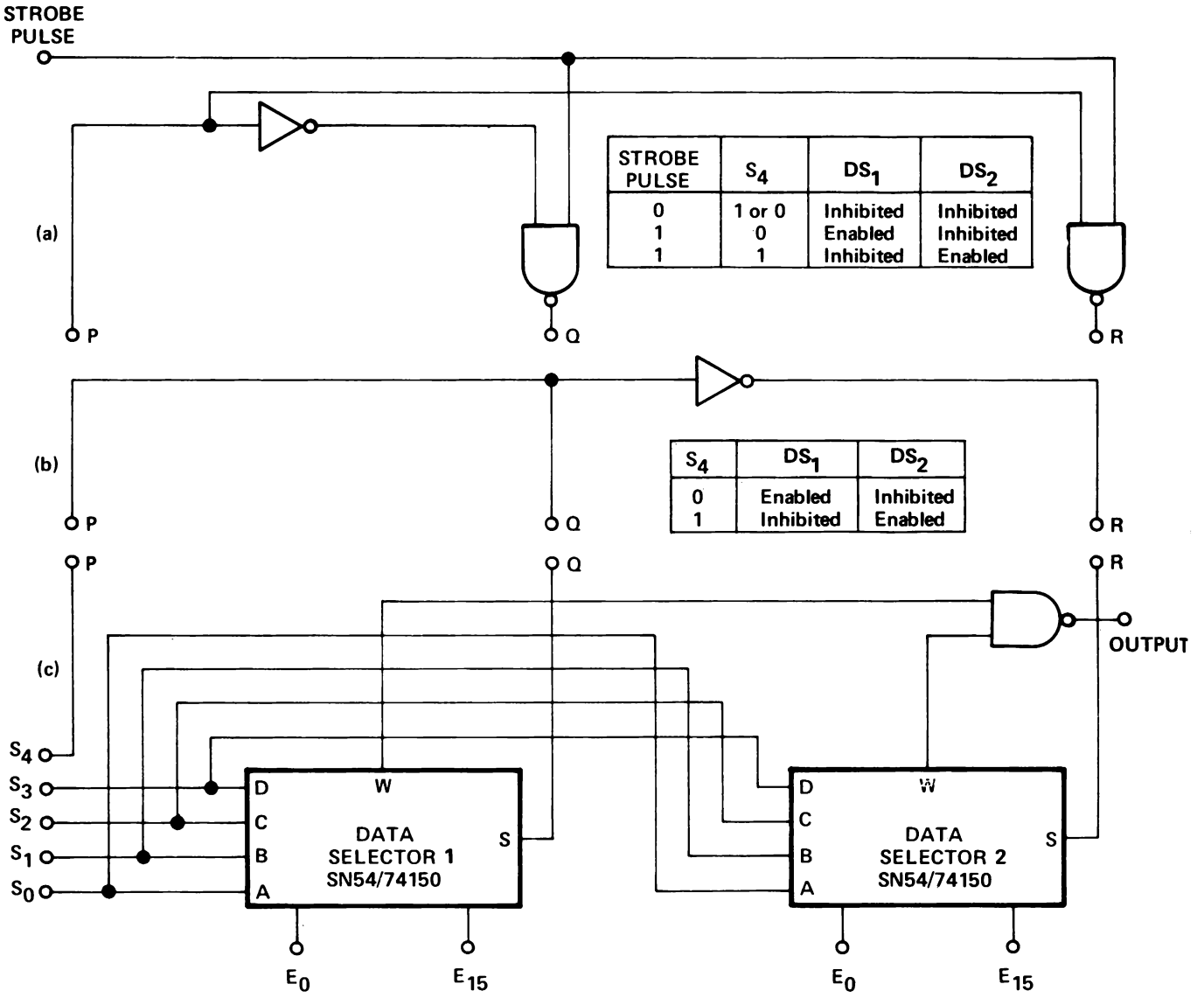


Figure 4. Block Diagram of Data Selectors Being Used to Select 1 out of 32 Information Sources
Control Circuit (b) + Circuit (c) Gives a Non-Strobed System
Control Circuit (a) + Circuit (c) Gives a Strobed System

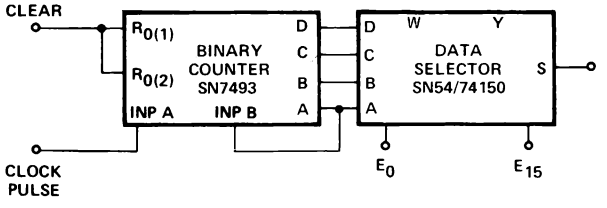


FIGURE 5. Block Diagram Using a Data Selector to Sequentially Select 1 Out of 16 Information Sources

during the time that the following data selector is being sampled. Change of incoming information for a data selector may then be triggered by the control (strobe) signal of the following data selector.

If an interim period is necessary to simultaneously change incoming information of all data selectors, Counter I as well as Counter II must be reset by the reset-latch, but the inverted incoming clock-pulse should *not* be used as signal H. In this operation mode, signal H functions as hold-off signal. As long as hold-off signal H is high, the

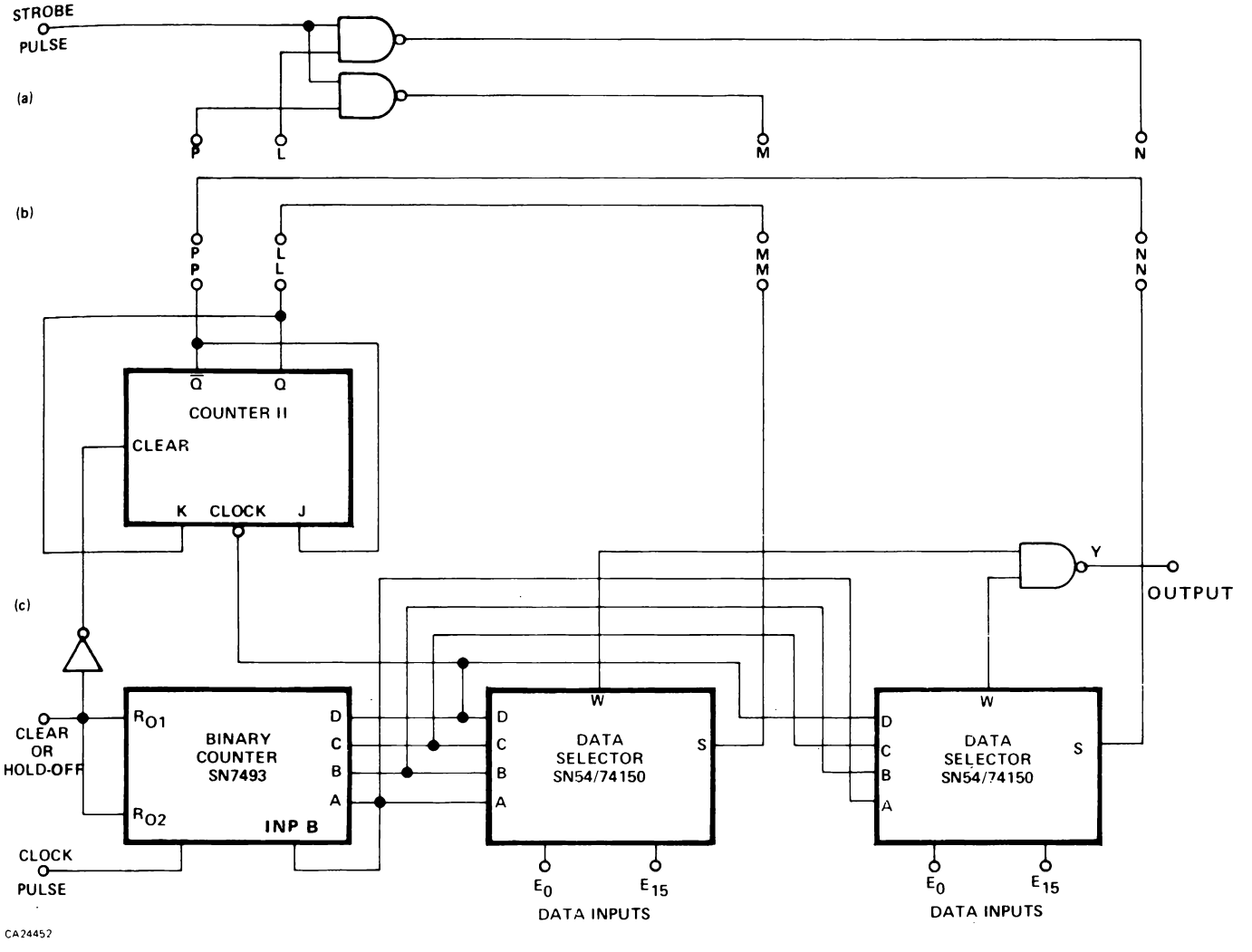


Figure 6. Block Diagram of Data Selector Being Used to Sequentially Select 1 out of 32 Information Sources
Control Circuit (a) + Circuit (c) Gives a Strobed System
Control Circuit (b) + Circuit (c) Gives a Non-Strobed System

reset-latch is not cleared and Counters I and II remain in the all-zero state. During the hold-off period, Inhibit-Enable signal I/E must be taken to a logical "0" to inhibit the data selectors.

If control circuit "c" of Figure 7 is used, the inverter in the I/E signal line may be omitted, in which case I/E input must be taken to a logical "1" to inhibit the data selectors.

The hold-off period can be terminated and a new cycle initiated by applying a negative-going pulse to the H input to clear the reset-latch, and taking the I/E input to a logical "1" to enable the data selectors (logical "0" in Figure 7c without I/E inverter).

PARALLEL-TO-SERIAL CONVERSION

Data selectors may be used to serialize parallel information. The circuits of Figures 5, 6, and 7 may be used for parallel-to-serial conversion.

The circuit of Figure 5 is capable of serializing one word of 16 bits or m words of 16/m bits.

The circuit of Figure 6 is capable of serializing one word of 32 bits or m words of 32/m bits.

Similarly, with the system of Figure 7, it is possible to serialize a word of 16n bits; or m words of 16n/m bits.

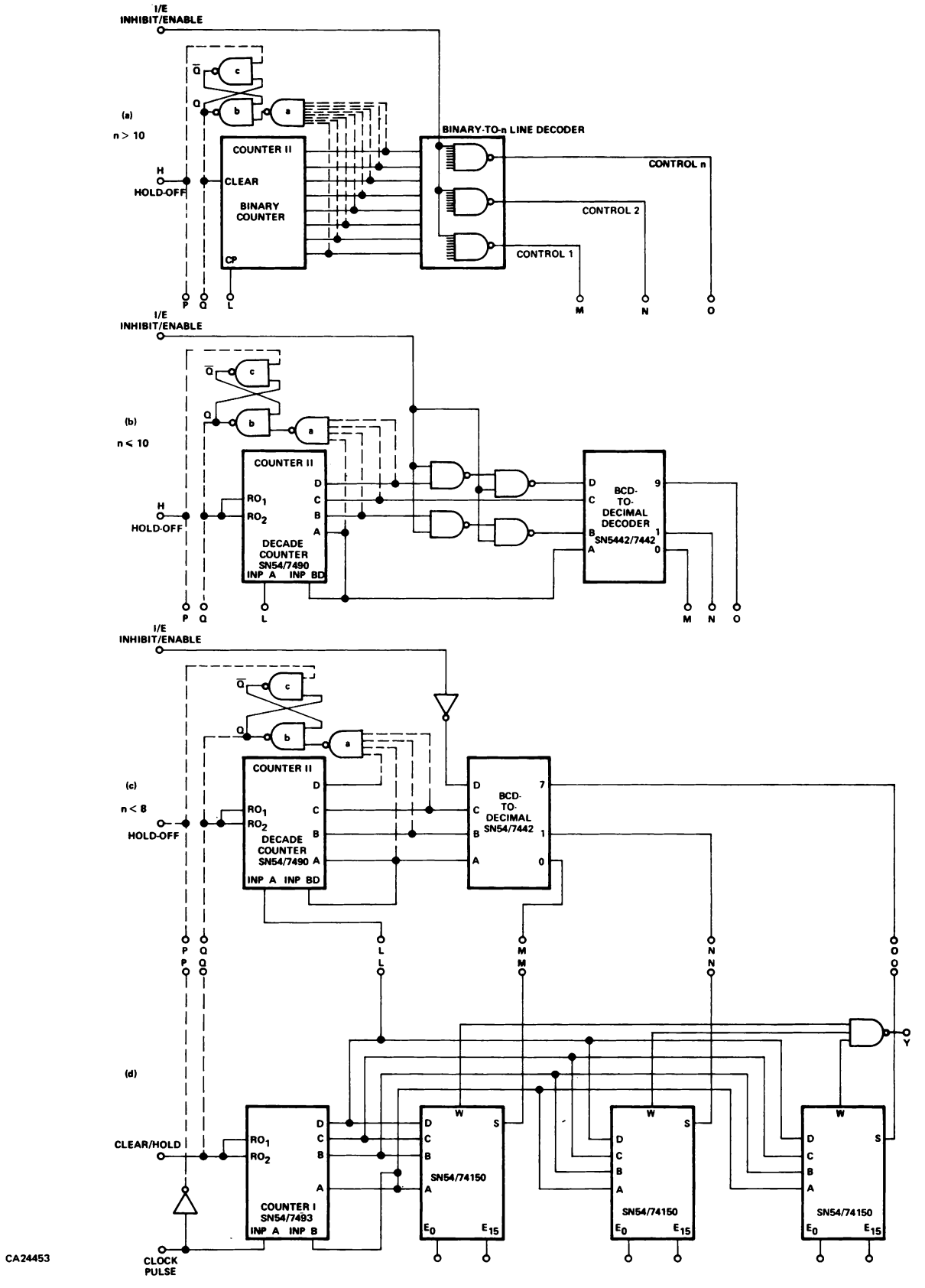


Figure 7. Block Diagram of Data Selectors Being Used for Sequential Selection of 1 out of n X 16 Information Sources Circuit (a) + Circuit (d) is Used for n = 10. Circuit (c) + Circuit (d) is Used for n ⩽ 8

MULTIPLEXING TO ONE LINE

The operations described in the previous sections are multiplexing to one line. The multiplexing capabilities of the circuits of Figures 5 through 7 can be enlarged by using shift registers as information sources. Thus, with a single data selector 16 words can be serially multiplexed onto one line by either shifting out or circulating (if the data must be preserved) the contents of the shift registers (Figure 8). The word length is determined by the number of stages of the shift registers. Very long words may be stored in adjacent shift registers. However the word capacity of the system will then be reduced.

A low-going loading signal (LS) indicates the shift register that is selected. The mode of operation of the shift registers is controlled by appropriate signals on the Register Control (RC) terminal.

The signals are,

RC = 0 for shift-out/serial-load
RC = 1 for data circulation

A complete cycle of either data shift-out/serial loading or data circulation is performed during each count cycle of the register (R) counter. Consequently, the R-counter must have as many states as the shift registers have stages. Loading of a shift register may take place during the cycle in which it is selected. In this case, LS-and RC-terminals with the same number must be connected. If the loading must occur in the following selection cycle, RC-terminals must be connected to the LS terminals with the next higher number. Any loading sequence may be obtained by connecting the RC-terminals to the appropriate LS-signals.

The data selector is strobed by the incoming clock-pulse while the shift registers and counters are operated by the inverted incoming clock-pulse. This is done to inhibit the data selector during the transition periods of the counters, shift registers and data inputs.

In Figure 9, a system similar to that of Figure 8 is shown. Here, shift registers for parallel loading are used. Loading of the registers takes place during the last clock-pulse of a selection cycle. If a register is to be loaded

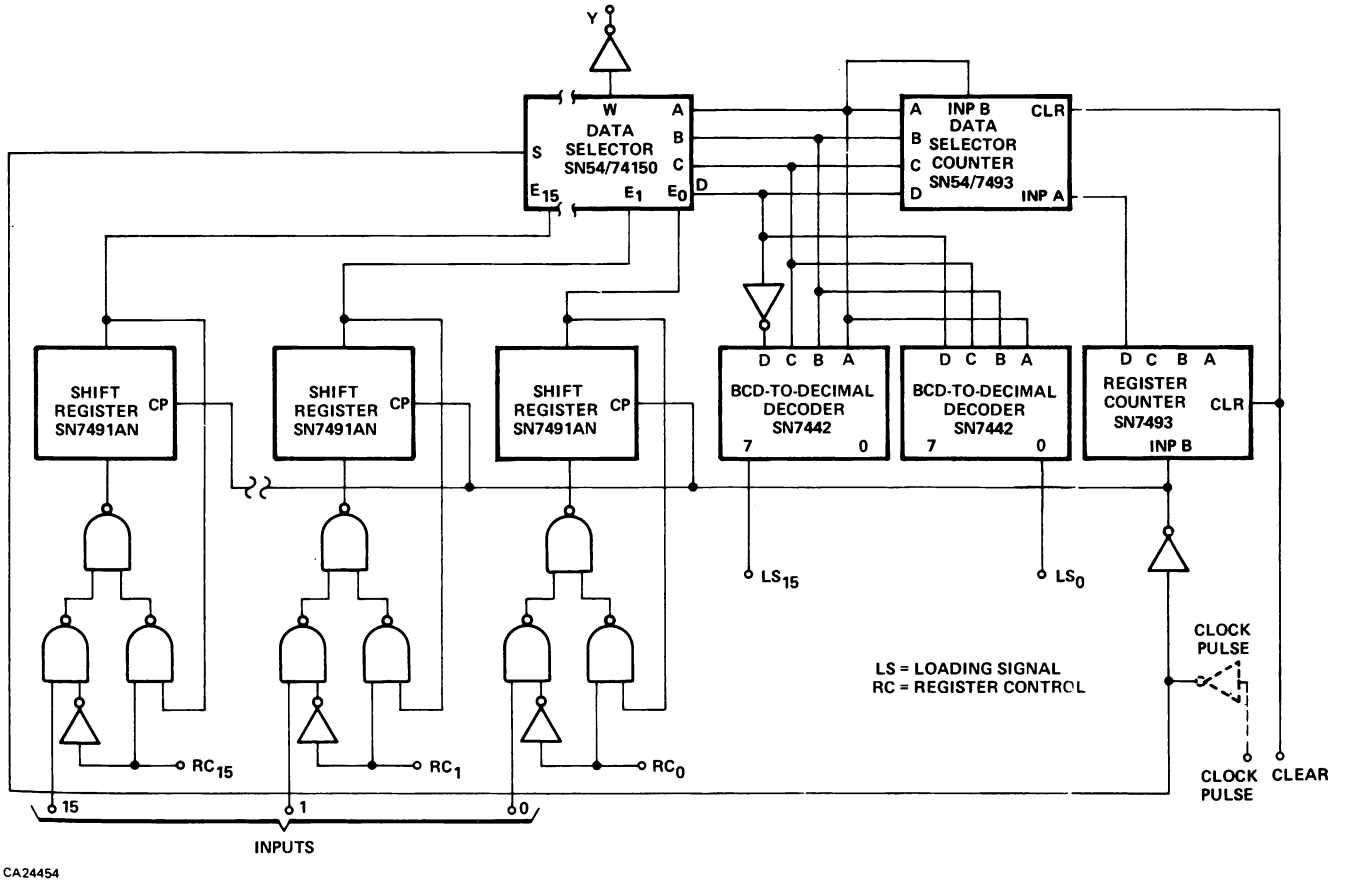


FIGURE 8. Block Diagram Showing Data Selectors Connected to Multiplex to a Single Output

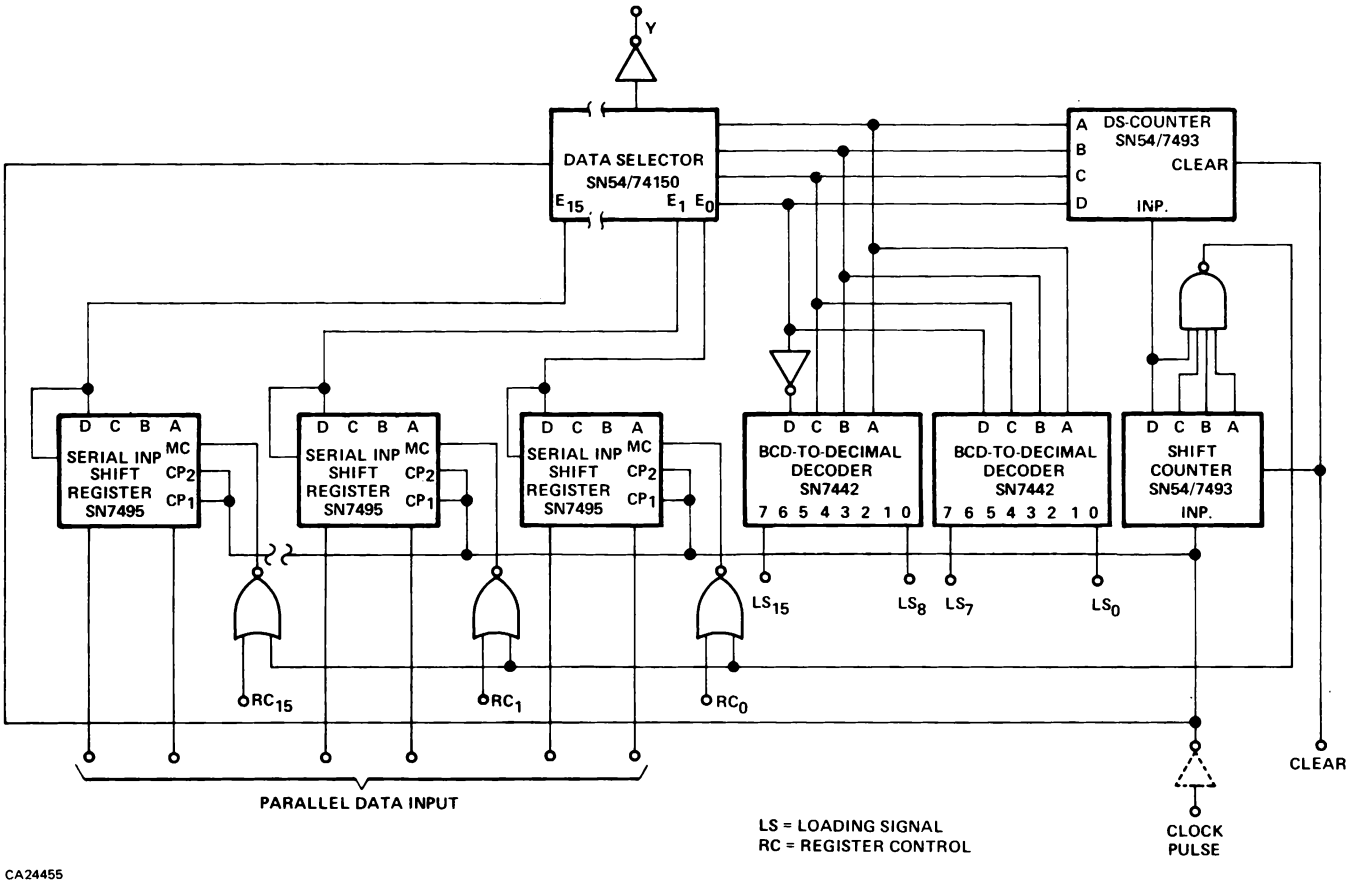


Figure 9. Block Diagram Using Data Selectors to Multiplex Parallel Inputs to a Single Output

at the end of its selection cycle, LS-and RC-terminals with the same numbers must be connected together. As with the previous system, any loading sequence can be obtained by connecting the appropriate LS-and RC-terminals. As in Figure 8, the data selector is inhibited during counter, shift register and data input transition periods.

If the information on the output of the data selector is to appear in phase with the incoming clock pulse, an additional inverter (dashed in Figures 8 and 9) may be used in the incoming clock-pulse line.

MULTIPLEXING TO MULTIPLE LINES

In general, multiplexing means transmitting a large number of information units over a smaller number of channels or lines. Consequently, the number of outgoing lines of a multiplexing system is not necessarily restricted to one. Multiplexing to multiple lines is necessary for instance when a multitude of words have to be transferred, a whole word at a time. For multiplexing n-bit words, n data selectors are necessary.

A system for multiplexing up to 16 words of n bits onto n parallel lines is shown in Figure 10. This system can be used either for random word selection, or with a binary counter (SN7493) for sequential word selection.

The word capacity of the circuit of Figure 10 can be expanded by using shift registers, in each of which are stored equally numbered bits of the words to be multiplexed. Shift registers with a length of m bits expand the word capacity of the system to m X 16 words of n bits.

Such a system is shown in Figure 11, where shift registers for serial loading are used. This system may be considered an expanded version of the system shown in Figure 8. Instead of one combination of shift registers and a data selector, n such combinations are used in parallel. Operation and control of this system is similar to that of the system of Figure 8. A low-going LS signal indicates which rank of shift registers have been selected. Shift register operation is controlled by the appropriate signals on the RC terminals.

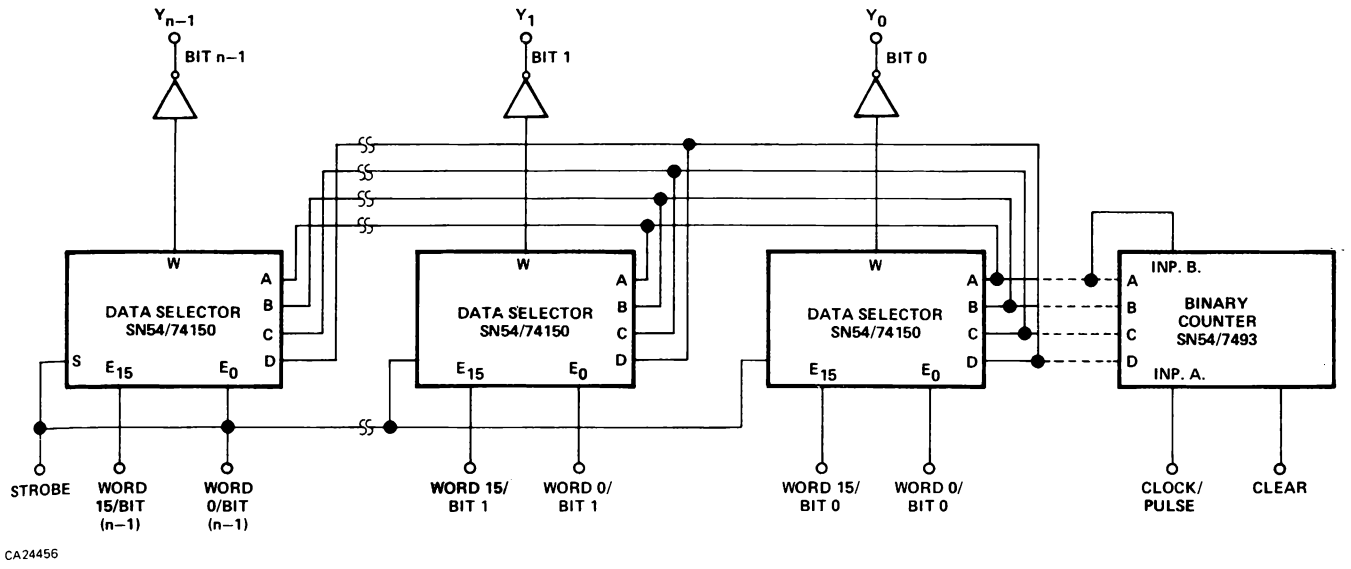


Figure 10. Block Diagram Showing Data Selectors Used to Multiplex Up to 16 Words of n Bits Onto n Parallel Lines

These signals are,

RC = 0 for shift-out/serial-load
RC = 1 for data circulation

Again, the shift registers perform a complete cycle of either shift-out/serial-loading or data circulation during each count cycle of the register (R) counter, which has as many states as the shift registers have stages.

As in the system of Figure 8, any shift register loading sequence may be obtained by connecting the RC-terminals to the appropriate LS-terminals. For instance, loading of a rank of shift registers occurs during the cycle in which the rank is selected, when equally numbered LS- and RC-terminals are connected together. The R-counter and the shift registers are operated with the *inverse* of the clock pulse which strobes the data selectors. This inhibits the data selectors during transition periods of the counters, shift registers and data inputs. In order to compensate for the high fan-out, power inverters are used in the clock-pulse lines.

If the enabling pulse of the data selectors must be in phase with the incoming clock pulse, an additional inverter (dashed in Figure 11) is used in the incoming clock-pulse line.

A system as in Figure 11 is also possible with shift registers for parallel loading. Such a system may be considered an expanded version of the system shown in Figure 9. Instead of one combination of shift registers and a data selector, n such combinations are used in parallel.

DATA SELECTORS AS CHARACTER GENERATORS

Data selectors with a binary counter for sequential selection can be used as character generators. The characters to be generated may be either fixed (wired-in), or manually changeable (switches). Further, they may be controlled and/or determined by a logic system.

In Figure 12 a character generator for manually changeable characters using an SN74151 is shown. In fact, every data selector circuit with sequential selection can be used as a character generator. The circuits shown in Figures 5, 6, 7, 8, and 9 can be used as character generators with each character appearing in serial form at the output.

The circuits of Figures 10 and 11 are capable of generating characters in parallel form or multiple characters in serial form.

BINARY WORD COMPARISON WITH DATA SELECTORS

Data selectors may be used with 4-line to decimal decoders to determine quality of binary words.

In Figure 13, a comparator for two 3-bit words is shown. It uses a BCD-to-decimal decoder, SN7442N, and the eight-bit data selector, SN74151, which has complementary outputs. The SN7442N is used as a 3-line binary-to-octal decoder with an enable/inhibit input D (outputs 8 and 9 are not used). The comparator is enabled when the D-input of the SN7442N is taken to a logical "0". A logical "1" on the D-input inhibits the comparator. The

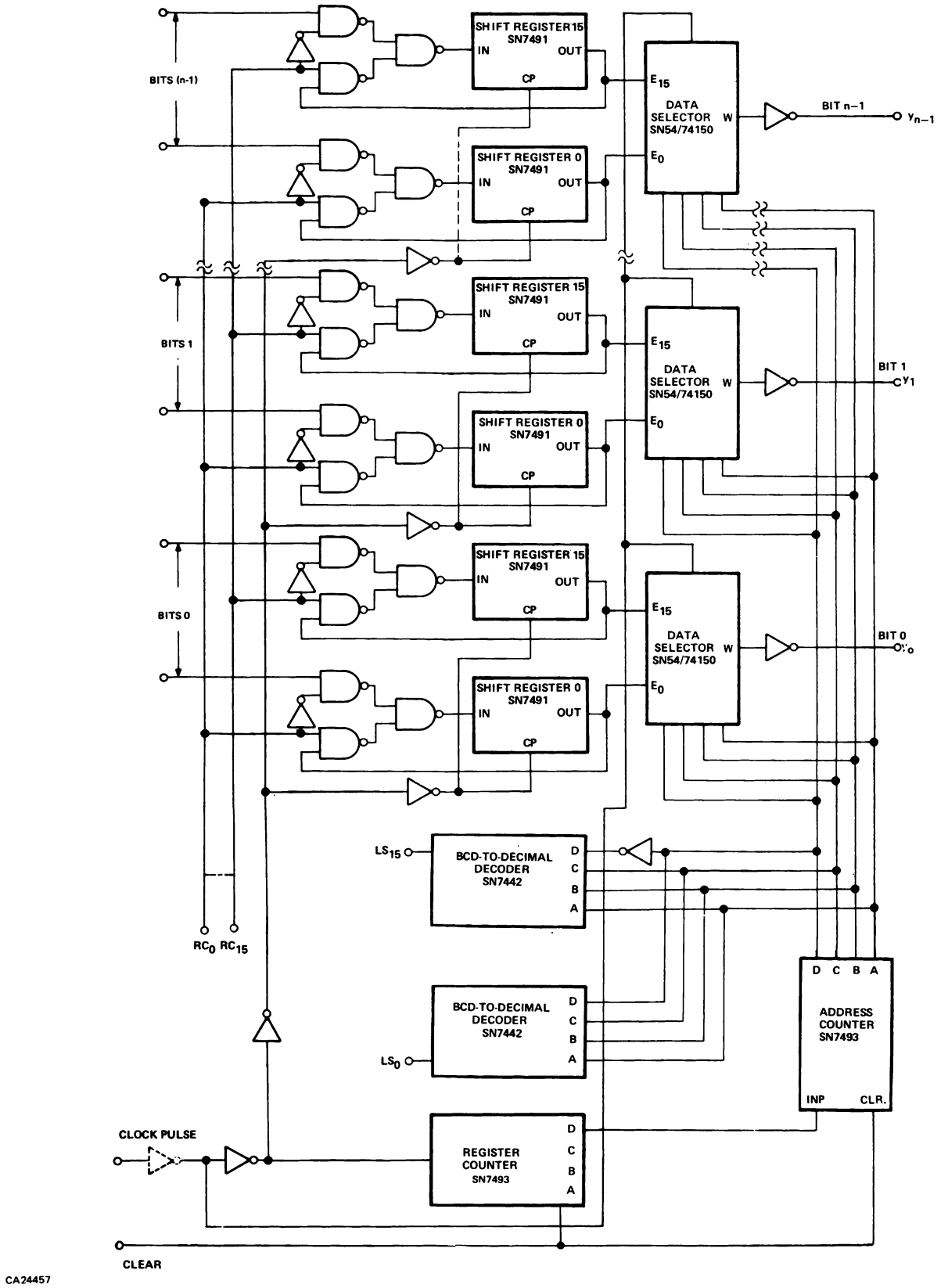


Figure 11. Block Diagram of Data Selectors Being Used to Multiplex 16m Words of n Bits Onto n Parallel Lines

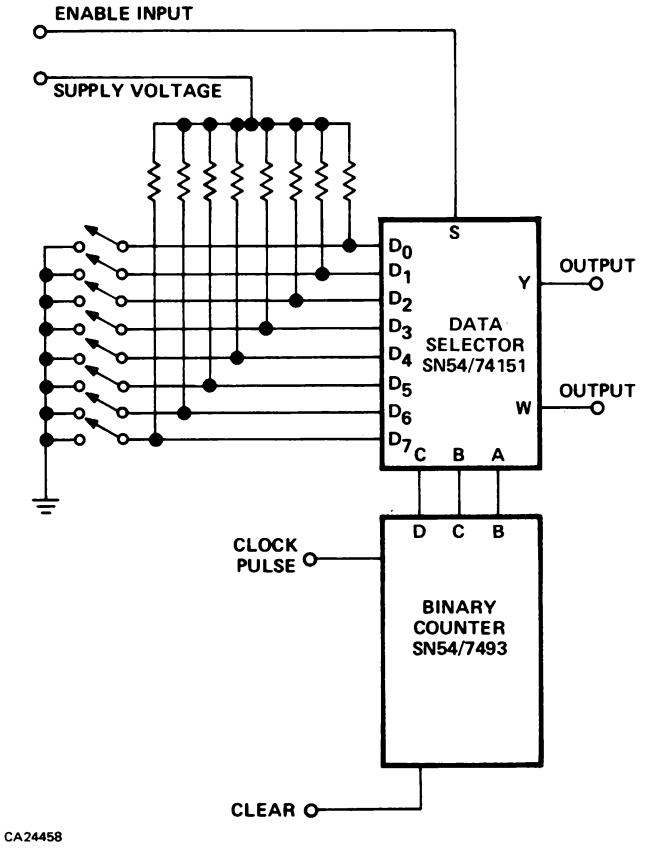


FIGURE 12. Block Diagram of a 8-Bit Character Generator for Manually Changeable Characters

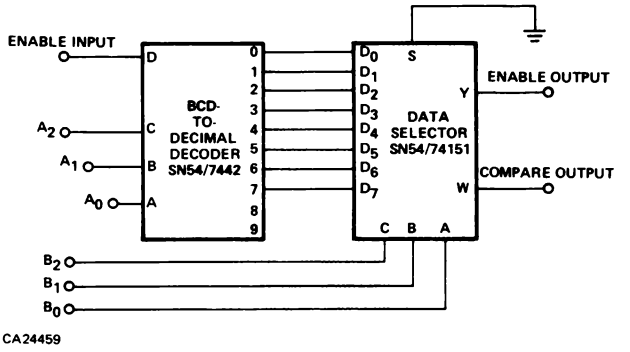


FIGURE 13. Block Diagram of a Data Selector Used as a Comparator for 2 Words of 3 Bits

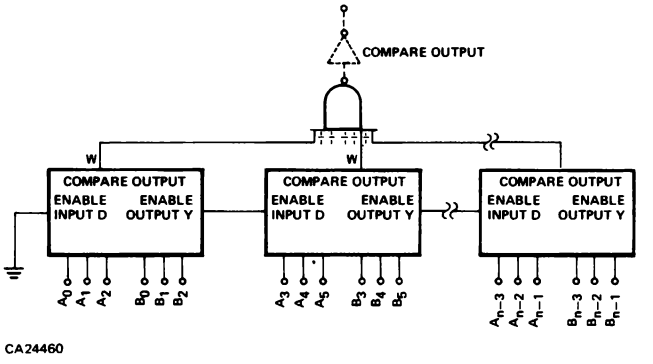


FIGURE 14. Block Diagram of Comparators Cascaded to Compare Longer Words

comparator has two outputs: a compare output, W and an enable output, Y. The output signals in the enabled and inhibited states are as follows:

D = 0 (Comparator Enabled):

W = 1 and Y = 0 if, word A = word B

W = 0 and Y = 1 if, word A ≠ word B

D = 1 (Comparator Inhibited):

W = 0 and Y = 1 regardless whether words A and B are equal or not.

If a logical "0" output signal is required to indicate equality, then the enable-output Y may be used as the enable as well as the compare output.

The comparator shown in Figure 13 may be cascaded to compare longer words, as is shown in Figure 14. If equality is to be indicated by a logical "1" an additional inverter (dashed in Figure 14) is necessary.

The data selector, SN74151, in the circuits of Figures 13 and 14 may be replaced by the SN74152 if the enable output-signal Y is an external inversion of output-signal W. This inversion is not necessary when the SN74152 is used in conjunction with the excess-3-Gray-to-decimal decoder, SN7444, as is shown in Figures 15 and 16.

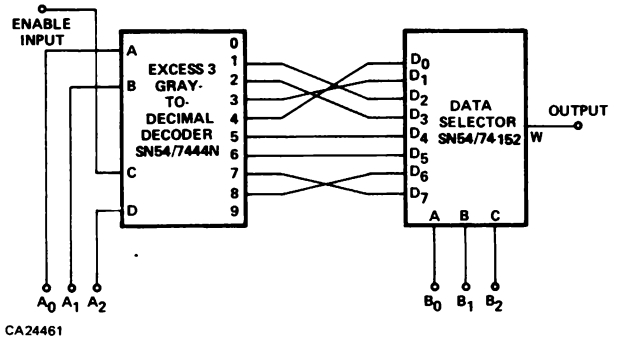


FIGURE 15. Block Diagram of a Comparator Used to Compare 2 Words of 3 Bits Using an Excess-3-Gray-to-Decimal Decoder

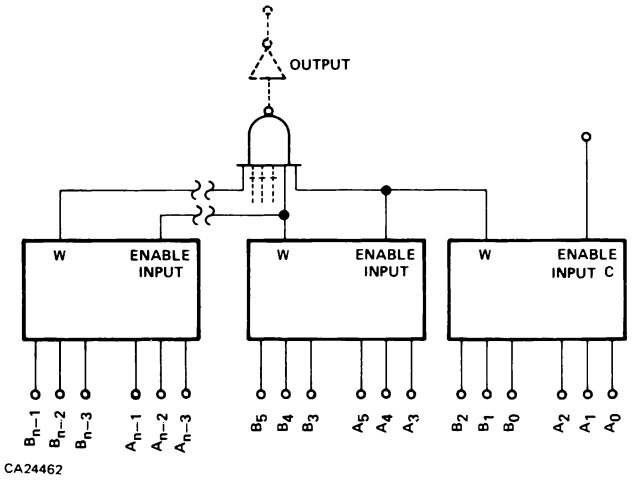


FIGURE 16. Block Diagram of Comparators from Figure 15 Cascaded for 2 Words of n Bits

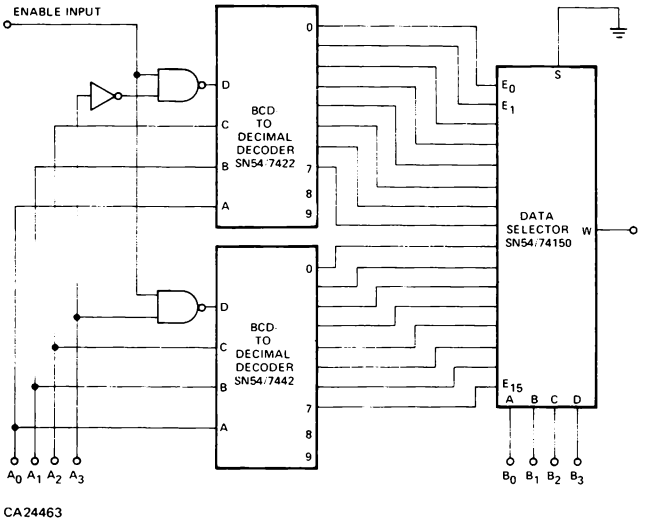


FIGURE 17. Data Selector Used as a 4 Bit Word Comparator

In these figures, the decoder is used as a 3-line-binary-to-octal decoder (outputs 0 and 9 are not used) with input C as the enable/inhibit control. Input C must be a logical "1" to enable the comparator and a logical "0" to inhibit it. Output signal W in the enabled and inhibited states is as follows:

C = 1 (Comparator Enabled):

W = 1 if, word A = word B

W = 0 if, word A ≠ word B

C = 0 (Comparator Inhibited):

W = 0 regardless whether words A and B are equal or not.

As a consequence, output W is the compare-output as well as enable-output, and no external inversions are necessary.

In Figure 17, a comparator for two 4-bit words using two BCD-to-Decimal decoders, SN7442, and one 16-bit data selector, SN74150, is shown. The decoders are again used as 3-line binary-to-octal decoders with input D as enable/inhibit input. The decoder enable/inhibit inputs are controlled through NAND gates by the comparator enable-input and the most significant bit of word A. In fact, the combination of the two decoders form a 4-line binary-to-hexadecimal decoder. A logical "1" on the enable input enables the comparator, whereas a logical "0" inhibits it.

Output signals in the enabled and inhibited states are as follows:

Enable input = 1 (Comparator Enabled):

W = 1 if word A = word B

W = 0 if word A ≠ word B

Enable input = 0 (Comparator Inhibited):

W = 0 regardless whether words A and B are equal or not.

Consequently, output W can be used as the compare-output as well as the enable-output.

Also, the comparator of Figure 17 may be cascaded to compare longer words, as is shown in Figure 18. If a logical "1" output signal is required to indicate equality, an additional inverter (dashed in Figure 18) is necessary.

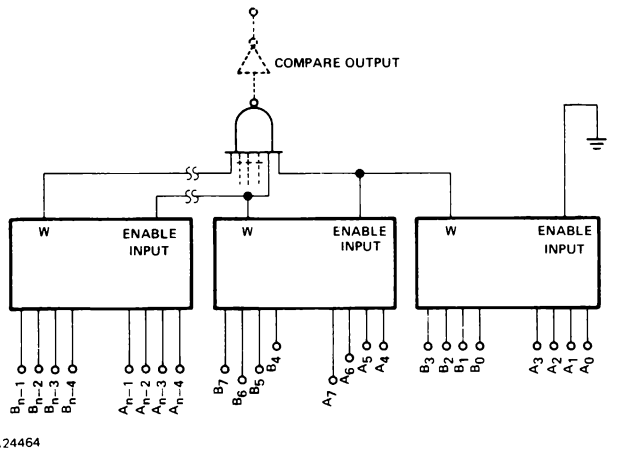


FIGURE 18. Block Diagram of Cascaded Comparators from Figure 17 Used to Compare 2 Words of n Bits

IMPLEMENTING LOGIC FUNCTIONS WITH DATA SELECTORS

Almost any logic function can be implemented with data selectors. The simplest implementation is obtained when the logic function can be written either as a true or an inverted sum of products of its logic variables, because the characteristic logic expression of data selectors is an inverted sum of products.

To implement a given logic function it is necessary to select a data selector which is able to satisfy all (min) terms of the function, directly or through conditioning.

The logic function of the data selector SN74150 is

$$\begin{aligned} Y = \overline{W} = \overline{S}\,(&\overline{A}\overline{B}\overline{C}\overline{D}\overline{E}_0 + \overline{A}\overline{B}\overline{C}\overline{D}E_1 + \overline{A}\overline{B}\overline{C}D\overline{E}_2 \\ &+ \overline{A}\overline{B}\overline{C}DE_3 + \overline{A}\overline{B}C\overline{D}\overline{E}_4 + \overline{A}\overline{B}C\overline{D}E_5 \\ &+ \overline{A}\overline{B}CD\overline{E}_6 + \overline{A}\overline{B}CDE_7 + \overline{A}B\overline{C}\overline{D}\overline{E}_8 \\ &+ \overline{A}B\overline{C}\overline{D}E_9 + \overline{A}B\overline{C}D\overline{E}_{10} + \overline{A}B\overline{C}DE_{11} \\ &+ \overline{A}BC\overline{D}\overline{E}_{12} + \overline{A}BC\overline{D}E_{13} + \overline{A}BCD\overline{E}_{14} \\ &+ ABCDE_{15}) \end{aligned}$$

When S = 0, the data selector is enabled and, the logic expression for the SN74150, with an external inverter, is

$$\begin{aligned} F = &\overline{A}\overline{B}\overline{C}\overline{D}\overline{E}_0 + \overline{A}\overline{B}\overline{C}\overline{D}E_1 + \overline{A}\overline{B}\overline{C}D\overline{E}_2 + \overline{A}\overline{B}\overline{C}DE_3 \\ &+ \overline{A}\overline{B}C\overline{D}\overline{E}_4 + \overline{A}\overline{B}C\overline{D}E_5 + \overline{A}\overline{B}CD\overline{E}_6 + \overline{A}\overline{B}CDE_7 \\ &+ \overline{A}B\overline{C}\overline{D}\overline{E}_8 + \overline{A}B\overline{C}\overline{D}E_9 + \overline{A}B\overline{C}D\overline{E}_{10} + \overline{A}B\overline{C}DE_{11} \\ &+ \overline{A}BC\overline{D}\overline{E}_{12} + \overline{A}BC\overline{D}E_{13} + \overline{A}BCD\overline{E}_{14} \\ &+ ABCDE_{15} \end{aligned} \quad (1)$$

Similarly, for the SN74151 and SN74152, the following expression is valid.

$$\begin{aligned} F = &\overline{A}\overline{B}\overline{C}\overline{D}_0 + \overline{A}\overline{B}\overline{C}D_1 + \overline{A}\overline{B}C\overline{D}_2 + \overline{A}\overline{B}CD_3 + \overline{A}B\overline{C}\overline{D}_4 \\ &+ \overline{A}B\overline{C}D_5 + \overline{A}BC\overline{D}_6 + ABCD_7 \end{aligned} \quad (2)$$

The logic function to be implemented can be obtained from expressions (1) or (2) by conditioning the desired minterms, and eliminating unused minterms. A minterm is conditioned by applying the appropriate logic signal to its corresponding data input. Such a conditioning signal can vary from a simple logical "1" to the output signal of a complex gate array of combinational logic. Minterms are eliminated by applying a logical "0" to the appropriate data inputs.

If more minterms than are available in expressions (1) and (2) are required, they may be created by appropriate conditioning of one or more data inputs and/or using more than one data selector connected as in Figure 19. Use of n data selectors with m data inputs provide a total of mn minterms.

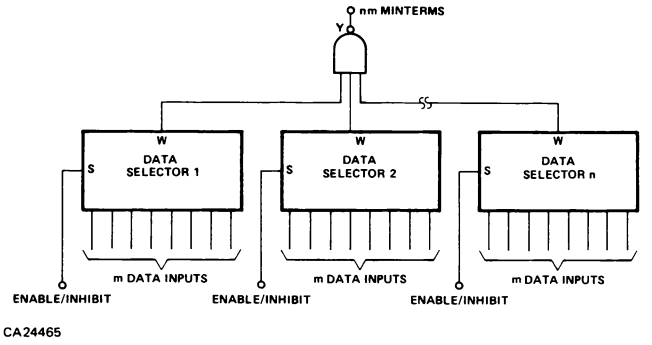


FIGURE 19. Block Diagram Showing How Minterms Can Be Expanded By Cascading Data Selectors

KARNAUGH MAPS: Several approaches are possible to determine, for a given logic function, which minterms are to be eliminated or conditioned. One such method is the use of Karnaugh maps.

A Karnaugh map is an orderly arrangement of all possible combinations of its variables. Each cell represents a unique combination of these variables. In other words, each cell represents a minterm.

Numerical values can be assigned to the cells of a Karnaugh map by considering the minterms as binary numbers.

When the logic expression of a data selector is represented by a Karnaugh map, the numerical value assigned to a cell corresponds with the number of the data input which governs the minterm represented by that cell. This means that the cell with numerical value n represents the minterm governed by E_n, in the case of the SN74150, and by D_n when the SN74151 or SN64152 is considered.

B A / C	00	01	11	10
0	0 D_0	1 D_1	3 D_3	2 D_2
1	4 D_4	5 D_5	7 D_7	6 D_6

FIGURE 20. Three-Variable Karnaugh Map With Numerical and Data Input Designations for SN54/74151 and SN54/74152

B A / D C	00	01	11	10
00	0 E_0	1 E_1	3 E_3	2 E_2
01	4 E_4	5 E_5	7 E_7	6 E_6
11	12 E_{12}	13 E_{13}	15 E_{15}	14 E_{14}
10	8 E_8	9 E_9	11 E_{11}	10 E_{10}

FIGURE 21. Four-Variable Karnaugh Map With Numerical and Data Input Designations for SN54/74150

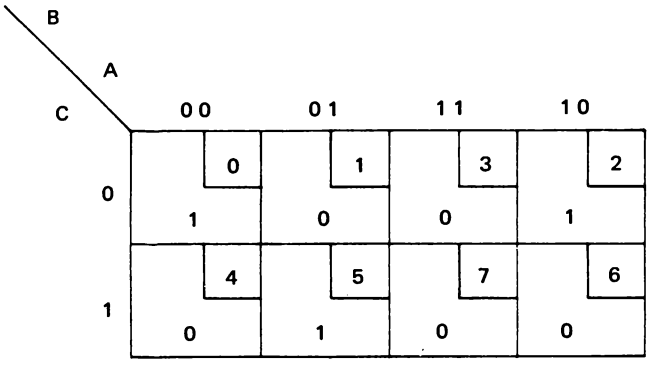
Three- and four-variable Karnaugh maps with numerical and data-input designations are shown in Figures 20 and 21. A is the least significant variable.

When the number of variables in the logic function to be implemented is equal to or less than the number of data select inputs of the data selector, a single map representation of the desired logic function is used to determine data input conditioning. The data inputs governing cells marked "0" must be made logical "0" and those governing cells marked "1" must be made a logical "1".

When the number of variables in the desired logic function is greater than the number of data select inputs of the data selector, it is easier to use multiple map representation of the logic function rather than an expanded single Karnaugh map. In most cases, data-input conditioning can be determined more rapidly with a multiple map representation where the number of variables in each map is equal to the number of data select inputs of the data selector.

The multiple mapping method is illustrated by the following examples.

Example 1
Logic function: $F = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}C$
Data Selector: SN54/74151 or SN54/74152

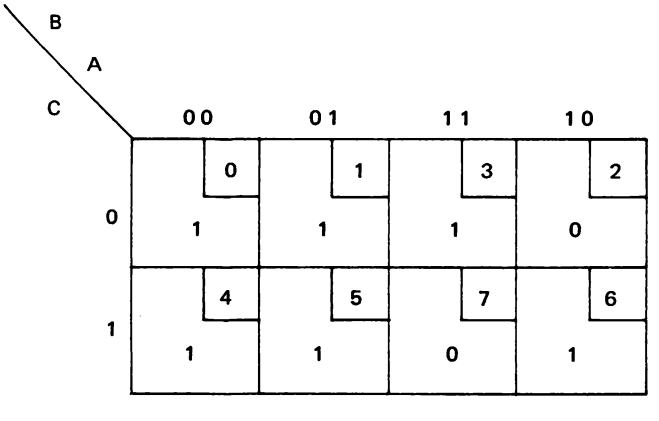


The conditioning signals to be used are

$D_0 = D_2 = D_5 = 1$

$D_1 = D_3 = D_4 = D_6 = D_7 = 0$

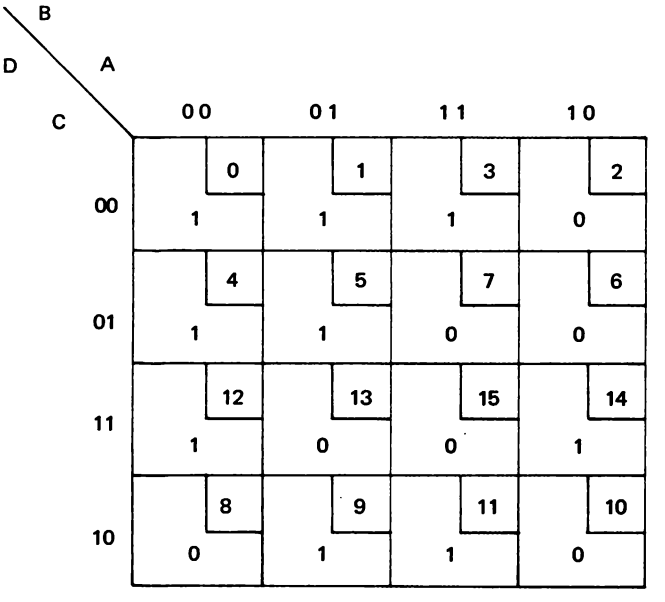
Example 2
Logic function: $F = \overline{B} + A\overline{C} + \overline{A}C$
Data Selector: SN54/74151 or SN54/74152



The conditioning signals to be used are

$D_0 = D_1 = D_3 = D_4 = D_5 = D_6 = 1$
$D_2 = D_7 = 0$

Example 3
Logic function: $F = A\overline{C} + \overline{A}CD + \overline{B}\overline{D}$
Data Selector: SN54/74150



The conditioning signals to be used are

$E_0 = E_1 = E_3 = E_4 = E_5 = E_9 = E_{11} = E_{12} = E_{14} = 1$
$E_2 = E_6 = E_7 = E_8 = E_{10} = E_{13} = E_{15} = 0$

Example 4
Logic Function: $F = A\overline{C} + \overline{A}CN + \overline{B}\overline{N}$
Data Selector: SN54/74151 or SN54/74152

The number of available data select inputs is 3. Therefore, 3-variable Karnaugh maps will be used. The number of variables in the desired logic function exceeds the number of available data select inputs by one excess-variable (N).

The logic function must be expanded to obtain an expression in which *all* minterms contain the excess-variable N. The minterm AC in the desired logic function does not contain the excess-variable N, and must be expanded as follows:

$$A\overline{C}(N + \overline{N}) = A\overline{C}N + A\overline{C}\overline{N}$$

The expanded logic function is then

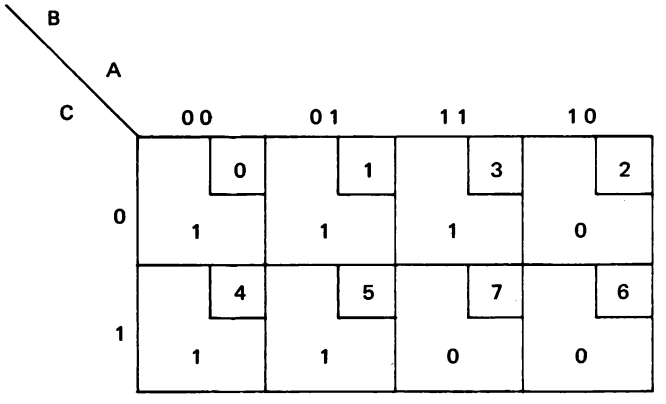
$$F = A\overline{C}N + A\overline{C}\overline{N} + \overline{B}\overline{N} + \overline{A}CN$$

The excess-variable N may appear in either one of two different states. Therefore, two maps are necessary to account for all possible combinations of the variables. The first map is valid for N = 0 or $\overline{N}$ = 1. Therefore, the

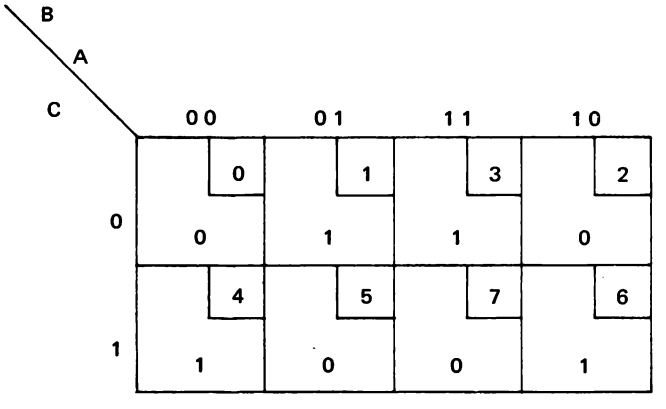
conditioning signals derived from this map have to be AND-ed with $\overline{N}$.

The second map is valid for N = 1 and the conditioning signals derived from this map must be AND-ed with N.

The total conditioning signal for the data-inputs is obtained by OR-ing the conditioning signals derived from identically numbered cells of both maps shown below.



$\overline{N} = 1$



$N = 1$

DATA–INPUT	MAP $\overline{N} = 1$	MAP N = 1	TOTAL
D_0	$1 \cdot \overline{N} = \overline{N}$	$0 \cdot N = 0$	$\overline{N} + 0 = \overline{N}$
D_1	$1 \cdot \overline{N} = \overline{N}$	$1 \cdot N = N$	$\overline{N} + N = 1$
D_2	$0 \cdot \overline{N} = 0$	$0 \cdot N = 0$	$0 + 0 = 0$
D_3	$1 \cdot \overline{N} = \overline{N}$	$1 \cdot N = N$	$\overline{N} + N = 1$
D_4	$1 \cdot \overline{N} = \overline{N}$	$1 \cdot N = N$	$\overline{N} + N = 1$
D_5	$1 \cdot \overline{N} = \overline{N}$	$0 \cdot N = 0$	$\overline{N} + 0 = \overline{N}$
D_6	$0 \cdot \overline{N} = 0$	$1 \cdot N = N$	$0 + N = N$
D_7	$0 \cdot \overline{N} = 0$	$0 \cdot N = 0$	$0 + 0 = 0$

The conditioning signals to be used are

$$D_0 = D_5 = \overline{N}$$

$$D_1 = D_3 = D_4 = 1$$

$$D_2 = D_7 = 0$$

$$D_6 = N$$

Example 5
Logic Function: $F = A\overline{C}NM + AB\overline{D}M + \overline{A}C + AD\overline{N}M + \overline{B}D\overline{N}\overline{M}$
Data Selector: SN54/74150

The number of data select inputs is 4 and consequently 4-variable Karnaugh maps must be used. The number of variables (6) in the desired logic function exceeds the number of available data select inputs by 2. The 2 excess-variables M and N may appear in 4 different combinations, which means that 4 Karnaugh maps are necessary to account for all possible combinations of the variables.

Map 1 is valid for: $\overline{M}\overline{N} = 1$
Map 2 is valid for: $M\overline{N} = 1$
Map 3 is valid for: $\overline{M}N = 1$
Map 4 is valid for: $MN = 1$

The conditioning signals derived from a map must be AND-ed with the combination of the excess-variables for which that map is valid. The total conditioning signals for the data inputs is obtained by OR-ing the separate conditioning signals derived from *equally* numbered cells of the 4 maps.

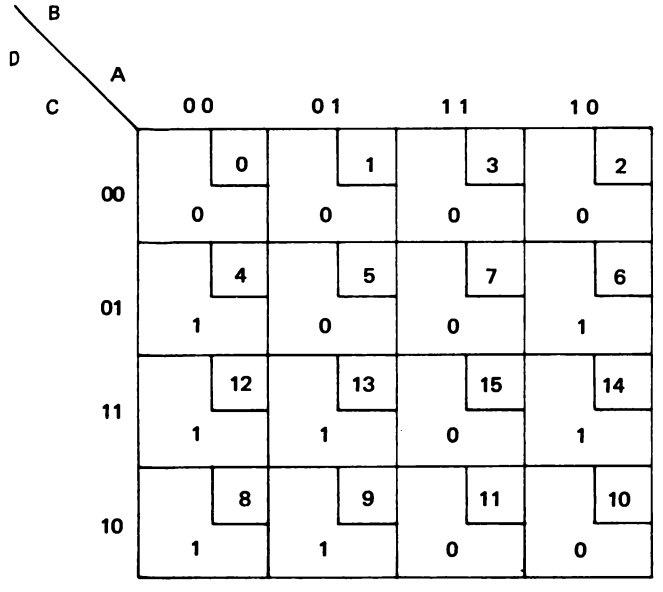
Again, the logic expression must be expanded to obtain an expression in which *all* minterms contain all excess-variables.

The minterms are expanded as follows:

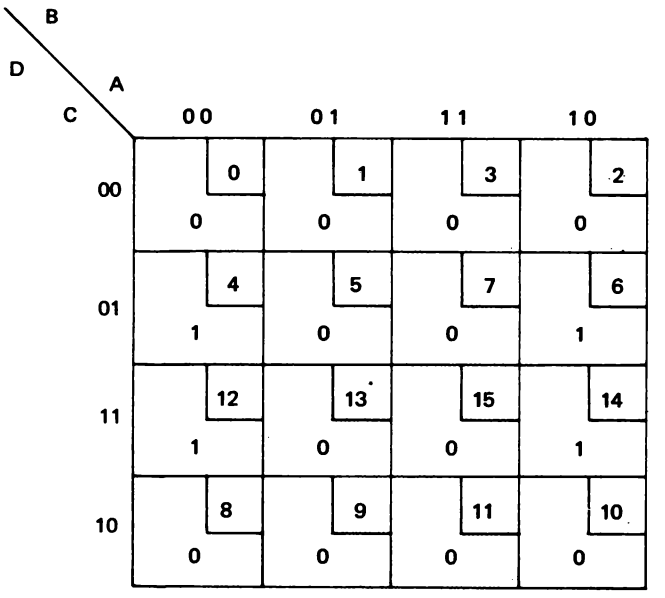
$$AB\bar{D}M = AB\bar{D}M\,(N + \bar{N}) = AB\bar{D}MN + AB\bar{D}M\bar{N}$$
$$\bar{A}C\,(\bar{M}\bar{N} + M\bar{N} + \bar{M}N + MN) = \bar{A}C\bar{M}\bar{N} + \bar{A}CM\bar{N} + \bar{A}C\bar{M}N + \bar{A}CMN$$

The resulting expanded logic function is

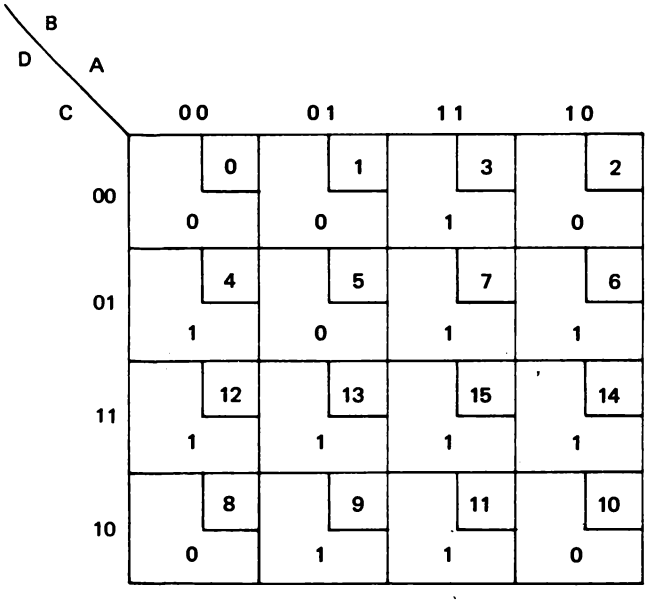
$$F = A\bar{C}MN + AB\bar{D}MN + AB\bar{D}M\bar{N} + \bar{A}C\bar{M}\bar{N} + \bar{A}CM\bar{N} + \bar{A}C\bar{M}N + \bar{A}CMN + ADM\bar{N} + \bar{B}D\bar{M}\bar{N}$$



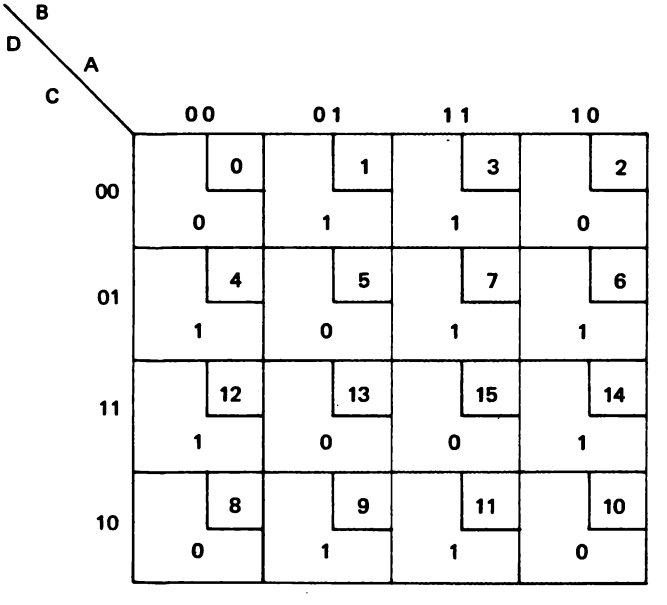
MAP 1; $\bar{M}\bar{N} = 1$



MAP 3; $\bar{M}N = 1$



MAP 2; $M\bar{N} = 1$



MAP 4; $MN = 1$

DATA– INPUT	MAP 1 $\overline{M}\overline{N} = 1$	MAP 2 $M\overline{N} = 1$	MAP 3 $\overline{M}N = 1$	MAP 4 $MN = 1$	TOTAL
E_0	$0 \cdot \overline{M}\overline{N} = 0$	$0 \cdot M\overline{N} = 0$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	0
E_1	$0 \cdot \overline{M}\overline{N} = 0$	$0 \cdot M\overline{N} = 0$	$0 \cdot \overline{M}N = 0$	$1 \cdot MN = MN$	MN
E_2	$0 \cdot \overline{M}\overline{N} = 0$	$0 \cdot M\overline{N} = 0$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	0
E_3	$0 \cdot \overline{M}\overline{N} = 0$	$1 \cdot M\overline{N} = M\overline{N}$	$0 \cdot \overline{M}N = 0$	$1 \cdot MN = MN$	$M\overline{N} + MN = M$
E_4	$1 \cdot \overline{M}\overline{N} = \overline{M}\overline{N}$	$1 \cdot M\overline{N} = M\overline{N}$	$1 \cdot \overline{M}N = \overline{M}N$	$1 \cdot MN = MN$	$\overline{M}\overline{N} + M\overline{N} + \overline{M}N + MN = 1$
E_5	$0 \cdot \overline{M}\overline{N} = 0$	$0 \cdot M\overline{N} = 0$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	0
E_6	$1 \cdot \overline{M}\overline{N} = \overline{M}\overline{N}$	$1 \cdot M\overline{N} = M\overline{N}$	$1 \cdot \overline{M}N = \overline{M}N$	$1 \cdot MN = MN$	$\overline{M}\overline{N} + M\overline{N} + \overline{M}N + MN = 1$
E_7	$0 \cdot \overline{M}\overline{N} = 0$	$1 \cdot M\overline{N} = M\overline{N}$	$0 \cdot \overline{M}N = 0$	$1 \cdot MN = MN$	$M\overline{N} + MN = M$
E_8	$1 \cdot \overline{M}\overline{N} = \overline{M}\overline{N}$	$0 \cdot M\overline{N} = 0$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	$\overline{M}\overline{N}$
E_9	$1 \cdot \overline{M}\overline{N} = MN$	$1 \cdot M\overline{N} = M\overline{N}$	$0 \cdot \overline{M}N = 0$	$1 \cdot MN = MN$	$\overline{M}\overline{N} + M\overline{N} + MN = M + \overline{N}$
E_{10}	$0 \cdot \overline{M}\overline{N} = 0$	$0 \cdot M\overline{N} = 0$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	0
E_{11}	$0 \cdot \overline{M}\overline{N} = 0$	$1 \cdot M\overline{N} = M\overline{N}$	$0 \cdot \overline{M}N = 0$	$1 \cdot MN = MN$	$M\overline{N} + MN = M$
E_{12}	$1 \cdot \overline{M}\overline{N} = \overline{M}\overline{N}$	$1 \cdot M\overline{N} = M\overline{N}$	$1 \cdot \overline{M}N = \overline{M}N$	$1 \cdot MN = MN$	$\overline{M}\overline{N} + M\overline{N} + \overline{M}N + MN = 1$
E_{13}	$1 \cdot \overline{M}\overline{N} = \overline{M}\overline{N}$	$1 \cdot M\overline{N} = M\overline{N}$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	$\overline{M}\overline{N} + M\overline{N} = \overline{N}$
E_{14}	$1 \cdot \overline{M}\overline{N} = \overline{M}\overline{N}$	$1 \cdot M\overline{N} = M\overline{N}$	$1 \cdot \overline{M}N = \overline{M}N$	$1 \cdot MN = MN$	$\overline{M}\overline{N} + M\overline{N} + \overline{M}N + MN = 1$
E_{15}	$0 \cdot \overline{M}\overline{N} = 0$	$1 \cdot M\overline{N} = M\overline{N}$	$0 \cdot \overline{M}N = 0$	$0 \cdot MN = 0$	$M\overline{N}$

The conditioning signals to be used are:

$$E_0 = E_2 = E_5 = E_{10} = 0$$

$$E_1 = MN$$

$$E_3 = E_7 = E_{11} = M$$

$$E_4 = E_6 = E_{12} = E_{14} = 1$$

$$E_9 = M + \overline{N}$$

$$E_8 = \overline{M}\overline{N}$$

$$E_{13} = \overline{N}$$

$$E_{15} = M\overline{N}$$

Examples 4 and 5 show that if a "1" appears in *equally* numbered cells of *all* maps, that particular conditioning signal is independent of all the excess-variables and is a logical "1". Similarly, if a "0" appears in *equally* numbered cells of *all* maps, that particular conditioning signal is independent of the excess-variables and is a logical "0".

Séries 15 300
High Noise Immunity logic
(B 119)

SERIES 15300 HIGH NOISE IMMUNITY LOGIC

By
David A. Bonham

High Noise Immunity Logic, HNIL, is a DTL family of logic designed for use in areas of high electrical noise. The high noise immunity is obtained by having a threshold which is typically 5.5 V. This gives a typical dc noise immunity in both states of at least 4.5 V. The supply voltage can be anywhere in the range 11.5 V to 16.0 V, although 12 V or 15 V will be common choices because one or the other of these two voltages will often be available elsewhere within a system. A typical gate dissipation is 35 mW. Maximum propagation delays are of the order of 40 ns for high to low output transitions and 110 ns for low to high.

The standard series of devices is available in both plastic and ceramic packages and has an operating temperature range of from −30°C to +85°C. Full military temperature range devices are also available.

DEVICE CHARACTERISTICS

Basic Circuitry of Gates

The gates are DTL with variations of open collector and resistive and active pullup. They have the well known advantages of DTL. Some of these advantages are:

1. Inputs can be expanded at will, by adding diodes. A dual 5 input diode expander is available for this purpose.
2. The inputs have a very high breakdown voltage and so will tolerate input transients.
3. The open collector gates (and sometimes resistive pullup gates) can be wired-AND. This reduces package count and also makes it possible for them to drive data paths. Wire-AND is explained in more detail later in this report.
4. Having a low gain bandwidth they will tolerate slow input edges.
5. There are no current spikes at switching edges even with active pullup devices. (The active pullup is not a true totem pole and both transistors can never be switched on together.)

Figure 1 shows the circuit of the basic HNIL gate. It is a form of modified DTL. The high threshold is obtained

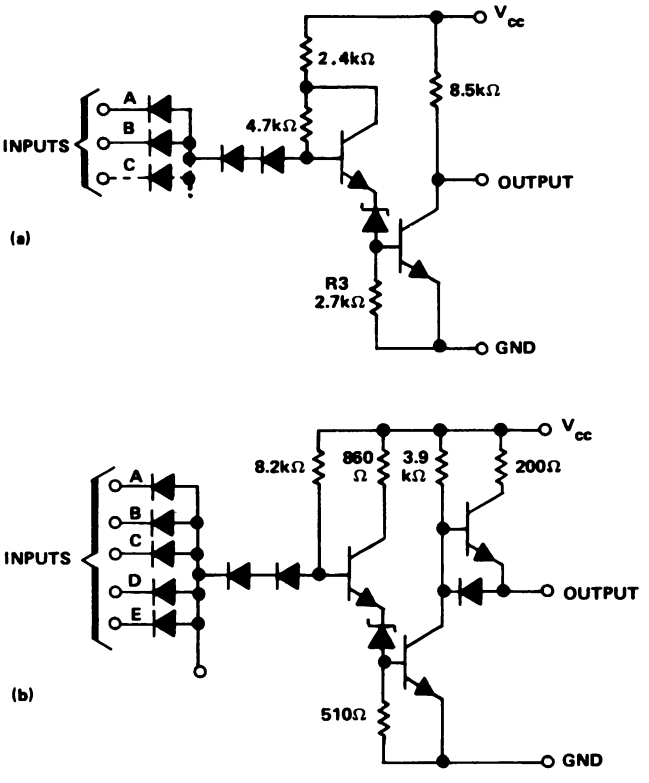


FIGURE 1. Basic HNIL Gate (a). Basic HNIL Gate with Active Pullup (b).

by using the reverse breakdown of an emitter-base junction V_{EB}. The value of the threshold is:

$$V_T = V_{EB} + 2\,V_{BE} - 3\,V_F \qquad (1)$$

The reverse emitter-base junction has a breakdown of about 6.3 V and a temperature coefficient of about 2 mV/°C, giving an overall threshold temperature coefficient of approximately 2.5 mV/°C, after considering the diode junctions.

The first transistor is nonsaturating. It sources a higher current than would the diode of conventional DTL, so that there is more base drive available to the output transistor. This means that R3 can be smaller and the h_{FE} need not be so high.

The input characteristic of a HNIL gate is shown in Figure 2. Aside from the threshold, the most important features are the positive breakdown voltage and the clamping action. The breakdown voltage will usually be between 35 V and 50 V, so that any transients will not blow up the diode inputs.

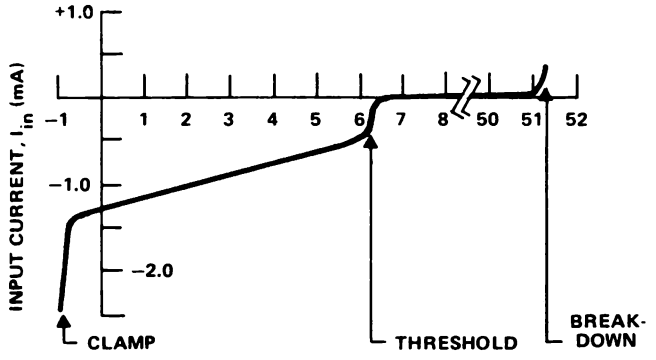


FIGURE 2. Typical Input Characteristic of Basic HNIL Gate

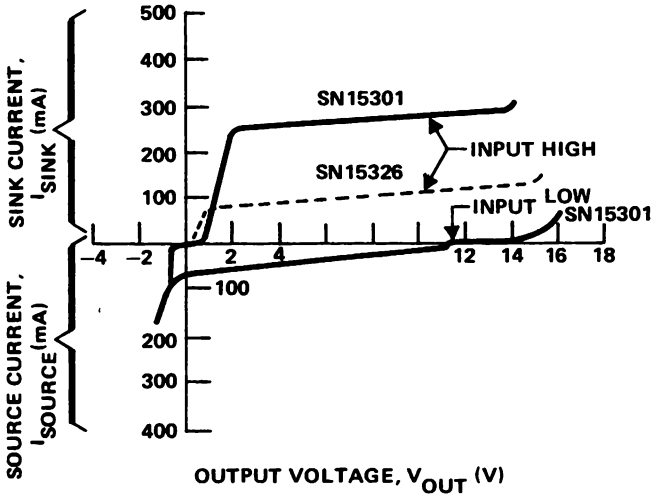


FIGURE 3. Typical Output Characteristics of a HNIL Buffer

The inputs exhibit a clamp action to negative input voltages. This is because of the way the diode inputs are fabricated. A by-product of their construction is that a substrate diode is formed between the input terminal and ground. It has a slope impedance of about 70 Ω so that it will match undershoot up to the logical "0" voltage for lines of 100 Ω to 150 Ω impedance.

The output characteristics of a HNIL buffer are shown in Figure 3. Its high voltage swing and its ability to sink 60 mA and source 15 mA show that the devices will often be able to drive external loads without interface circuitry. For comparison, the output characteristic of an open collector gate is also shown in Figure 3.

Figure 4 shows the transfer characteristic of a HNIL gate. It can be seen how sharp the change over is from one output state to the other. With a typical device it occurs for

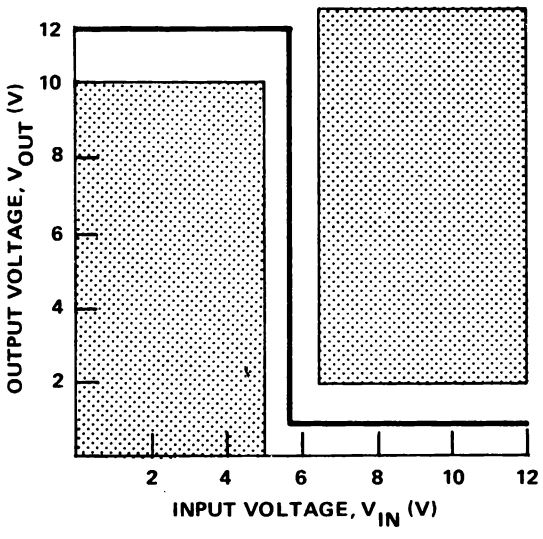


FIGURE 4. Typical Transfer Characteristics of a HNIL Gate

a 200 mV change at the input. This gives the maximum noise margins for the given voltage swing.

The variations of the characteristics of a basic HNIL gate with different supply voltages and temperatures are indicated in Figure 5, with important variations shown quantitatively.

Fan-Out

Fan-out is the number of devices that any one gate can drive without jeopardizing the noise margin. All HNIL gates have similar inputs. Differences usually lie in the output capability. Buffers have a worst-case fan-out of 20 or 25. Devices with active pullup, and other devices have a worst-case fan-out of 5.

An example, the SN15333, is shown in the "0" state in Figure 6. In this example:

$$I_{OL} = 15 \text{ mA} @ V_{OL} = 0.8 \text{ V max.}$$

The gate will sink 15 mA in the "O" state.

$$I_{IL} = -2.6 \text{ mA max} \qquad (2)$$

The maximum input current to the next gate is −2.6 mA each.

$$\text{Fan-out} = \frac{15}{2.6} => 5$$

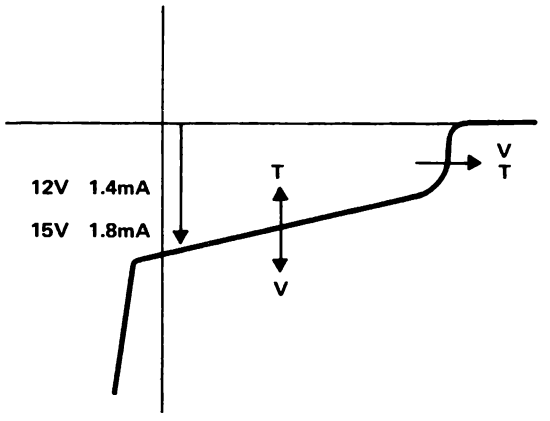
5 is the fan-out in the "O" state.

The SN15333 is shown in the "1" state in Figure 7. In this example:

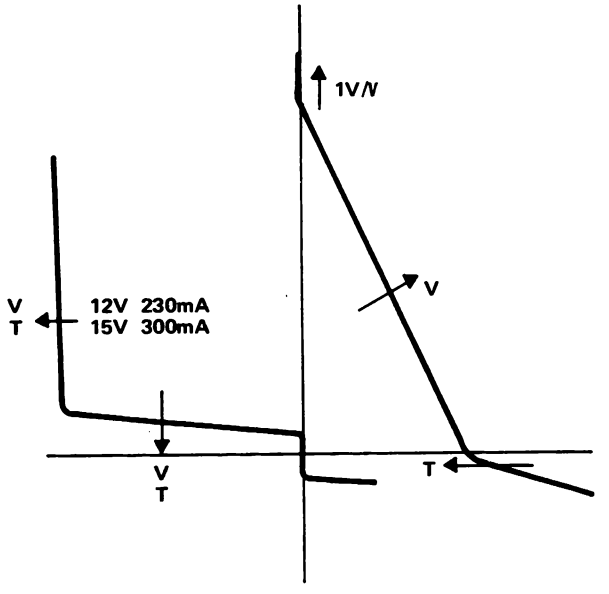
$$I_{IH} = 5\ \mu\text{A} @ V_{IH} = 10.5 \text{ V} \qquad (3)$$

$$V_{CC} = 12 \text{ V}$$

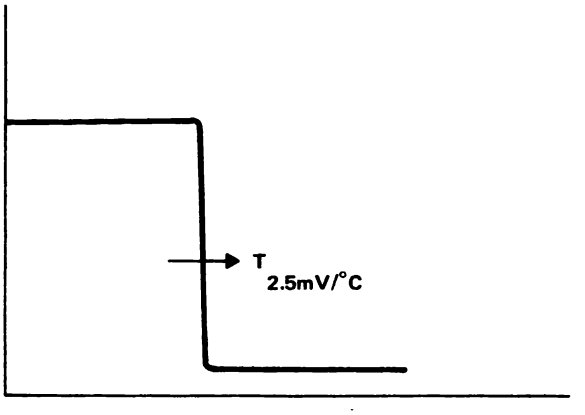
$$R = 9.1 \text{ k}\Omega$$



(a) INPUT CHARACTERISTIC



(b) OUTPUT CHARACTERSTIC



(c) TRANSFER CHARACTERISTIC

FIGURE 5. Variations of Characteristics of a Basic HNIL Gate with Different Supply Voltages and Temperatures

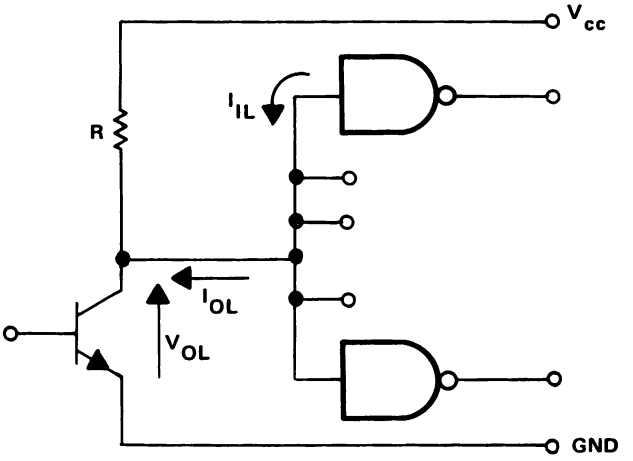


FIGURE 6. Fan-Out of a HNIL SN15333 in the "0" State

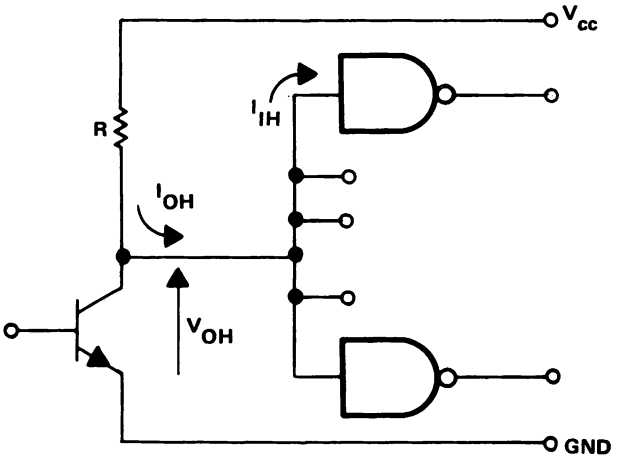


FIGURE 7. Fan-Out of a HNIL SN15333 in the "1" State

$$I_{OH} = 25\ \mu A\ @\ V_{OH} = 11.7\ V$$

or

$$I_{OH} = 50\ \mu A\ @\ V_{OH} = 11.5\ V$$

$$\text{Fan-out} = \frac{25}{5} = 5\ @\ V_{OH} = 11.7\ V$$

$$\text{Fan-out} \triangleq \frac{50}{5} = 10\ @\ V_{OH} = 11.5\ V$$

These are worst case considerations and, in practice, "1" state fan-out will always be many times higher because the I_{IH} will be less than 1 μA.

Table 1 shows the voltage levels in both states at input and output. Differencing the high state voltages gives a 3.5 V worst case and a 5.5 V typical noise margin. For the low state the margin is 4.2 V and 5.5 V.

Table 1. Voltage Levels in Both States at Input and Output

	Min	Typ	Max
V_{OH}	10.0 V	11.5 V	
V_{OL}		0.5 V	0.8 V
V_{IH}	6.5 V	6.0 V	
V_{IL}		6.0 V	5 V

AC Noise Immunity

As the noise pulse width decreases, the pulse height required to affect the gate output increases. Thus the circuit is more immune to noise as the pulse width is reduced. Figure 8 shows the relationship.

Output Speed

The effect of fan-out on propagation delays is shown in Figure 9. Figure 10 shows the effect of capacitive load on the propagation delays of a buffer gate.

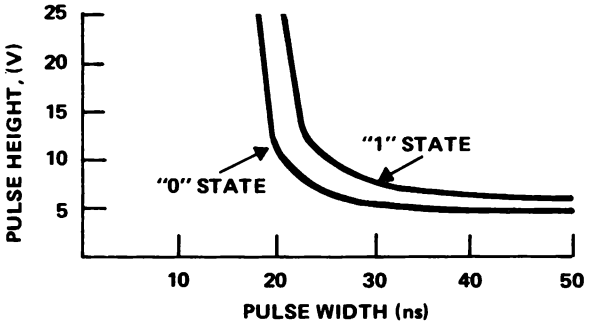


FIGURE 8. Noise Immunity versus Pulse Width for HNIL Gate

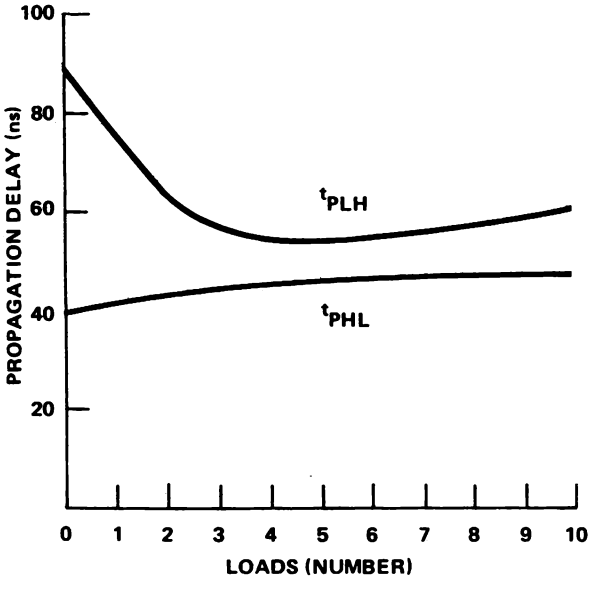


FIGURE 9. Propagation Delay versus Fan-out for HNIL SN15326

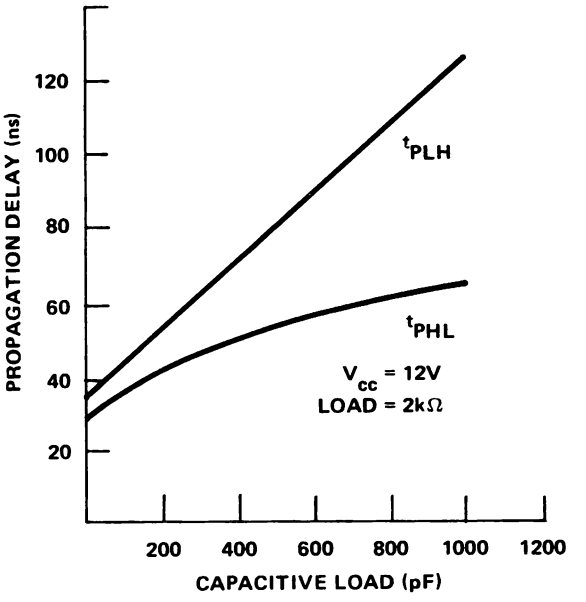


FIGURE 10. Propagation Delay versus Capacitive Load for HNIL SN15301

Input Speed

Usually with a logic family, pulse edges have to be better than a certain speed to ensure that the output of a gate being driven does not oscillate during the input transition.

A digital gate becomes an amplifier as the input crosses the threshold. However HNIL is deliberately designed to be slow and have a low bandwidth. Any small feedback capacitance does not, therefore, cause the gate to go unstable. Thus HNIL gates will tolerate slow ramps.

SYSTEM CONSIDERATIONS

Line Driving

The HNIL buffer gates are excellent for line driving, with the high voltage swing providing good noise immunity. In the "1" to "0" transition the waveform at the driver switches immediately down to less than 2 V. The receiving diode impedance matches the line very well so that after an undershoot at the receiver, the waveforms at both ends settle. An important feature of the output characteristic is that at $V_{OL} = 0$ V, $I_O = 0$ mA. This means that a positive overshoot cannot happen on this transition.

The line impedance is chosen after considering the "0" to "1" transition. Typically, with a 75 Ω line the receiver waveform will cross the threshold immediately. However, a line of 100 Ω (or more) characteristic impedance should be used to accommodate conditions of low V_{CC} and for a high output impedance.

Figure 11 shows the input and output characteristics arranged as a Bergeron diagram. Figure 12, which is derived from Figure 11, shows the typical waveforms which will occur at the transmitting and receiving gates when driving 100 Ω and 150 Ω lines. These considerations are for lines

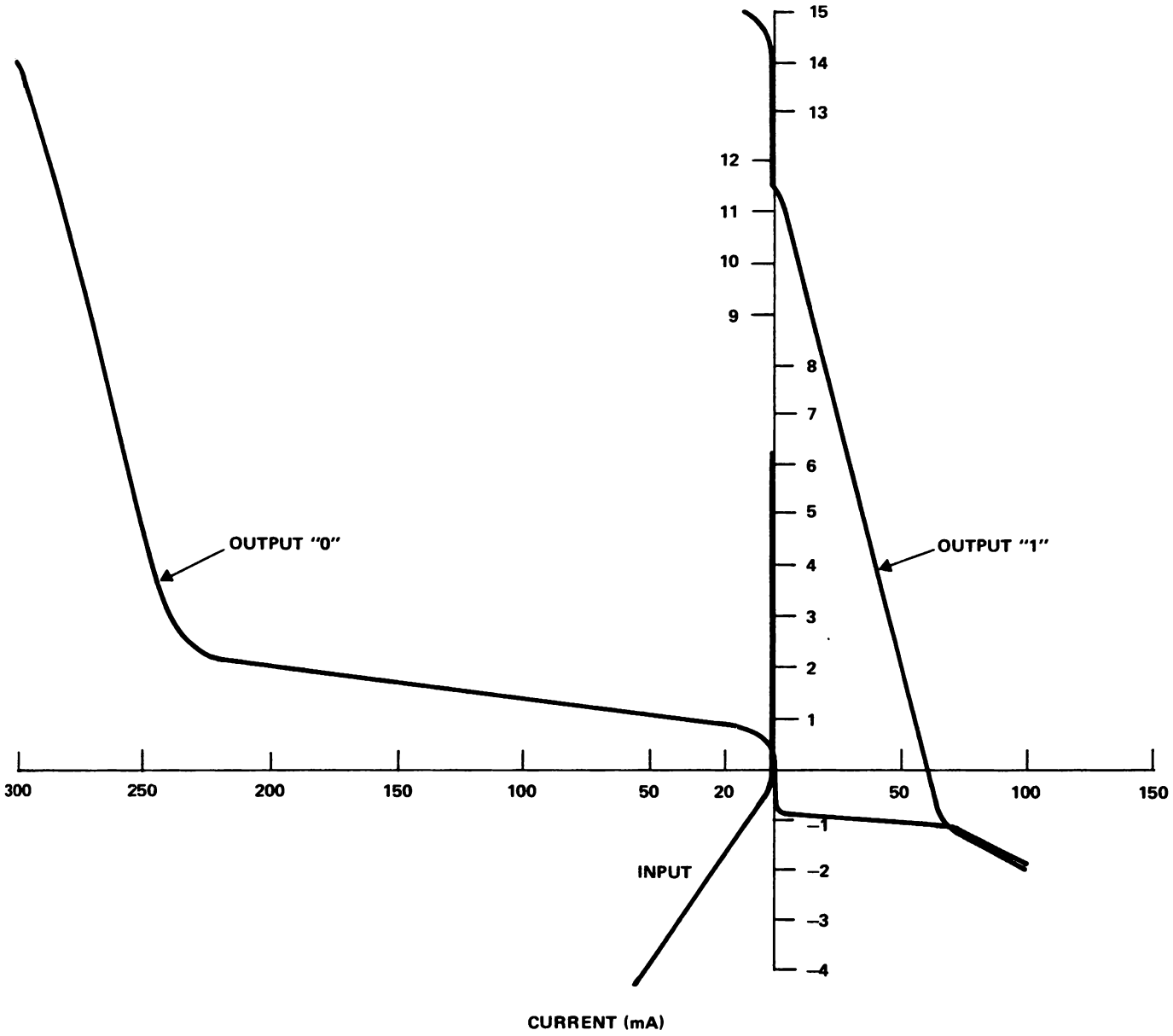


FIGURE 11. Input and Output Characteristics of HNIL SN15301 Arranged as a Bergeron Diagram (V_{CC} = 12 V)

of controlled impedance. However, it is preferable, for reasons of economy, to drive single, open wires.

Open Wires

Because they look like a transmission line of high characteristic impedance, open wires can cause problems on the "0" to "1" transition. If the output impedance of the logic gate is too low there will be an overshoot which can cause input breakdown at the receiver. If the output impedance is too high then it will take several propagation delays along the line and back before the receiver threshold is passed. Ideally, an output impedance should be the same as the line. With HNIL, the wide voltage swing compared with the threshold window plus the high input voltage tolerance allows a wide range of output impedances while maintaining correct operation. The active pullup devices will drive open lines as will open collector devices with a resistive pullup of 300 Ω. The latter, however, implies that the gate must be capable of sinking at least 40 mA in the "0" state.

These considerations for both transmission lines and open lines assume that the line is going to be of such a length that the rise or fall time of the driver is shorter than twice the propagation delay along the line. Because the fastest edge with HNIL will be about 25 ns, this means that only reflection phenomena for lines longer than 3 metres will have to be considered.

Crosstalk

It can be shown to a simple approximation that:[1]

$$V_{in} = V_S (1.5 + Z_m/Z_0) (1 + Z_1/Z_0) \qquad (4)$$

1. D. Bonham, *Schottky TTL*, Texas Instruments Application Report B93, p. 11.

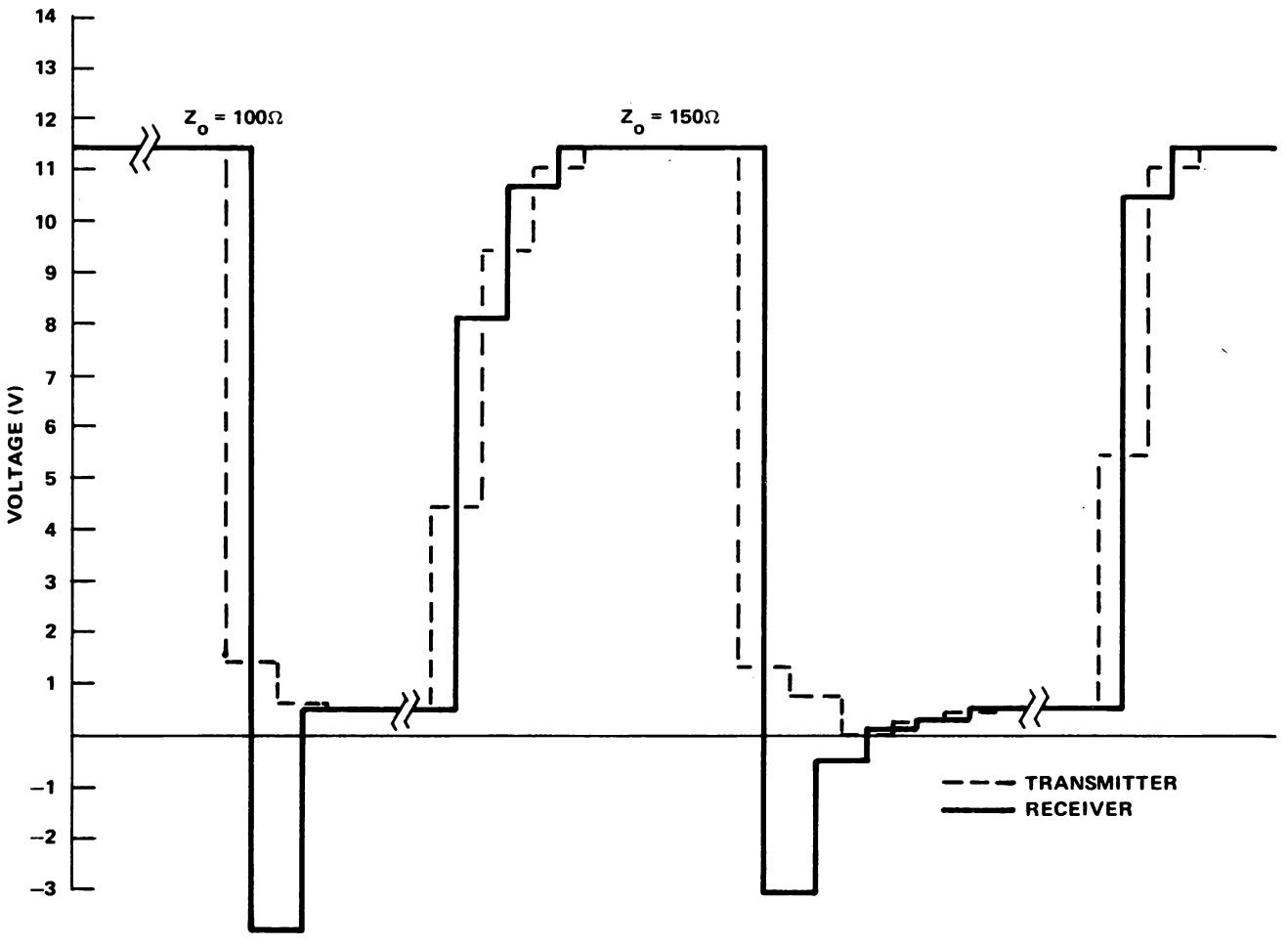


FIGURE 12. Typical Waveforms Which Occur at the Transmitting and Receiving Gates When Driving 100 Ω and 50 Ω Lines

where V_{in} is the voltage induced at the input to gate number 4 by the switching of gate 1 as in Figure 13. If:

the voltage swing,	$V_S = 10$ volts	
the gate output impedance,	$Z_1 = 15\ \Omega$	
the line impedance,	$Z_0 = 100\ \Omega$	(5)
the coupling impedance,	$Z_m = 200\ \Omega$	
these values give,	$V_{in} = 2.5$ volts	

which is much less than the noise margins for this logic family.

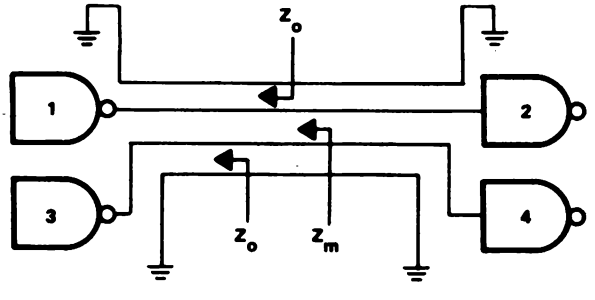


FIGURE 13. Crosstalk in HNIL

Noise Coupling Into Short Interconnections Between Gates

If one takes two gates, one driving the other, it is the driver impedance which is the lower. Therefore, the value of noise coupled into a short connection between two gates is determined by the output impedance. Referring to Figure 14 it can be seen that the voltage coupled by stray capacitance V_{in} is given by:

$$V_{in} = \frac{V_S R}{R + X_C} \qquad (6)$$

where X_C is reactance of capacitor

As the logic is immune to 4.0 V at the input, the noise source can have an amplitude given by:

$$V_S = 4.0 \left(1 + \frac{X_C}{R}\right) \qquad (7)$$

before malfunction occurs.

For an open collector gate using a 1 V pullup resistor, with a stray capacitance of 0.5 pF coupling to a source of 0.5 MHz, $V_S = 2500$ V. In other words, there can be a

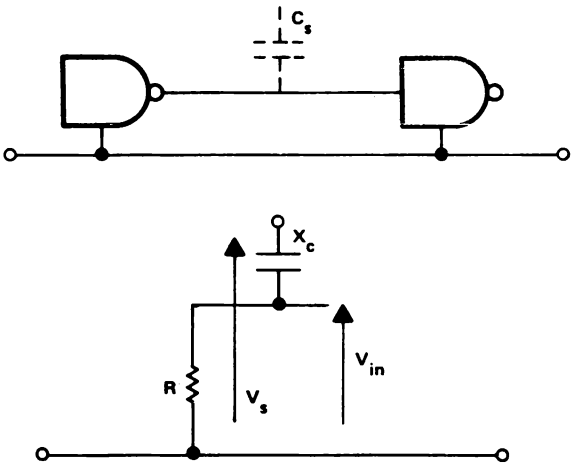


FIGURE 14. Noise Coupling in HNIL

2500 V noise source with these conditions before the logic will be upset.

Another way of estimating the noise immunity of logic is to see what transient interference it will tolerate rather than sinusoidal as discussed in the preceding paragraph. Consider a situation with the same conditions of 0.5 pF stray capacitance, 1 kΩ output impedance and 4 V noise immunity.

To have 4 V across the 1 kΩ impedance there must be 4 mA through the C_S and 1 kΩ.

$$I = C \frac{dV}{dt}$$

$$4\ mA = C_S \frac{dV}{dt} \tag{8}$$

$$\frac{dV}{dt} = \frac{4 \times 10^{-3}}{0.5 \times 10^{-12}} \times 10^{-6}\ V/\mu s$$

$$= 8000\ V/\mu s$$

Thus, a gate as above, will tolerate a transient of up to 8000 V/μs.

Interfacing

There is a pair of circuits in the 15300 series which will interface an HNIL part of a system with a low level logic system. One circuit, the 15361, converts from HNIL to either TTL, DTL, or RTL. There are inverting and non-inverting inputs.

The other circuit, the 15362, interfaces from low level logic such as TTL, DTL, or RTL to HNIL with a choice of an inverted or non-inverted input. It can even be driven by Low Power TTL.

The substantial output of the HNIL buffers allows many external loads to be driven directly. They will switch 16.5 V and sink 60 mA or source 15 mA. This will be enough for many relays. (Physically the diode should be mounted across the coil terminals and must be able to handle the normal coil current.) Lamp driving is more stringent than it would at first appear. This is because the resistance of a lamp when it is cold is much less than its operating resistance. It may be as little as a twentieth of its hot value. This causes a switch-on surge. The output transistor of this HNIL will tolerate this without going into breakdown, so there is little need to use a current limiting resistor, except perhaps, to enhance the life of the bulb.

Some indication of the ruggedness of the output transistors is shown by the fact that the gate output, when in the "0" state, may be taken up to the supply voltage or thereabouts. Some devices will stand this mistreatment indefinitely, although the buffer devices, which may be conducting 250 mA, may over-dissipate after about a second.

Higher voltage and current loads can be driven with the aid of a single extra transistor as shown in Figures 15(a) and 15(b). With a suitable transistor, such as a TIP 32, the circuit in Figure 15(b) will drive 1 amp. Of course many other variations are possible.

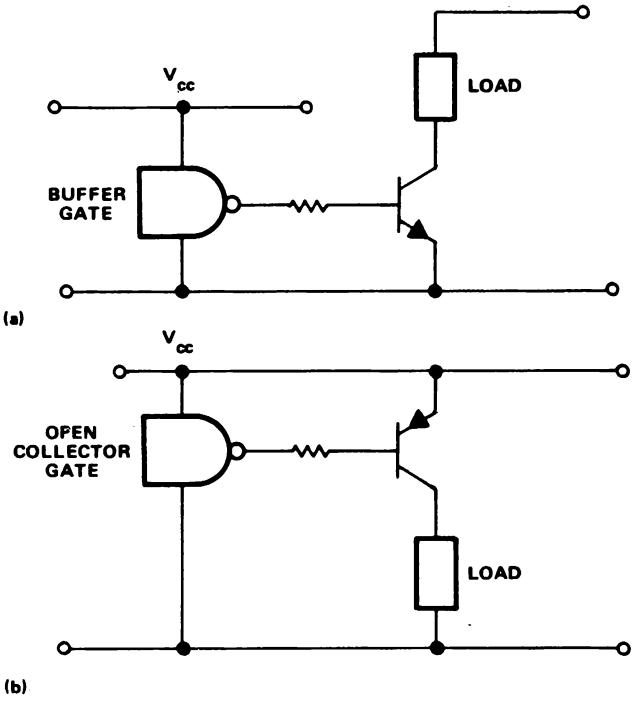


FIGURE 15. Two Interfacing Circuits for Driving Higher Voltage and Current Loads

Decoupling

As mentioned previously, the design of the active pullup is such that current spikes are not produced on the power line at pulse edges. The purpose of decoupling with HNIL is to supply any difference in supply current required for different logic states. Therefore, there is not the necessity to decouple as vigorously as with TTL since the differences on average tend to cancel, whereas spikes always add. Furthermore, half a volt on the line has only a fractional effect on the noise margin whereas in low level

logic it would have completely overcome the noise margin. A capacitance of 5 μF per board is all that is needed in most systems.

Ground Line

The average gate current for HNIL is 3 or 4 mA. For TTL SSI it is 3 mA. Thus, any impedance in the ground path (or voltage line) will have the same effect for a given number of gates, in terms of dc voltage; but the effect this dc voltage will have on the noise margin will be 4 or 5 times less with HNIL.

The transient currents of HNIL are much smaller than TTL and thus, the ac ground and supply noise have even less effect.

Unused Inputs

There are several alternative ways of dealing with unused inputs. They may be taken to the supply line directly. They may be connected to the line via a current limiting resistor. This avoids input breakdown if there are likely to be large voltage spikes on the line. Or they can be paralleled with used inputs. This adds one to the fan-out of the "1" state but nothing to the "0" state fan-out.

Expander inputs should be left open circuit when not used.

Wired-AND

Open collector gates can be wired-AND. The outputs of the gates are all taken to the same pullup resistor and this point is then used as if it were the output of a single gate. Logically what happens is that if any one of the gates goes low, this point is taken low, and it is high only if all the gate outputs are high. Therefore, the function which is actually performed for the cost of only one resistor is positive ANDing.

Two opposing rules must be observed when choosing the value of the pullup resistor. They are to ensure that both the logical zero and logical one states can be obtained.

Consider the case of fan-in from M outputs and fan-out to N inputs. Figure 16 shows the arrangement of the gates.

In the logical "1" state when all gates are high, the pullup resistor has to supply the leakage current to the gate inputs and outputs. Typically, the output leakage will be about 10 μA and the input 1 μA. The output must remain above the minimum logical "1" level. Therefore:

$$V_{CC_{min}} - V_{OH} \geq R\,(10\,M + N) \times 10^{-6} \qquad (9)$$

This gives the first rule

$$R \leq \frac{(V_{CC_{min}} - V_{OH}) \times 10^{6}}{(10\,M + N)} \qquad (10)$$

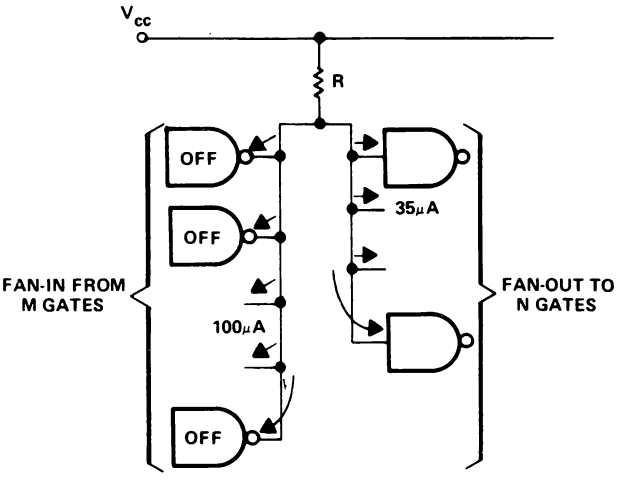


FIGURE 16. Wiring-AND in "1" State

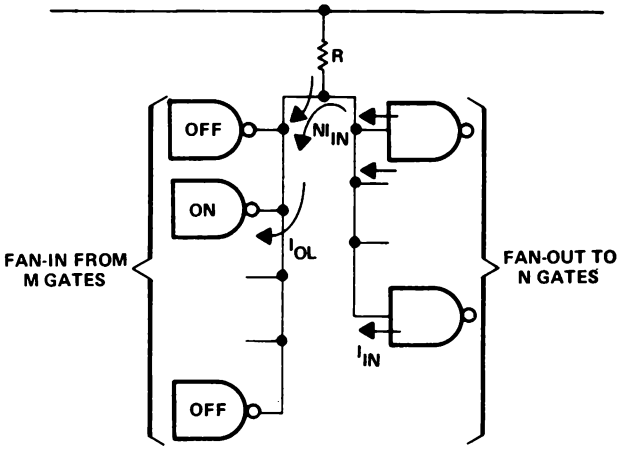


FIGURE 17. Wiring-AND in "0" State

In the logical "0" state, shown in Figure 17, the worst case is when only one gate is low and it has to sink the current from the N inputs and the resistor. Therefore:

$$I_{OL} \geq \frac{(V_{CC\ max} - V_{OL})}{R} + N.I_{IL} \qquad (11)$$

This gives the second rule

$$R \geq \frac{V_{CC\ max} - V_{OL}}{I_{OL} - N.I_{IL}} \qquad (12)$$

From these two equations for R, the minimum and maximum values for the pullup resistor can be calculated for any desired fan-out. Values near to R_{min} should be used for best noise immunity; although raising the resistance will slightly reduce the power consumption.

There is one specific example of wiring-AND which is of great use. It is the formation of a multi-input NOR gate from open collector inverters. The outputs of the inverters are simply taken to a common pullup resistor and the overall function from their inputs to this output is a positive NOR as in Figure 18.

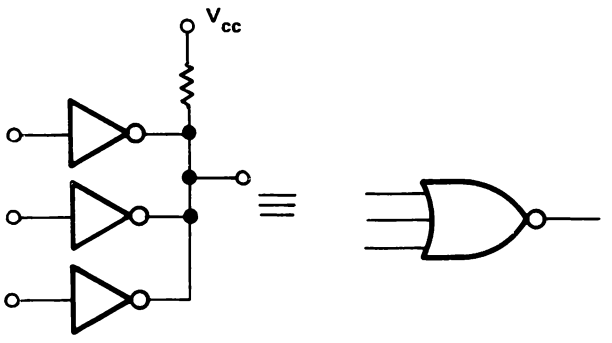


FIGURE 18. An Equivalent NOR Gate

APPLICATIONS OF HNIL

HNIL is ideally suited for industrial and consumer applications. It has an inherent high noise immunity without the need for screening and filtering. Thus, it is the best economic alternative in a small to medium system where screening and similar techniques would otherwise form a large percentage of the unit cost. Furthermore, its output capability will reduce the need for extra interface circuits. Typical applications include control circuitry in appliances, numerical-control machines, process control, materials handling, electrostatic equipment, automotive systems, aircraft instrumentation, medical electronics, and others.

The excellent line driving ability of HNIL, together with its noise immunity, suggests its use as an interface between pieces of equipment. In a low level logic system the difference in ground potentials between sections of equipment can cause a problem with noise margins. Using HNIL low level interfaces such as line drivers and receivers shown in Figure 19 overcomes this problem very simply.

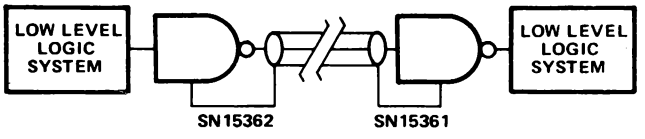


FIGURE 19. HNIL Circuits Used for Equipment Interfacing

Table 2. TI Series 15300 Product Spectrum

Device	Function
15301	Dual 5 Input Buffer (Active Pullup)
15302	Quad 2 Input Buffer (Open Collector)
15303	Quad 2 Input Buffer (Resistive Pullup)
15312	Dual J-K Flip Flop
15321	Quad 2 Input Gate (Active Pullup)
15322	Dual 5 Input Gate (Active Pullup)
15323	Quad 2 Input Gate (Open Collector)
15324	Quad 2 Input Gate (Resistive Pullup)
15325	Dual 2, Dual 3 Input Gate (Active Pullup)
15326	Dual 2, Dual 3 Input Gate (Resistive Pullup)
15331	Dual 5 Input Expander
15332	Hex Inverter (Open Collector)
15333	Hex Inverter (Resistive Pullup)
15334	Hex with Strobe (Open Collector)
15335	Hex with Strobe (Resistive Pullup)
15336	14-Pin Version of 15332
15342	Dual Monostable Multivibrator
15361	Dual Input Interface High to Low Level
15362	Dual Output Interface Low to High Level
15370	Quad Latch

Fast Multipliers Using TTL read only memories (CA 172)

FAST MULTIPLIERS USING TTL READ ONLY MEMORIES

by
Gene Cavanaugh

One of the most common and at the same time slowest operations in a computing machine is multiplication. Even in those cases where multiplications are made to cover many machine cycles, the number of multiplications required often imposes drastic limitations on machine throughput.

This application report deals specifically with a means of performing high speed multiplication utilizing currently available TTL Read-Only-Memory products plus Series 54/74 TTL MSI functions to allow a high performance and economical solution to binary multiplication. However, before exploring the method for multiplication with TTL ROMs, it is important to understand the fundamental algorithm of binary multiplication and discussion begins with a review of those fundamentals.

BASICS OF BINARY MULTIPLICATION

Binary multiplication can be expressed as a two step operation: ANDing the multiplicand with the multiplier one bit at a time, and adding. Furthermore, since adding is commutative (not dependent on the order in which made) the ANDed subproducts can be combined in any order that observes the binary weight of each bit.

Another fact, not so obvious, is that groups of multiplier and multiplicand bits can also be ANDed, summed, and combined. As Figure 1 shows, the effect is the same whether the bits are ANDed and summed in complete groups, or whether they are ANDed, summed in subgroups, and then the subgroups added. The only difference is in the way the subproducts are added, due to the difference in the weight accorded the binary bits in each method. "Weight" means the exponent or power of each bit; for example, if the MSB in a 4 bit multiplicand (2^3) is ANDed with the 2nd bit (2^1) in a multiplier, the result is a (2^3 X 2^1 = 2^{3+1} = 2^4) 2^4 bit (or 4th power bit).

For example, consider the binary multiplication of 15 X 15 as illustrated in Figure 1. First you will note that the process is identical with decimal multiplication; that is, one integer is multiplied by another to obtain a "subproduct," and the result is added to other "subproducts" to obtain the product. As discussed before, integer multiplication of binary numbers results in the ANDing process; that is, 0 X 0 is 0, 0 X 1 or 1 X 0 is 0, and 1 X 1 is 1, which is the truth table for an AND function. Multiplication is often accomplished by developing an array of AND functions and adding them with the proper binary

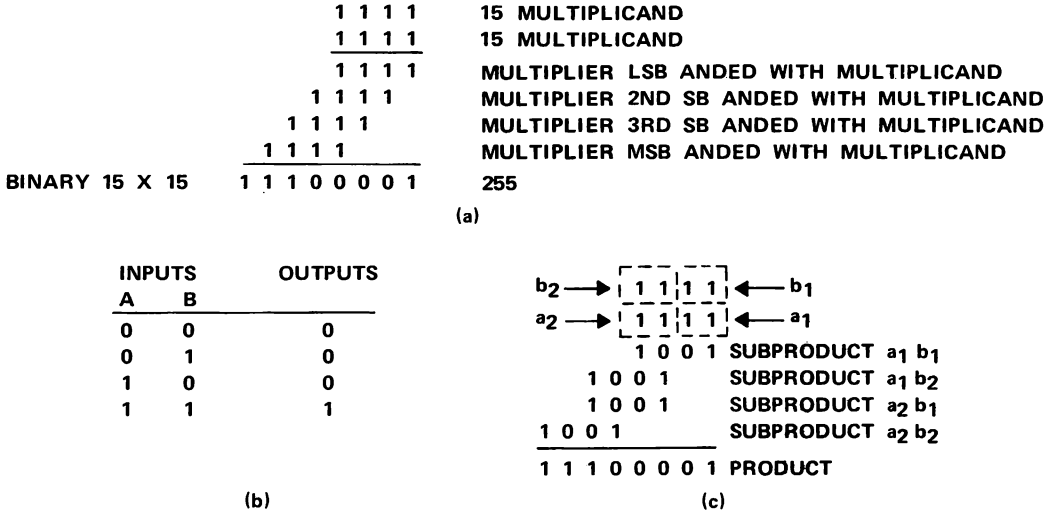

1 1 1 1 15 MULTIPLICAND
1 1 1 1 15 MULTIPLICAND
1 1 1 1 MULTIPLIER LSB ANDED WITH MULTIPLICAND
1 1 1 1 MULTIPLIER 2ND SB ANDED WITH MULTIPLICAND
1 1 1 1 MULTIPLIER 3RD SB ANDED WITH MULTIPLICAND
1 1 1 1 MULTIPLIER MSB ANDED WITH MULTIPLICAND
BINARY 15 X 15 1 1 1 0 0 0 0 1 255
(a)
INPUTS A B OUTPUTS
0 0 0
0 1 0
1 0 0
1 1 1
(b)
b2 1 1 1 1 b1
a2 1 1 1 1 a1
1 0 0 1 SUBPRODUCT a1 b1
1 0 0 1 SUBPRODUCT a1 b2
1 0 0 1 SUBPRODUCT a2 b1
1 0 0 1 SUBPRODUCT a2 b2
1 1 1 0 0 0 0 1 PRODUCT
(c)
CA32098

FIGURE 1. Binary Multiplication: (a) An Example Showing Binary 15 Multiplied by Binary 15; (b) Truth Table for AND Gate; (c) Binary 15 Multiplied by Binary 15 Two Bits at a Time

"weight" (more significant bits to the left of less significant bits). However, as decimal multiplication shows, the multiplication process can be accomplished just as well by summing subproducts. We can multiply binary integers and get a single bit subproduct, or we can multiply larger values (for example, 9 times 9) to obtain more complex subproducts. Of course, in binary multiplication, the basis of the entire operation is still binary integer ANDing followed by weighted additions.

MULTIPLICATION USING TTL ROMS

TTL Read Only Memories can be used effectively to perform high speed multiplications. For example, by programming two 1024 bit ROMs such as the SN74187, a binary 4 bit X 4 bit multiplier can be fabricated as shown in Figure 2. These ROMs are available as catalog products as the SN74284 and SN74285. Specifications on these can be found in the data sheet at the end of this application report; propagation delays versus multiplier size shown in Figure 3.

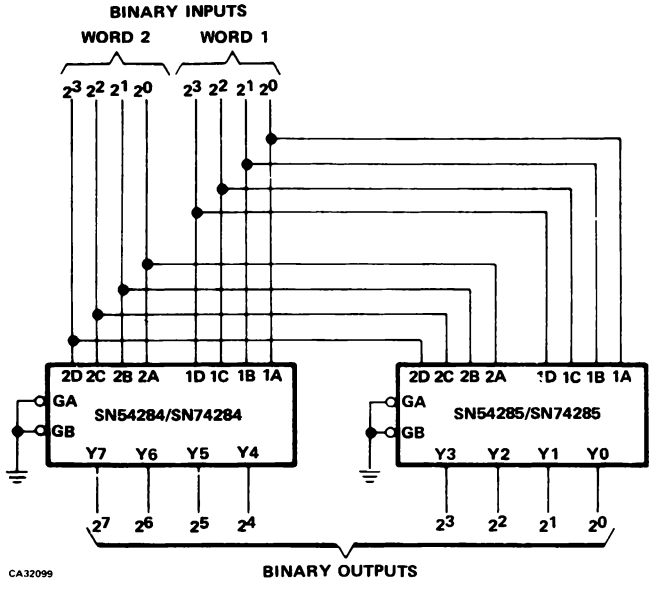


FIGURE 2. 4 Bit X 4 Bit Multiplier Using SN74284 or SN74285

Consider multiplications using ROMs, in which 4 bit X 4 bit products will be considered as subproducts for larger numbers. After the subproducts are developed, attaining high speed multiplication requires that a fast addition scheme be used to sum these subproducts. The carry save tree can be used here and is best accomplished with the Wallace[1] adder scheme. When using ROMs, almost any TTL adder can be used to combine subproducts, such as the SN74283 four bit full adder, which will give minimum package counts, or carry save trees in which the SN74H183 carry save adder is employed to give the best propagation delays.

The basic concept of the Wallace adder scheme is to consider carry outputs as sum bits of a higher order; that is, a carry in the 2^N column of binary bits is treated as a 2^{N+1} binary sum bit. This results in the generation of two groups of outputs; a carry group and a sum group. Figure 4 shows a section of a Wallace adder or "tree." The SN74H183 is ideal for this application since the carry and sum propagation delays are identical. Because the carry and sum groups must be combined, Figure 5 shows a high speed adder using the SN74S181 ALU and 74S182 look-ahead carry generator that will accumulate the groups.

Figure 6 shows a 16 bit X 16 bit multiplier with a SN74H183 Wallace tree network, SN74S181, SN74S182 carry lookahead adder, SN74284 and SN74285 multiplier chips, and featuring a 32 bit product in (typically) 103 nanoseconds.

TWO'S COMPLEMENT MULTIPLICATION

Multiplications involving two positive numbers are always the simplest possible multiplications to make and involve the minimum number of components. As a result, multiplication in the other quadrants (plus minus, minus plus, and minus minus) can be best evaluated in terms of the complexity compared to absolute value multiplication. Consequently, the first step in developing a 2's complement multiplier is to compare positive numbers to negative numbers to determine what differences will be encountered.

Let's compare positive zero through seven to negative zero through seven as illustrated in Figure 7. Notice that a 6 bit number is used, even though 3 bits are sufficient to show the data. This is because when multiplying two three-bit numbers, a 6 bit product is obtained, and all 6 bits of the product can be influenced by the multiplicand or the multiplier as illustrated in Figure 8. Note that for both numbers positive (+7 X +7), the Xs shown are all zeroes, and can be disregarded. For positive multiplier and negative multiplicand, the A group of Xs is all ones (for this specific example), but the B group is all zeroes and can be disregarded. For positive multiplicand and negative multiplier, the B group is all ones and the A group is all zeroes. For both negative numbers, groups A and B are all ones. The Xs not in the A or the B groups can be ignored in all cases as they develop the product sign and the product sign bit can be developed more efficiently by an alternate means.

Let's look a little closer at the A and B groups. In all cases, they are formed by multiplying the data bits of either the multiplier or the multiplicand with the sign bits of the other. But the sign bits are always all zeroes or all ones. If all zeroes, we can ignore the group, but if all ones, we find the result is exactly the same as if we had multiplied the data bits by minus one. Note further that multiplying a number by minus one has the effect of inverting the number bit by bit and adding one, that is, of obtaining the two's complement of the number as shown in Figure 9.

Note that the way the A and B groups are positioned in Figure 8 makes only the least significant three bits of the above operation significant. These least significant three bits are easily generated, however, by merely inverting all data bits in the operation and adding one. A simple way to do this is shown in Figure 10. Note that for positive numbers this results in an output of 111 plus 001, but 111 plus 001 is equal to 000, in the least significant three bits, so no error occurs. This method can be expanded by analogy to an N bit by N bit multiplier, in which case N bit correctors are required. This method is based on a suggestion by Phister.[2]

Note that this method obscures the sign information, but since the sign can be readily determined by simply passing the multiplier and multiplicand sign bits through an exclusive OR (0 plus 0 = 0, 1 plus 0 = 1, 0 plus 1 = 1, 1 plus 1 = 0), this is of very little consequence. This is shown in Figure 11.

In order to prevent a buildup of correction bits, the resulting corrections may be combined as shown in Figure 12. Note that the additional circuitry does not necessarily add any delay to the overall multiplier, as it is in parallel with the SN74284 and SN74285 chips. It may make additional levels necessary in the Wallace tree networks that follow, but normally there will be a design technique that will avoid this problem. It is believed that the method described represents a minimum component method of performing two's complement binary arithmetic.

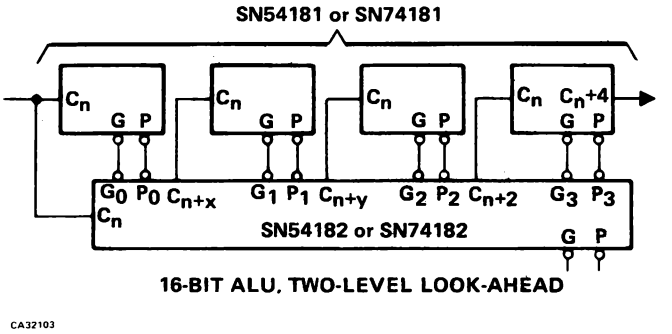
MULTIPLIER SIZE	PACKAGES* 26 PIN	REQUIRED 16 PIN	TYPICAL PROPAGATION DELAY (NANOSECONDS)
4 X 4		2	40*
8 X 8	3	13	70
16 X 16	5	74	103
24 X 24	6	143	119
36 X 36	10	270	119

PACKAGES USED: SN74284, SN74285, SN74283, SN74S181, SN74S04 (1 ONLY ON 16 X 16 AND LARGER), SN74S182

*OPEN COLLECTOR OUTPUT, A PULL-UP RESISTOR IS NEEDED TO ACHIEVE THIS. SEE DATA SHEETS ON SN74284 AND SN74285. ALL DELAYS SHOWN ARE COMPONENT DELAYS ONLY, AND NEGLECT SYSTEM DELAYS.

CA32101

FIGURE 3. Propagation Delays Versus Package Counts



CA32103

FIGURE 5. A High Speed Adder Using the SN74S181

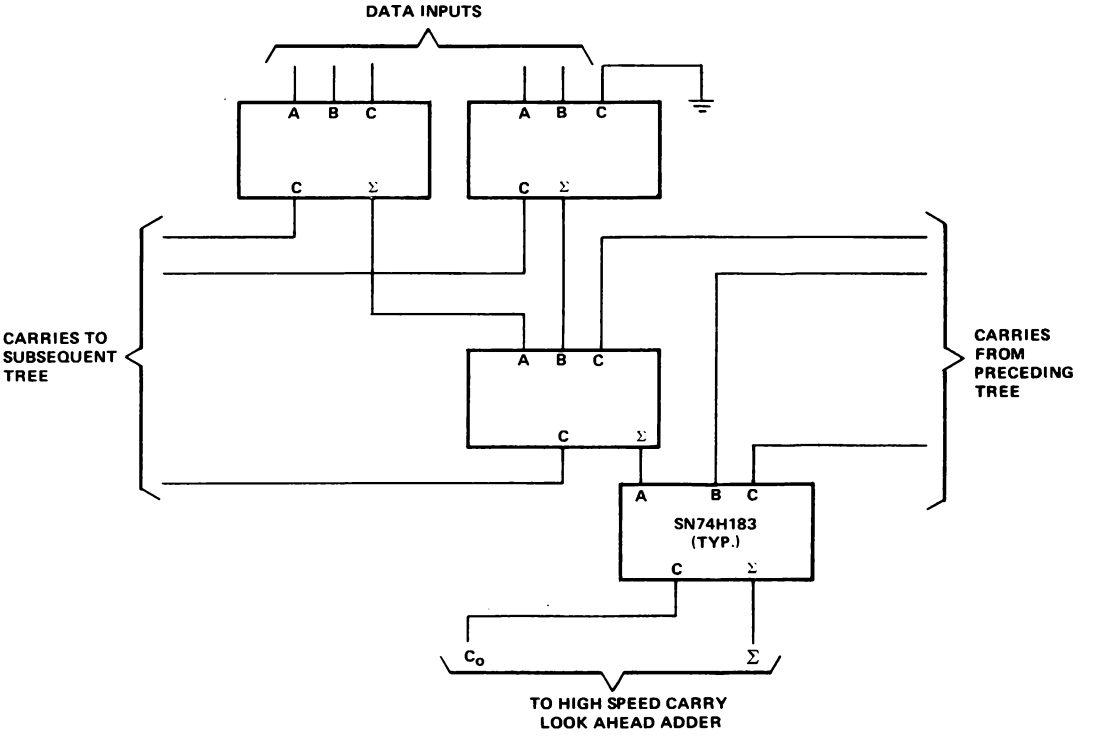


FIGURE 4. A Section of a Wallace Adder or "Tree"

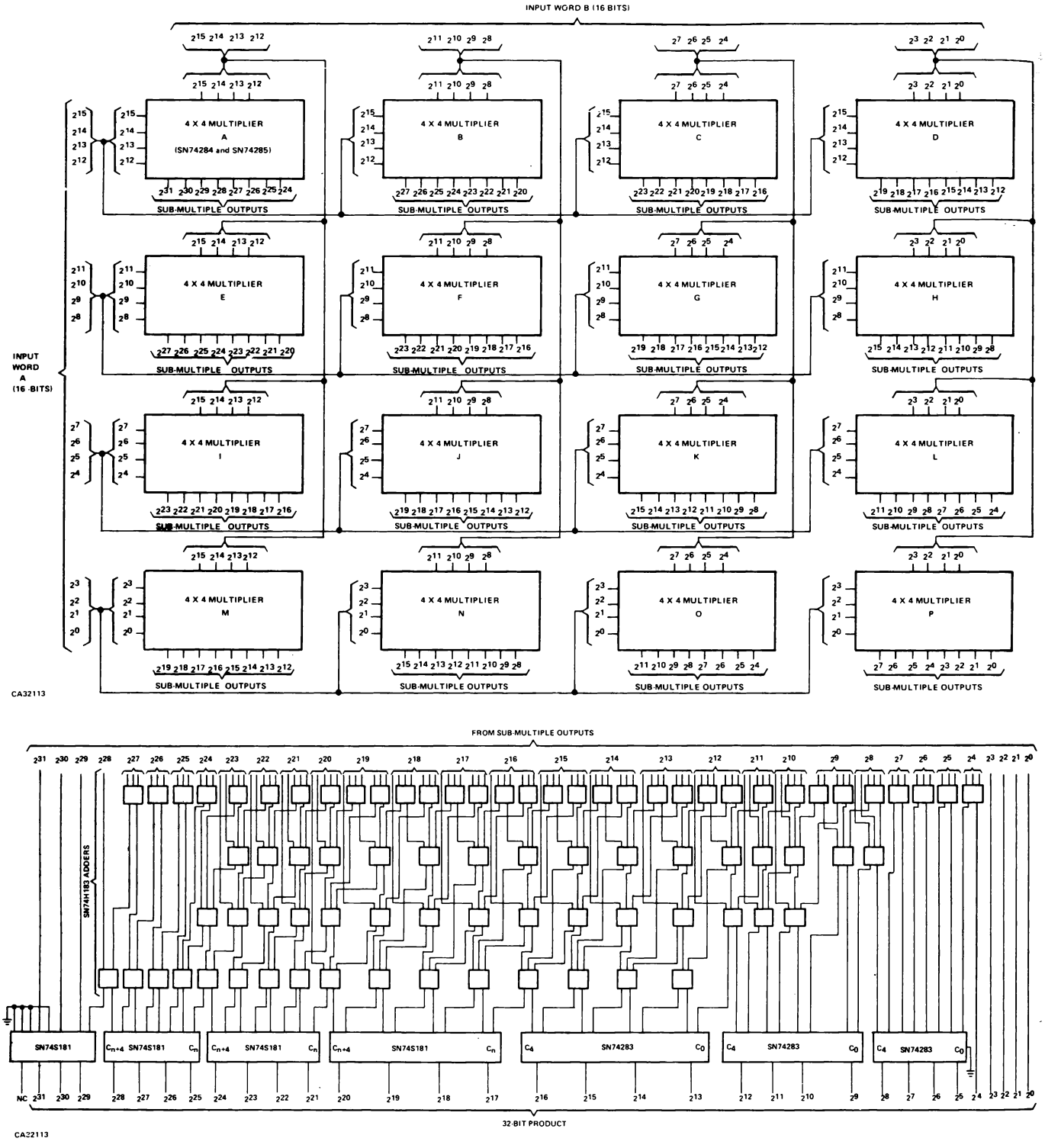

INPUT WORD B (16 BITS)
4 X 4 MULTIPLIER A (SN74284 and SN74285)
4 X 4 MULTIPLIER B
4 X 4 MULTIPLIER C
4 X 4 MULTIPLIER D
4 X 4 MULTIPLIER E
4 X 4 MULTIPLIER F
4 X 4 MULTIPLIER G
4 X 4 MULTIPLIER H
4 X 4 MULTIPLIER I
4 X 4 MULTIPLIER J
4 X 4 MULTIPLIER K
4 X 4 MULTIPLIER L
4 X 4 MULTIPLIER M
4 X 4 MULTIPLIER N
4 X 4 MULTIPLIER O
4 X 4 MULTIPLIER P
SUB-MULTIPLE OUTPUTS
INPUT WORD A (16 BITS)
CA32113
FROM SUB-MULTIPLE OUTPUTS
SN74H183 ADDERS
SN74S181
SN74283
32-BIT PRODUCT
CA32113

FIGURE 6. A 16 X 16 Multiplier with a SN74H183 Wallace Tree Network

TRUNCATED MULTIPLICATIONS

Often a truncated multiplier is adequate; in such a case considerably more savings can be had. For example, if an 8 bit product of two 8 bit numbers is required, we find (see Figure 13) that only one SN74284 and 3 SN74285s are needed, and the associated adder count is also roughly halved. Truncating the product to the same size number as the inputs can result in about a 2 to 1 savings in packages.

Truncating a product does lead to a truncation error. This arises because in the truncation we effectively cut the carry leads from the portion of the adder tree discarded by the truncation. Referring to Figure 14, a 8 bit X 8 bit multiplier, or Figure 6, a 16 X 16 multiplier, we can deduce that reducing the products to the 8 (or 16) most significant bits (one half size) causes 2 carry lines on the 8 bit X 8 bit and 6 carry lines on the 16 bit X 16 bit to be

left unterminated. Since any or all of these carry lines could have carries on them, depending on the numbers being multiplied, the absolute value of the truncation error is obviously equal to the number of carry lines left disconnected. This turns out to be (n/2 – 2) lines, where n is the size of the multiplier or multiplicand for a "square" multiplication. Note that we can cut the maximum value of this error in half by forcing logical zeroes on one half of these carry lines and logical ones on the other half. This amounts to forcing (n/4 – 1) carries onto the multiplier as indicated in Figure 15. Of course, this error can always be reduced by moving the truncation back in the LSB direction and discarding the least significant bits of the result; as Figure 15 indicates, even on a 32 bit X 32 bit multiplier, an extra three bits of Wallace Tree (and the associated multipliers) will reduce the Wallace Tree error to zero, and the total truncation error becomes an

POSITIVE NUMBERS		2'S COMPLEMENT NEGATIVE NUMBERS		1'S COMPLEMENT NEGATIVE NUMBERS		
SIGN	DATA	SIGN	DATA	SIGN	DATA	NUMBER
000	000	000	000	111	111	0
000	001	111	111	111	110	1
000	010	111	110	111	101	2
000	011	111	101	111	100	3
000	100	111	100	111	011	4
000	101	111	011	111	010	5
000	110	111	010	111	001	6
000	111	111	001	111	000	7

CA32104

FIGURE 7. Positive and Negative Numbers, Zero Through Seven

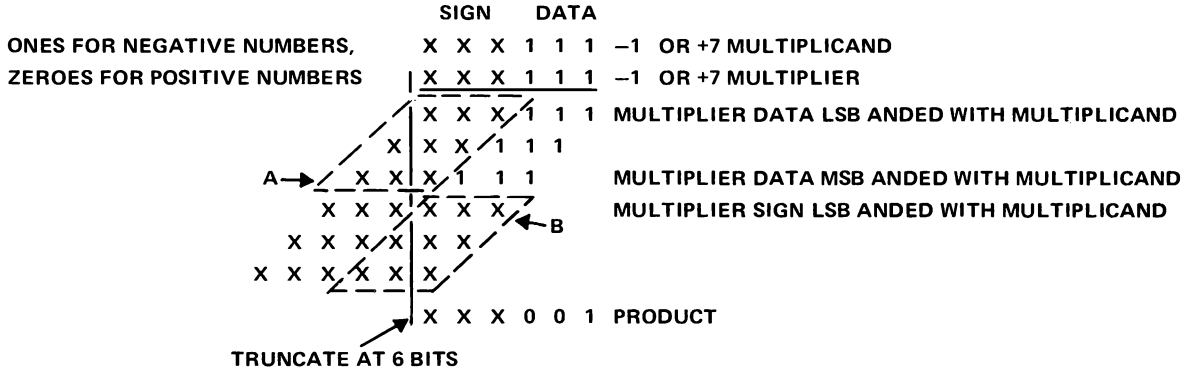

SIGN DATA
ONES FOR NEGATIVE NUMBERS, X X X 1 1 1 –1 OR +7 MULTIPLICAND
ZEROES FOR POSITIVE NUMBERS X X X 1 1 1 –1 OR +7 MULTIPLIER
X X X 1 1 1 MULTIPLIER DATA LSB ANDED WITH MULTIPLICAND
A
MULTIPLIER DATA MSB ANDED WITH MULTIPLICAND
MULTIPLIER SIGN LSB ANDED WITH MULTIPLICAND
B
X X X 0 0 1 PRODUCT
TRUNCATE AT 6 BITS
CA32105

FIGURE 8. Multiplying Two 3-Bit Numbers in 2's Complement Arithmetic

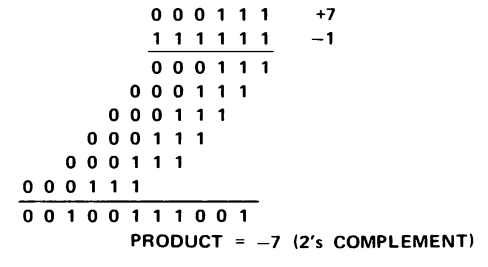


FIGURE 9. Multiplying By Minus One

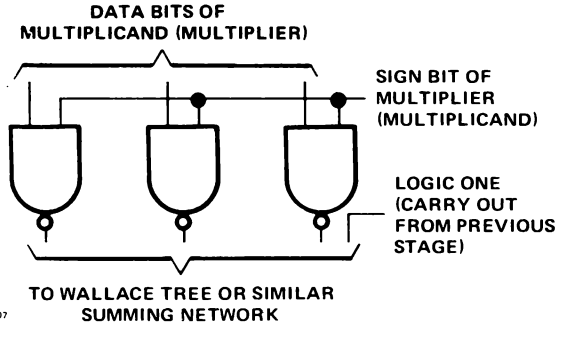

DATA BITS OF MULTIPLICAND (MULTIPLIER)
SIGN BIT OF MULTIPLIER (MULTIPLICAND)
LOGIC ONE (CARRY OUT FROM PREVIOUS STAGE)
TO WALLACE TREE OR SIMILAR SUMMING NETWORK
CA32107

FIGURE 10. Two's Complement Corrector for 3-Bit

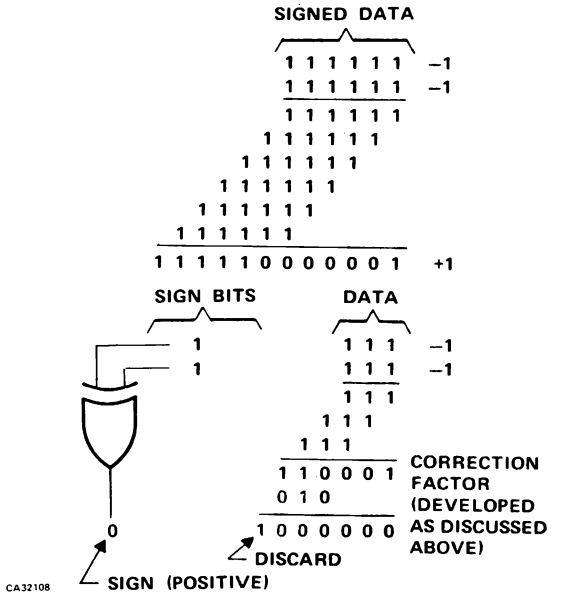


FIGURE 11. Developing the Sign Bit

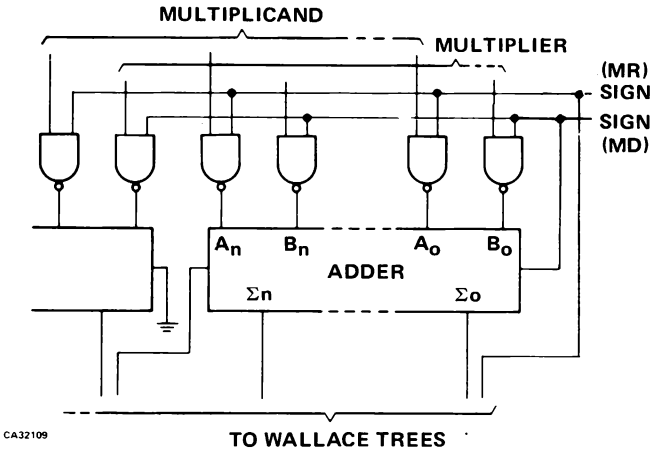


FIGURE 12. 2's Complement Correction Circuit

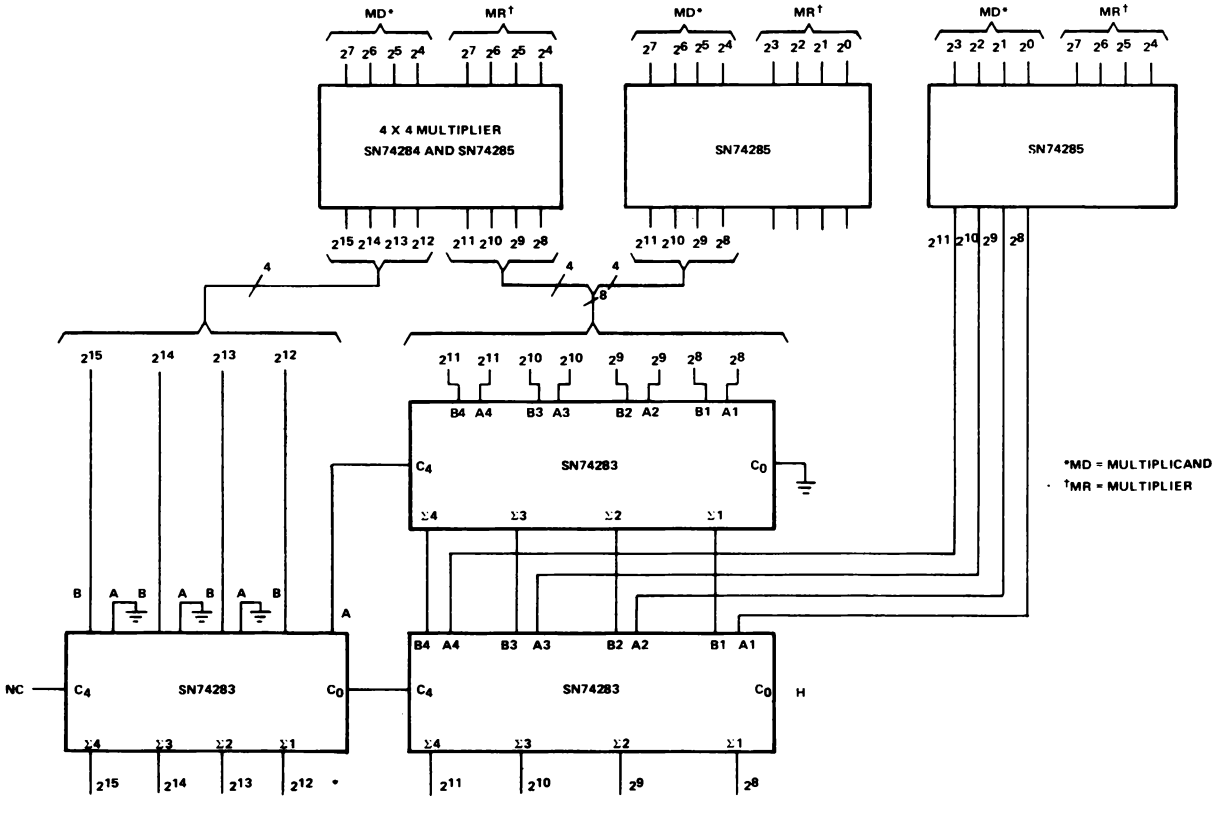


FIGURE 13. A Truncated 8 X 8 Multiplier

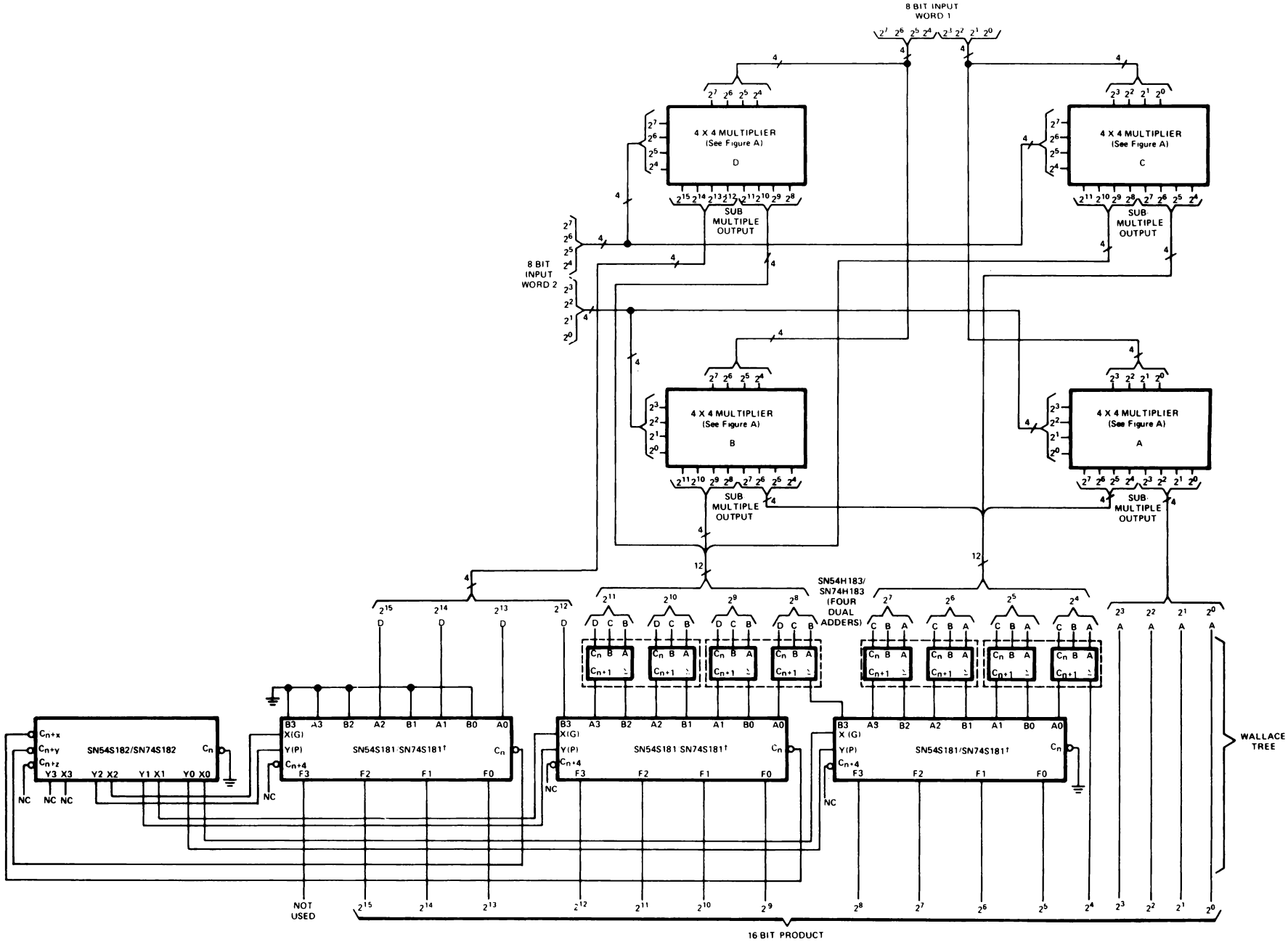


FIGURE 14. A 16 X 16 Multiplier with a SN74H183 Wallace Tree Network

MULTIPLIER SIZE (MULTIPLIER AND MULTIPLICAND EQUAL)	ERROR (WITH NO CORRECTION)	ERROR WITH N/4 - 1 ADDED TO PRODUCT
4 X 4	0	0
8 X 8	2	± 1
12 X 12	4	± 2
16 X 16	6	± 3
20 X 20	8	± 4
24 X 24	10	± 5
28 X 28	12	± 6
CA32114 32 X 32	14	± 7

FIGURE 15. Truncation Errors

(irreducible) ± 1 bit. The number of bits to be added to reduce the Wallace Tree error to zero is simply the number of binary bits required to represent the value of the error; therefore, a 20 X 20 up to a 32 X 32 (5 to 7 bits of error) are contained in the binary numbers 100 to 111 and require three additional Wallace Tree bits, the error in a 12 X 12 and a 16 X 16 are contained in binary numbers 10 and 11, so require two, etc. As indicated before truncation will always result in a round-off error of ± 1 bit which is exclusive of the Wallace Tree carry error.

REFERENCES

1. C. D. Wallace, "A Suggestion for a Fast Multiplier," *IEEE Transactions on Electronic Computers*, Vol. 13, No. 1 pp. 14-17, February 1964.

2. Phister, *Logical Design of Digital Computers*, pp. 311-314.

CIRCUIT TYPES SN54284, SN54285, SN74284, SN74285
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

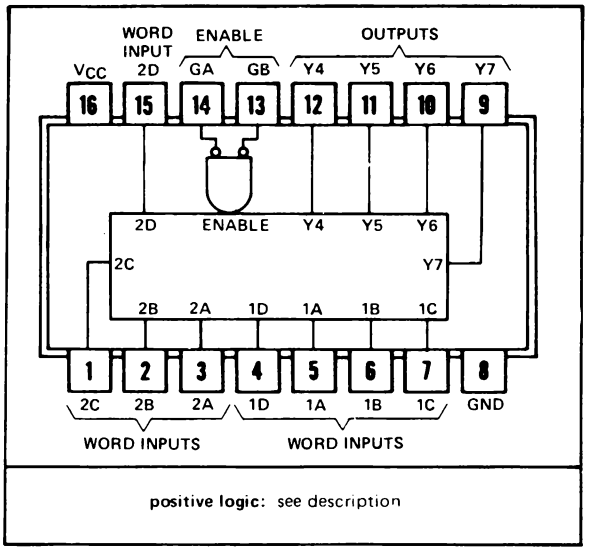
- Fast Multiplication of Two Binary Numbers 8-Bit Product in 40 ns Typical
- Expandable for N-Bit-by-n-Bit Applications: 16-Bit Product in 70 ns Typical 32-Bit Product in 103 ns Typical
- Fully Compatible with Most DTL and TTL Circuits
- Diode-Clamped Inputs Simplify System Design

description

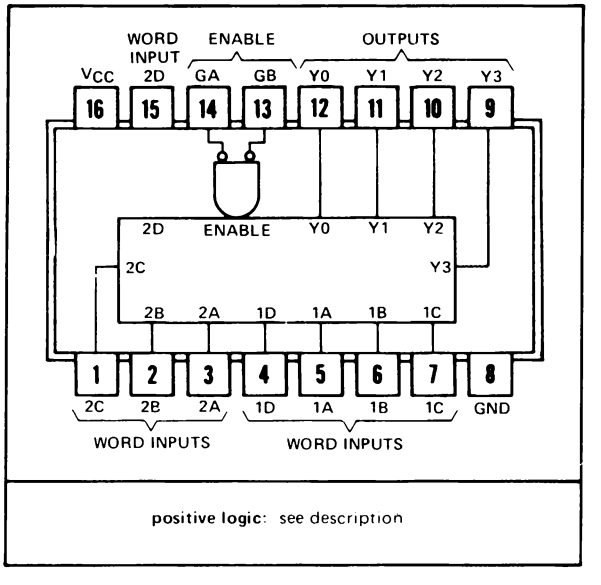
These high-speed TTL circuits are designed to be used in high-performance parallel multiplication applications. When connected as shown in Figure A, these circuits perform the positive-logic multiplication of two 4-bit binary words. The eight-bit binary product is generated with typically only 40 nanoseconds delay.

This basic four-by-four multiplier can be utilized as a fundamental building block for implementing larger multipliers. For example, the four-by-four building blocks can be connected as shown in Figure B to generate submultiple partial products. These results can then be summed in a Wallace tree, and, as illustrated, will produce a 16-bit product for the two eight-bit words typically in 70 nanoseconds. SN54H183/SN74H183 carry-save adders and SN54S181/SN74S181 arithmetic logic units with the SN54S182/SN74S182 look-ahead generator are used to achieve this high performance. The scheme is expandable for implementing N X M bit multipliers.

SN54284, SN74284
J OR N DUAL-IN-LINE OR W FLAT PACKAGE
(TOP VIEW)


WORD INPUT
ENABLE
OUTPUTS
VCC 2D GA GB Y4 Y5 Y6 Y7
16 15 14 13 12 11 10 9
2D ENABLE Y4 Y5 Y6
2C Y7
2B 2A 1D 1A 1B 1C
1 2 3 4 5 6 7 8
2C 2B 2A 1D 1A 1B 1C GND
WORD INPUTS
WORD INPUTS
positive logic: see description

SN54285, SN74285
J OR N DUAL-IN-LINE OR W FLAT PACKAGE
(TOP VIEW)


WORD INPUT
ENABLE
OUTPUTS
VCC 2D GA GB Y0 Y1 Y2 Y3
16 15 14 13 12 11 10 9
2D ENABLE Y0 Y1 Y2
2C Y3
2B 2A 1D 1A 1B 1C
1 2 3 4 5 6 7 8
2C 2B 2A 1D 1A 1B 1C GND
WORD INPUTS
WORD INPUTS
positive logic: see description

The SN54284 and SN54285 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74284 and SN74285 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54284, SN54285 Circuits . . . . . −55°C to 125°C
SN74284, SN74285 Circuits . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54284, SN54285			SN74284, SN74285			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CC}	Supply current	V_{CC} = MAX, T_A = 125°C, See Note 2	SN54284, SN54285 N package only			99	mA
		V_{CC} = MAX, See Note 2	SN54284, SN54285		92	110	
			SN74284, SN74285		92	130	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: With outputs open and both enable inputs grounded, I_{CC} is measured first by selecting an output product which contains three or more high-level bits, then by selecting an output product which contains four low-level bits.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF to GND, R_{L1} = 300 Ω to V_{CC}, R_{L2} = 600 Ω to GND, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from word inputs			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from word inputs			40	60	

NOTE 3: Load circuit is as described above

TEXAS INSTRUMENTS

Using the SN 74160 synchronous counters (CA 174)

USING THE SN74160 FAMILY OF SYNCHRONOUS COUNTERS

by
Gene Cavanaugh

The SN74160 through SN74163 series of 4 bit TTL synchronous counters are designed to eliminate certain drawbacks associated with ripple counters. For instance, all storage elements are clocked simultaneously to provide synchronous operation, minimizing output overlaps or "skew". In addition, these counters are capable of being loaded to any number synchronously with the clock, and cascading circuitry has been provided on the chip to make it easier for the system designer to build longer counters. As versatile as the SN74160, -161, -162, -163 counters are, problems sometimes arise when they are cascaded for high speed applications. However, there are techniques which can be used with these counters to ensure that their full potential is realized.

Before we look at the details of cascading these counters, it is important to be familiar with the carry circuitry that has been incorporated on the chip.

CARRY CIRCUITRY OPERATION

Figure 1 shows the logic diagram of the SN74163 synchronous binary counters. There are three pins associated with the carry operation: count enable P input (CEP), count enable T input (CET), and the ripple carry output (RC). The RC output is normally at a logic 0 and remains there until the counter reaches maximum count (1111) and the CET is at a logic 1. RC then produces a logic 1. The carry operation is similar on the SN74160, -161, and -162 versions.

Referring to Figure 2, a logic 1 on CEP allows the counter to count when clocked, it has nothing to do with carries between counters. CET not only enables its own counter but also controls the RC output to subsequent counters. Both CEP and CET must be high before the counter is enabled, i.e., allowed to follow the clock. Also note when cascading these counters, the first counter must count at maximum input clock frequency, but it divides down the frequency at which the next counter must operate. For a binary counter such as the SN74163 operated at 25 MHz, for example, the first counter must accept 25-MHz inputs but the second counter need only accept counts at about 1.6 MHz or 16 times as slow.

Refer to the interconnection diagram shown in Figure 3. In the example given, the RC1 output (of the first counter) is available for 40 ns (one clock pulse period) only, but RC2 is available for 640 ns. It is also true that when the cascaded counters are required to propagate a carry, the most significant counter comes to a maximum count condition first, the next most significant counter comes to a maximum next, and so forth.

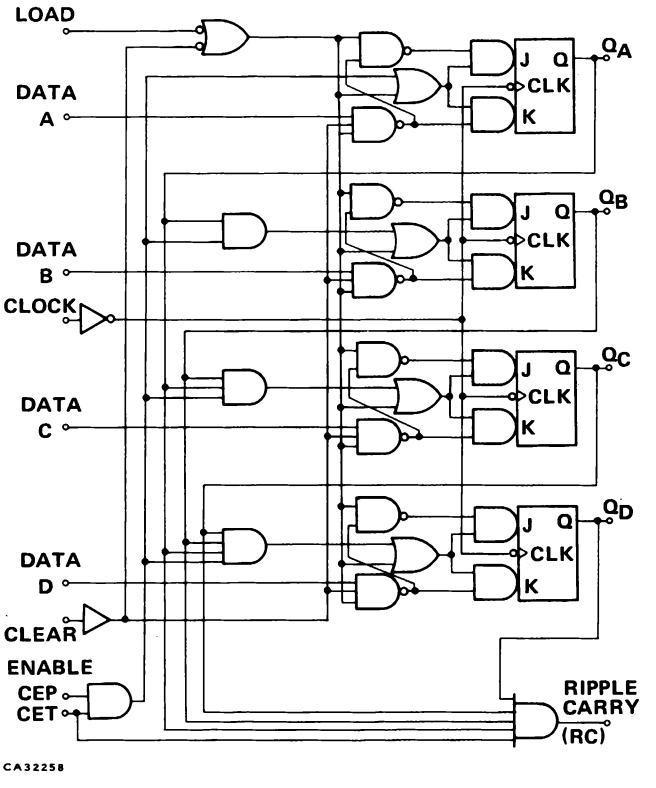


FIGURE 1. SN74163 Logic Diagram

As Figure 3 shows, the least significant counter drives the CEP inputs to all other counters in a chain. It is also the last counter to come to a maximum count and, since the Q outputs of the counter drive the RC gate, the RC1 output involves a clock-to-flip-flop output-to-carry delay as shown in Figure 4. By the time that RC1 is valid, all other counters have been at a maximum count long enough for all CET connections to be valid, so the only signal required by the other counters is the CEP signal from RC1. Therefore,

it follows that the critical path for the chain is clock-to-RC1-to-CEP plus counter setup time as shown in Table 1. Since this path is slower than the internal counter delays, it limits the frequency of the chain to less than the frequency of a single counter (also shown in Table I).

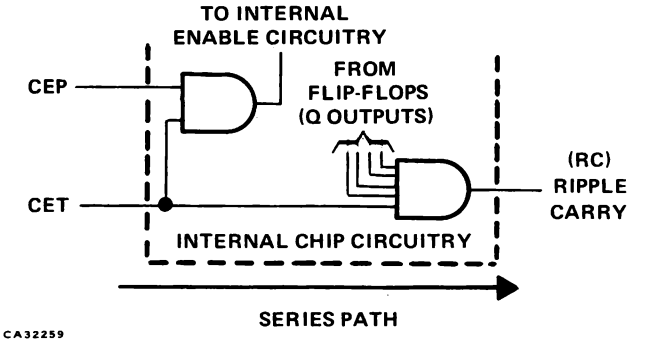


FIGURE 2. Carry Circuitry of the SN74163

isn't necessary to wait for the carry from the first counter, count frequency will not be affected. These criteria are easily met by forcing CET1, CEP1 and CET2 to a logic 1 (enabled), rippling RC2 into CET3, and RC3 into CET4. RC1 is then connected to the CEP of all subsequent counters.

This interconnection scheme is a modified "carry-look-ahead" system. Only RC1 is carried forward to all subsequent stages. As discussed later, the ripple mode carry system used for all other counters in the chain causes some carry signal phase shifting which can be a problem in some applications.

Ripple Carry Signal Phase Shifting

In Figure 5 the carry circuitry of the counters is as discussed in the previous application. When the SN74163 counter reaches max count (1111) the RC output does not appear for 10 ns (typically) due to the inherent propagation delay in the carry circuitry.

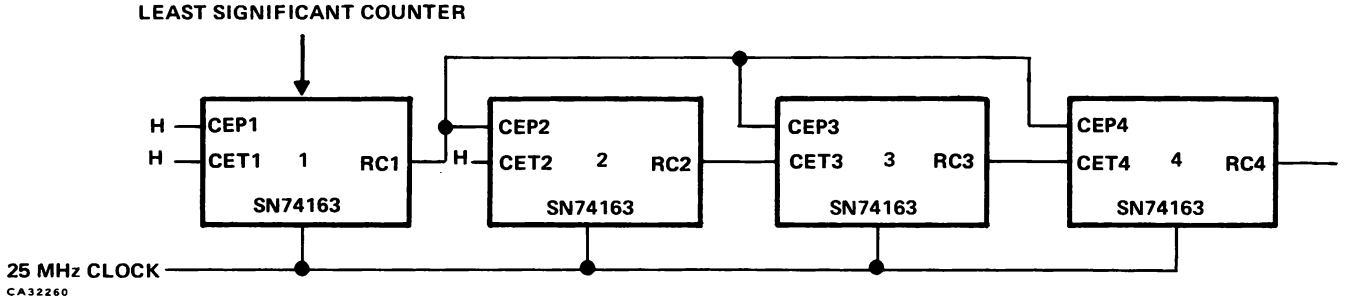


FIGURE 3. SN74163 Interconnection for a 16-Bit Counter

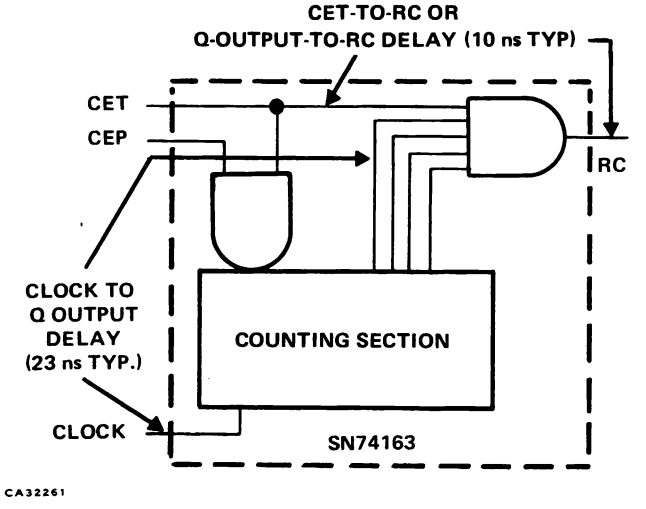


FIGURE 4. RC Delay from Clock

All the other counters have their flip-flop outputs at a maximum, so the critical path for them is CET-to-RC (typically 10 ns). Therefore, ripple carry techniques may be used through all counters except the first, and as long as it

Suppose that Counter 2 is making the step from a maximum count (1111) to a minimum count (0000). As shown in Figure 6, RC2 remains for 10 ns after the Counter 2 flip-flop outputs have changed to 0000. Now suppose further that Counter 3 is at 1110 and changes to 1111 at the same time Counter 2 goes to 0000. Also assume that the subsequent counters are at maximum count (1111). Because the Ripple Carry from Counter 2 is applied for 10 ns after Counter 3 changes, the RC3 output will put out a 10-ns-wide pulse. Since the flip-flop outputs of Counter 4 are at 1111, this 10-ns "carry glitch" will also appear at RC4.

The RC glitch does not cause problems with the counter enabling or cascading system because the CEP input of each counter beyond the first is driven by the RC output of the first counter, and this signal is phased correctly to prevent improper operation. If the RC glitch is not gated out, it can be a problem where the enable signal is used for other purposes such as maximum count indicator to other logic. Fortunately, there's one thing operating in the system designer's favor: the SN54160/74160 family is *guaranteed* to operate up to 25 MHz (any one counter). This means all gates and flip-flops on the chip are very tightly controlled – large deviations from the norm simply

Table I. Frequency Capabilities of the SN74160 Family

Parameter	Counting		Programming		Units
	Typ	Max	Typ	Max	
Clock to RC output	23	35	23	35	ns
CET or CEP setup time	15	20			ns
Load setup time			15	25	ns
External NAND Gate (SN74S00)			3	5	ns
Totals	38	55	41	65	ns
Maximum Clock Frequency (excluding wiring delays)	26.3	18.2	24.4	15.4	MHz

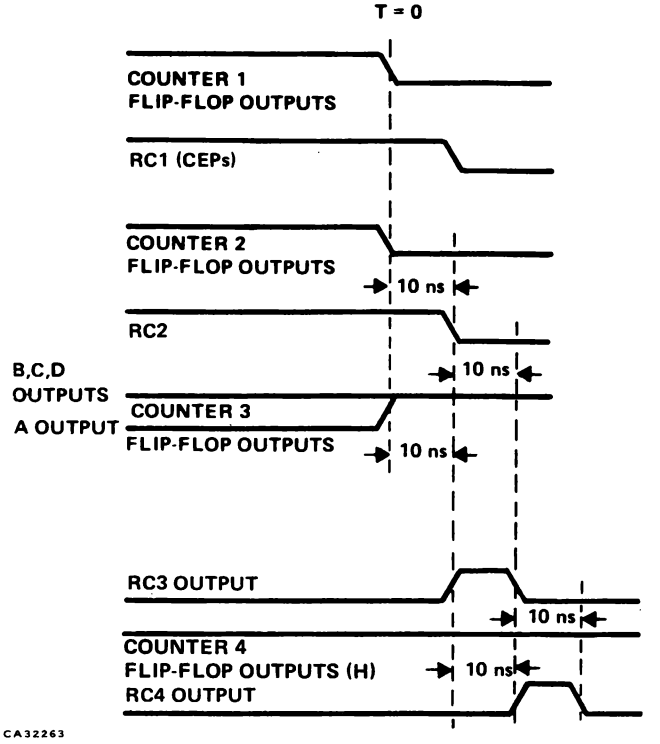


FIGURE 6. Timing Relations with the Carry "Glitch" in the SN74160 Family

to provide the programming pulse. This approach does limit the frequency of cascaded counters. Referring to Table I, the minimum count frequency of the SN74160 family is

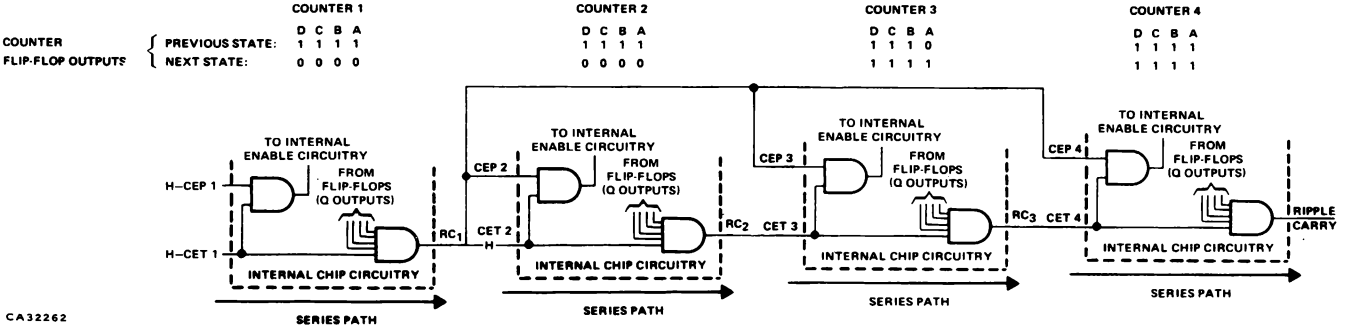


FIGURE 5. Carry "Glitches" in the SN74160 Family

don't exist. As a result, the delays will be highly predictable and can be dealt with.

The easiest way to remove the RC "glitch" for external use is to NAND RC1 with RC4 (or the highest order counter). Since RC1 occurs 10 ns after the Q outputs of the counters change, but the "carry glitch" never occurs earlier than 20 ns after the Q outputs change, they do not occur simultaneously. A common application for the SN74160 family of counters is to utilize the RC output for programming (parallel loading). This signal is fed back to the counter "LOAD" input through an inverter in order to parallel load in new data after the counter chain reaches maximum count. On the next clock pulse, the counter chain will synchronously jump to the state of the data inputs. This application is shown in Figure 7 with the RC outputs NANDed together to eliminate the RC glitch and only slightly greater than 18 MHz when cascaded, with a typical of about 26 MHz. When programming, however, the delay in the external NAND gate drops the frequency response of the chain down to about 15 MHz, with a typical of about 24 MHz.

Carry Anticipate Circuits

Fortunately, where maximum clock frequency is the overriding consideration, external circuitry can be added to bring the chain frequency back to the frequency capability of an individual counter, 32 MHz typically or 25 MHz minimum. This is accomplished by a carry-anticipate circuit which is so called because it detects the count immediately preceding a maximum count ("anticipates" the carry output) and ANDs this condition with the next clock pulse (usually in a flip-flop so the information will be stored for a

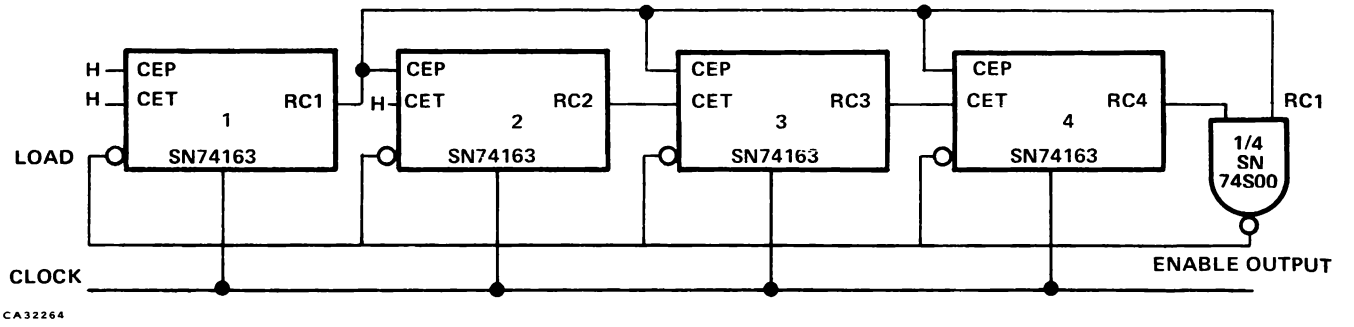


FIGURE 7. Programming the SN74160 Family with a NAND Gate

full clock period) to provide a "fast carry" to replace RC1. With the carry anticipate circuit shown in Figure 8, it is also necessary to provide a clock inversion to the flip-flop, because the SN74S112 triggers on the negative clock edge while the SN74160 family triggers on the positive clock edge. This is no problem because the gating element used to detect the count preceding maximum count has an additional path used for clock inversion. This also offers the benefit of having the clock delay path matched to the carry-anticipate path; i.e., since both are on one chip (the SN74S182), they will be simultaneously slow or fast, keeping the same relative delays. Note that the other half of

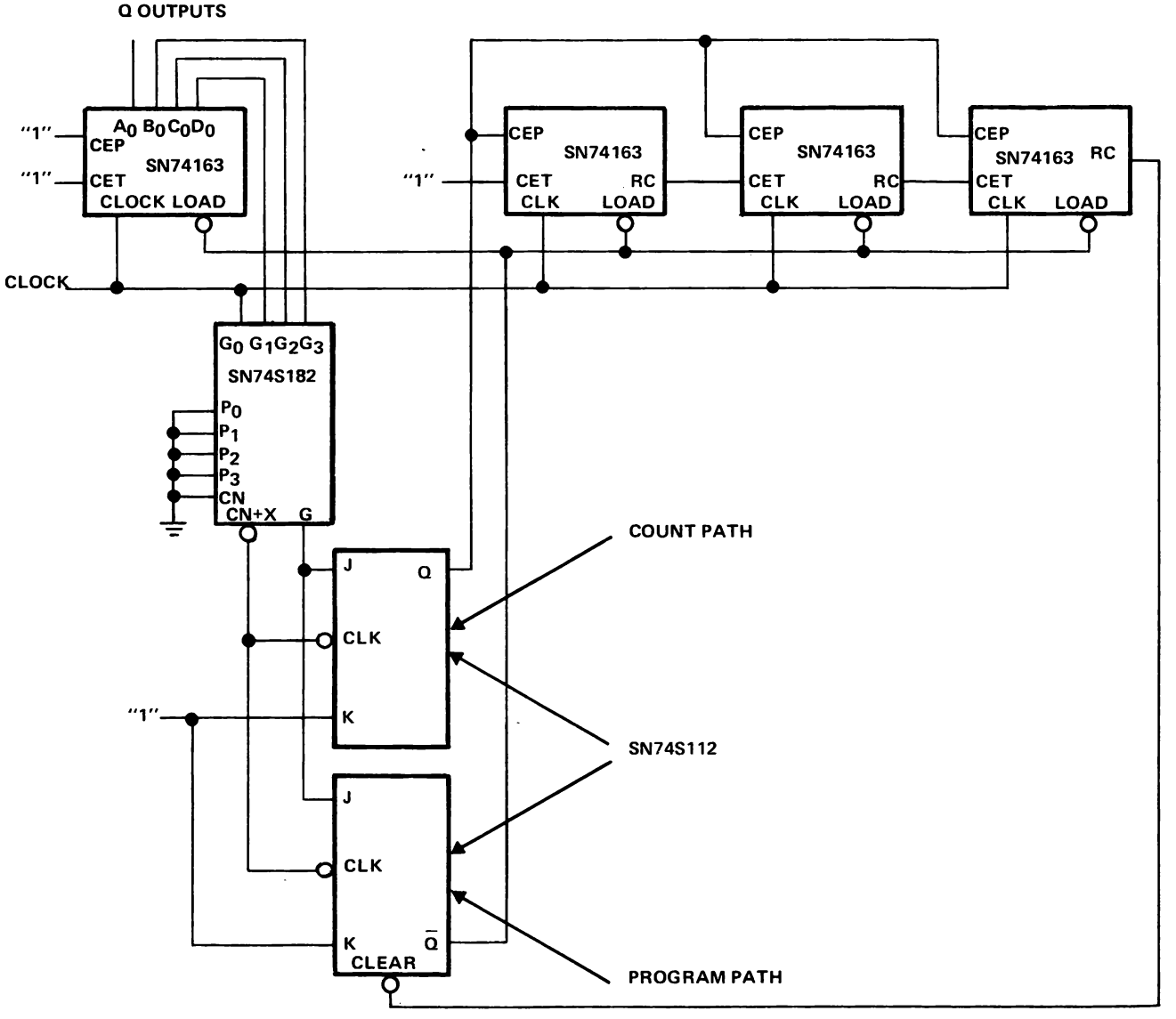


FIGURE 8. Carry Anticipate Circuitry Using the SN74S112, with Programming

the SN74S112 can be used to program the chain, also, if desired.

Of course, a SN74S11 could be used to detect the count preceding a maximum, and to delay the clock, and a SN74S74 could be used to generate the chain CEP and to program. This is shown in Figure 9. Note, however, the worst case numbers for the components used slightly limit programming frequency as shown in Table 2. It should also be pointed out that these are only two of many variations of circuits which could be used for carry-anticipate circuits.

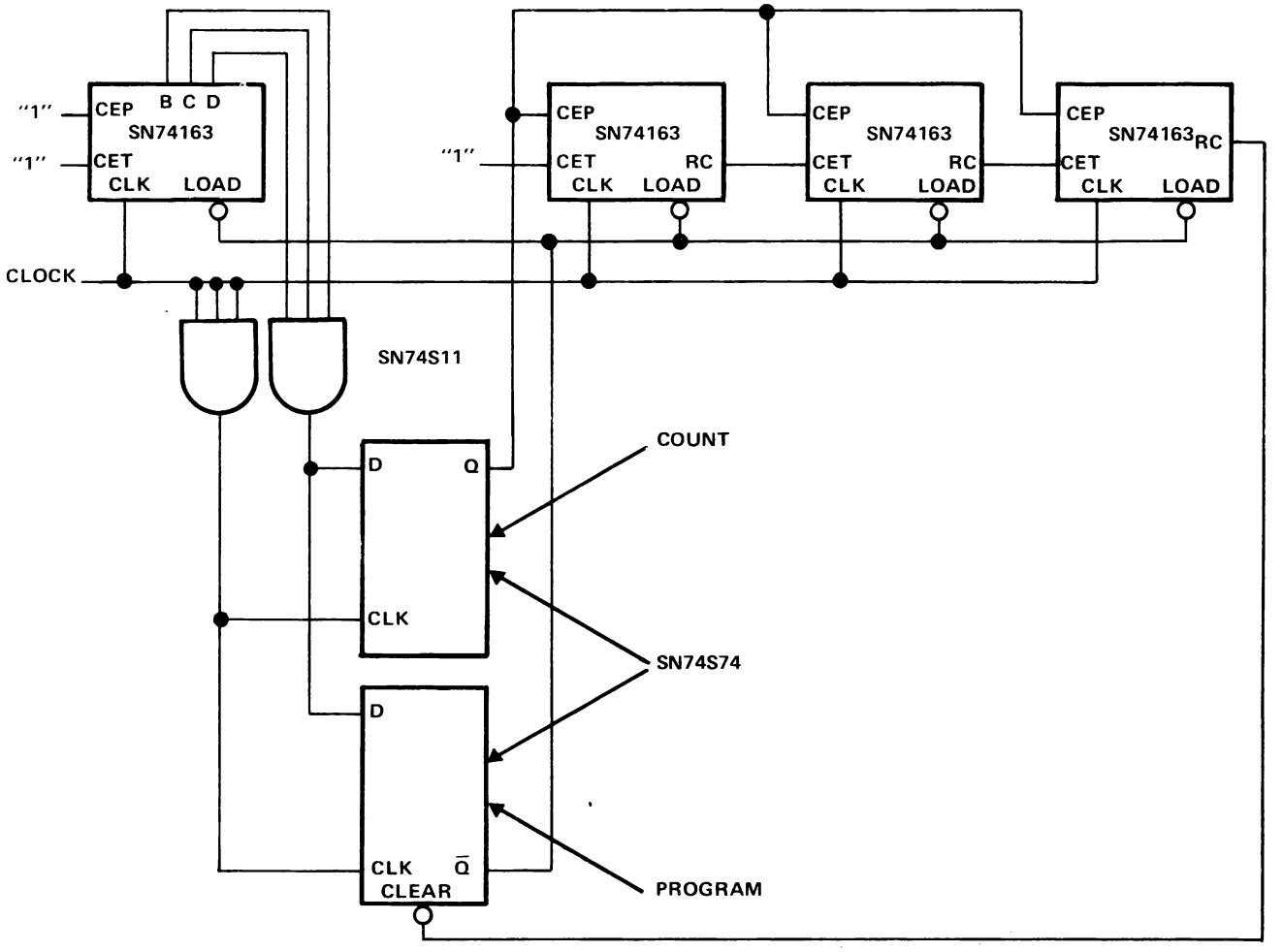


FIGURE 9. Carry Anticipate Circuitry Using the SN74S74 with Programming

Table II. Frequency Capabilities of the SN74160 Family Using Carry-Anticipate

Parameter		Counting		Programming		Units
		Typ	Max	Typ	Max	
Clock to Q	LH	13	20	13	20	ns
outputs	HL	15	23	15	23	ns
SN74S182 G	LH	5	7.5	5	7.5	ns
output	HL	7	10.5	7	10.5	ns
SN74S182 Cn+x	LH	4.5	7	4.5	7	ns
output	HL	4.5	7	4.5	7	ns
SN74S112 setup		2	3	2	3	ns
SN74S112 clock	LH	4	7	4	7	ns
to output	HL	5	7	5	7	ns
SN74160 count setup		15	20			ns
SN74160 load setup				18	20	ns
SN74S11	LH	4.5	7	4.5	7	ns
	HL	5	7.5	5	7.5	ns
SN74S74 setup	LH	3	5	3	5	ns
	HL	3	5	3	5	ns
SN74S74 clock	LH	6	9	6	9	ns
to output	HL	6	9	6	9	ns
Circuit 1 Delays		24.5	34	27.5	39	ns
Circuit 2 Delays		26	36	29	41	ns
Circuit 1 Frequency		32*	25*	32*	25*	MHz
Circuit 2 Frequency		32*	25*	32*	24.4	MHz

*Circuit delay times are short enough to permit the counter to be operated without limitations.

MOS/LSI in Terminals Application Report

(B 109)

MOS/LSI IN TERMINALS

The functions performed by terminals are data processing operations such as entry, buffering, transmission/reception and the display of the digital data. MOS/LSI is particularly well suited for these functions.

Figure 1 shows a block diagram of a typical terminal system. This system forms the basis for this discussion which will include:

MOS/LSI Code Converters
MOS/LSI Asynchronous interface circuits
MOS/LSI Digital storage buffer circuits
MOS/LSI Character generator circuits
MOS/LSI Keyboard encoder circuits

Some of these devices are still being developed.

COMMUNICATIONS LINK

Relative to data processing times, the communications link varies from very slow to slow. Teletype grade lines are generally used for asynchronous transmissions and are limited to about 120 characters per second. Voice grade lines are used for synchronous data transmission and are good for about 600 characters per second. Wideband lease lines are available for up to 1200 characters per second. The modem on the end of the communication line prepares the data for transmission down a serial data channel.

ASYNCHRONOUS INTERFACE

Serial data from the line is accepted and translated to parallel data for use in the terminal. For transmission, the parallel data is converted to serial.

TMS 6010 JC/NC Asynchronous Data Interface

The TMS 6010 JC/NC is Texas Instruments MOS/LSI subsystem designed to insure the data interface between a serial communicator link and data processing equipment such as peripheral and computer.

Figure 2 shows a functional block diagram of the TMS 6010 JC/NC. The receiver section of the TMS 6010 will accept serial data from the transmission line and convert it to parallel data. The serial word will have start, data and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking the proper parity, start and stop bits and convert the data to parallel. The transmitter section will accept parallel data, convert it to serial form and generate the start, parity, and stop bits. Receiver and transmitter sections are separate and the device can operate in full duplex mode.

To allow maximum flexibility of operation, the TMS 6010 has been designed as a fully programmable circuit. The device can operate either in full duplex (simultaneous transmission and reception) or in half duplex (alternate transmission and reception). The data word may be

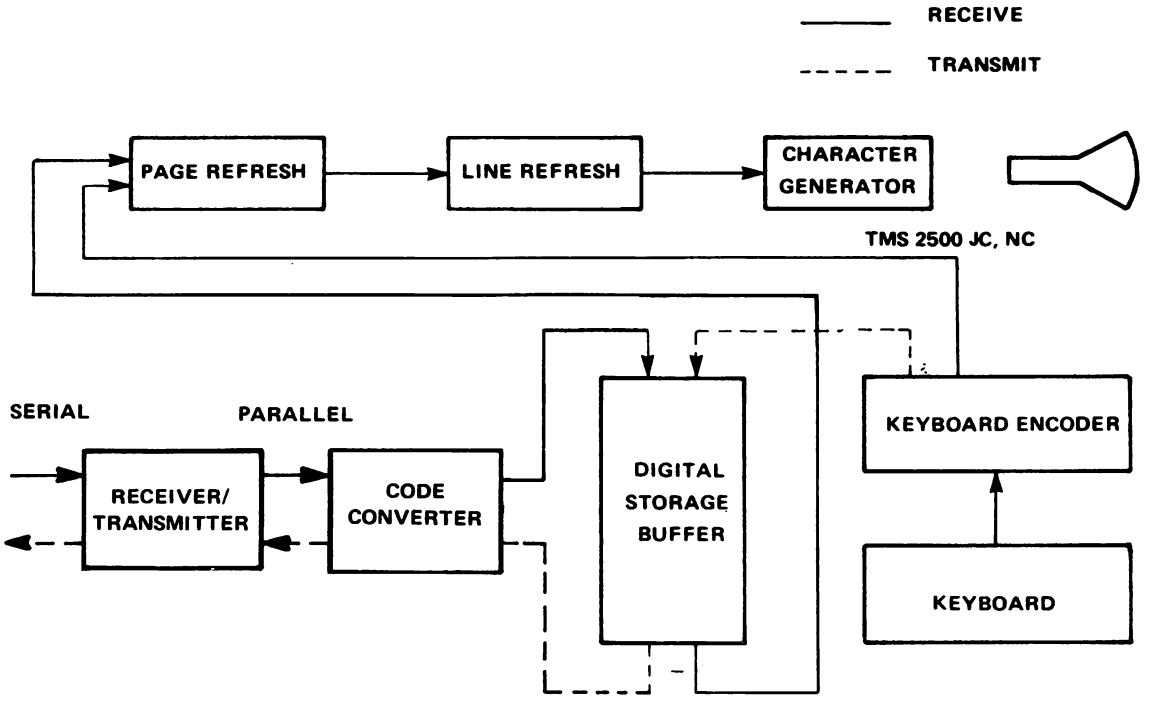


FIGURE 1. Block Diagram of a Typical Terminal System

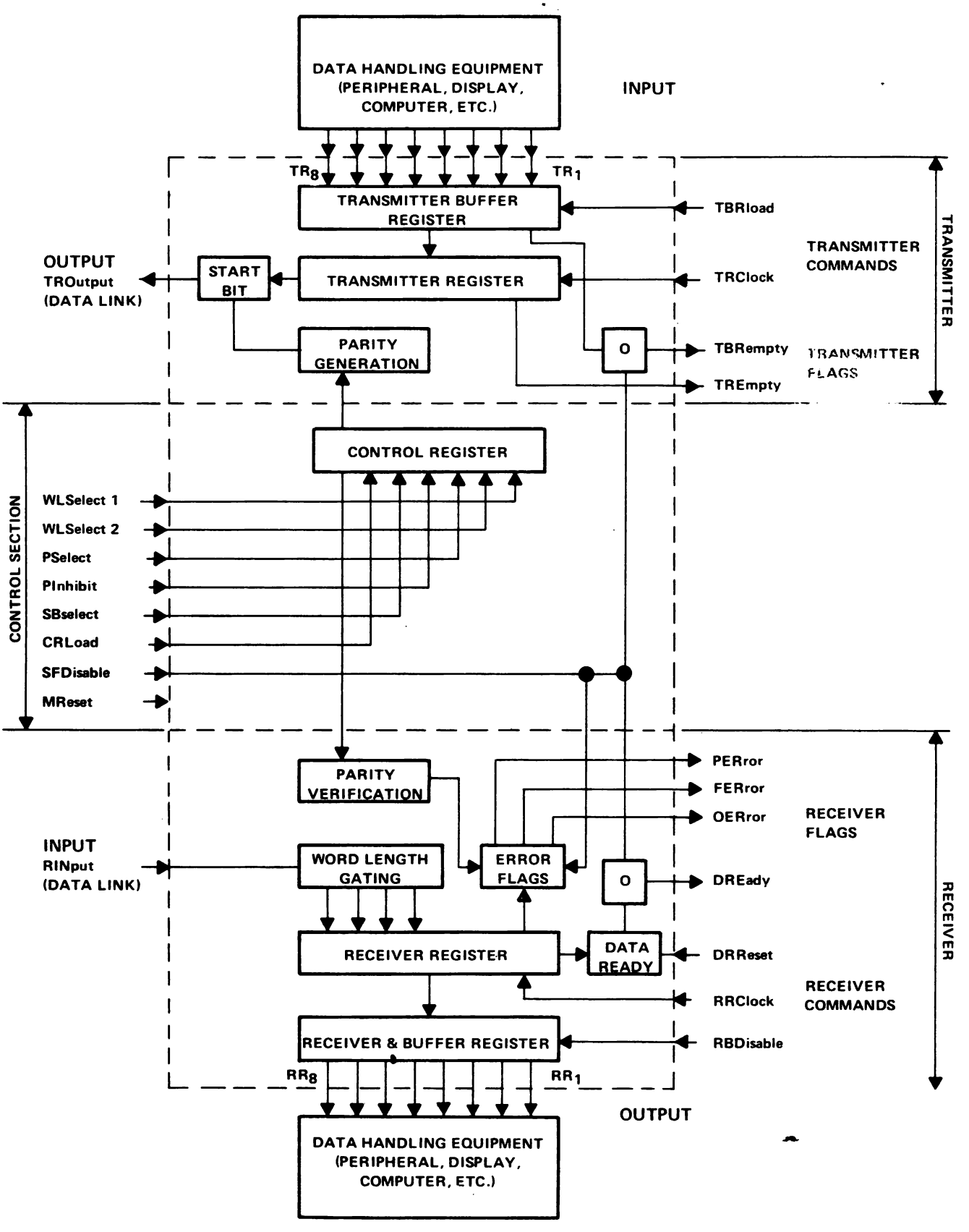


FIGURE .2. Functional Block Diagram of TMS 6010 JC/NC

externally selected to be 5, 6, 7, or 8 bits long. The baud rate is externally selected by the clock frequency, which can vary between 0 and 160 kHz. The parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification. The stop bit can be selected as either a single- or double-bit stop. Static logic is used to maximize flexibility of operation and to simplify the task of the user. The data holding registers are static and will hold a data word until it is replaced by another word.

To allow for a wide range of possible configurations, triple-state push-pull buffers have been selected on the parallel data outputs. They allow the wire-OR configuration.

The TMS 6010 can be used in a wide range of data handling equipment such as Modems, peripherals, printers, data displays, and minicomputers. By taking full advantage of the latest MOS/LSI design and processing techniques it has been possible to implement the entire transmit, receive, and format function necessary for digital data communication, in a single package, avoiding the cumbersome circuitry previously necessary.

P-channel enhancement-mode low-threshold technology permits the use of standard power supplies (+5 V, −12 V) as well as direct TTL/DTL interface. No external components are needed.

The operation of this device can be best understood by visualizing the TMS 6010 as three separate sections: 1) transmitter, 2) receiver, and 3) common control. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

Transmitter Section

The transmitter section will accept data in parallel form, serialize it, format it, and transmit it in serial form. Parallel input data is received on the transmitter buffer register data inputs TR1 through TR8. Serial output data is transmitted on the TROutput terminal. Input data is stored in the transmitter buffer register. A logic low on the TBRLoad command terminal will load a character in the transmitter buffer register. If words of less than 8 bits are used, only the least significant bits are accepted. The character is justified into the least significant bit, TR1.

The data is transferred to the transmitter register when TBRLoad terminal goes from low to high. The loading of the transmitter register is delayed if the transmitter section is presently transmitting data. In this case the loading of the transmitter register is delayed until the transmission has been performed.

Data is transmitted in serial form on the TROutput terminal. The data is clocked out by TRClock. The clock rate is 16 times faster than the data rate. The data format is as follows: start bit, data, parity bit, stop bits (1 or 2). Start bits, parity bits, and stop bits are generated by the TMS 6010. When no data is transmitted the output TROutput sits at a logic high. The start of the transmission is defined as the transition of TROutput from a logic high to a logic low.

Two flags are provided. A logic high on the TBREmpty flag indicates that a word has been transferred to the transmitter register and that the transmitter buffer register is now ready to accept a new word. A logic high on the TREmpty flag indicates that the transmitter section has completed the transmission of a complete word including stop bits. The TREmpty flag will sit at a logic high until the start of transmission of a new word. Both transmitter buffer register and transmitter registers are static and will perform dc storage of data.

Receiver Section

The data is received in serial form on the receiver input RInput. The data is presented in parallel form on the eight data outputs RR1 through RR8. RInput is the data input terminal. The data from RInput enters the receiver register at a point determined by the character length, the parity, and the number of stop bits. RInput must be maintained high when no data is being received. The data is clocked through the RR clock. The clock rate is 16 times faster than the data rate. Data is transferred from the receiver register to the receiver buffer register and appears on the 8 RR outputs. The MOS output buffers used for the eight RR terminals are triple-state push-pull output buffers which permit the wire-OR configuration through use of the RRDisable terminal. When a logic high is applied to RRDisable, the RR outputs are floating. IF the word length is less than 8 bits, the most significant bits will be at a logic low. The output word is right justified. RR1 is the least significant bit and RR8 is the most significant bit.

A logic low applied to the DRReset terminal resets the DReady output to a logic low. Several flags are provided in the receiver section. There are three error flags (parity error, framing error and overrun error) and a data-ready flag. All status flags may be disabled through a logic high on the SFDisable terminal.

A logic high on the PError terminal indicates an error in parity. A logic high on the OError terminal indicates an overrun. An overrun occurs when the previous word was not read, i.e., when the DReady line was not reset before the present data was transferred to the data receive holding register. A logic high on the DReady terminal indicates that a word has been received, stored in the receiver buffer register and that the data is available on outputs RR1 through RR8. The DReady terminal can be reset through the DRReset terminal.

Common Control Section

The common control section directs both the receiver and the transmitter sections. The initialization of the TMS 6010 is performed through the MReset terminal. The Master Reset is strobed to a logic high after power turn-on to reset all registers and to reset the serial output line to a logic high. All status flags (parity error, framing error, overrun error, data ready, transmitter buffer register) are disabled when the SFDisable is at a logic high. When disabled, the status flags set at a logic low. The number of bits per word is controlled by the WLSelect 1 and WLSelect 2 lines. The word length may be 5, 6, 7, or 8 bits.

The selection is as follows:

WORD LENGTH	WLS1	WLS2
5	Low	Low
6	Low	High
7	High	Low
8	High	High

The parity to be checked by the receiver and generated by the transmitter is determined by the PSelect line. A logic high on the PSelect line selects even parity and a logic low selects odd parity. The parity will not be checked or generated if a logic high is applied to PInhibit; in this case the stop bit or bits will immediately follow the data bit. When a logic high is applied to PInhibit, the PError status flag is brought to a logic low, indicating a no-parity error because parity is disregarded in this mode. To select either one or two stop bits, the SBSelect terminal is used. A logic high on this terminal will result in two stop bits while a logic low will produce only one. To load the control bits (WLSelect 1, WLSelect 2, PSelect, PInhibit, SBSelect) a logic high is applied to the CRClock terminal. This terminal may be strobed or hardwired to a logic high.

CODE CONVERTERS

A terminal system is designed to operate with one code, USASCII for example. For it to use information from sources using other than USASCII code, Selectric for example, a code converter must be included in the terminal system.

Codes are used to transfer information over data links between such equipment as peripherals, terminals, and computers.

A code word is a binary word that represents either an alphanumeric character or a command.

For instance:

The letter A is represented by 1000001 in USASCII code

The command DEL (delete) is represented by 1111111 in USASCII code

Depending on the code used, the size of the alphabet (characters and commands) may vary between 64 and 256. The number of bits in a common alphanumeric code word may vary between 6 and 8.

Many different codes are commonly used in data processing equipment. Equipment is built for a specific code and for that code only. To build a system from several pieces of data processing gear using different codes, it is necessary to convert codes.

MOS ROMs are ideally suited for code conversion. The code to be translated is fed at the input of the ROM and the output of the ROM represents the translated input code.

The most popular ROM size for code converter applications is the 2048-bit organized as 256 words x 8 bits. A ROM this size will handle all the usual codes for data transmission. (The most cumbersome code is the EBCDIC with room for 256 characters of 8 bits.) Because most codes use a 7-bit word and a 128-character alphabet, it is often possible to make a 2048-bit ROM, organized as 256 words of 8 bits, work both ways and not only translate code A into code B but also, upon command, translate B into A.

Standard Off-The-Shelf Code Converters

It is possible to program individual devices from a series to be used in different applications for use in popular code-converter applications, 3 devices from TI's TMS 2600 JC/NC series to take care of the most common codes. These devices are:

TMS 2602 JC/NC	USASCII to Selectric Selectric to USASCII
TMS 2603 JC/NC	EBCDIC to USASCII
TMS 2604 JC/NC	USASCII to EBCDIC Line Selectric to EBCDIC

These devices are presently available as off-the-shelf items.

Codes and Their Definitions

An almost endless variety of codes exists for data transmission. This causes a problem because users have difficulty in agreeing on a code, and when they do they often modify it slightly for their own purposes. Some of the most popular codes are:

Hollerith

Hollerith is used on punched cards. It is a 12-bit code with a very large alphabet (256 characters and commands). This is the code used on the 80-column punched cards as shown in Figure 3. A normal card punch machine will only punch 64 characters. Because of these limitations, the Hollerith code is not generally used for data transmission.

BCD Code (Binary Coded Decimal)

BCD is a very simple code with 64 characters of 6 bits. This is the code used with the new SYSTEM 3 IBM punched cards (96 columns, 6 bits/column).

EBCDIC (Extended Binary-Coded-Decimal Interchange Code)

EBCDIC is a widely-used code with room for 256 characters of 8 bits as shown in Figure 4.

USASCII (USA Standard Code for Information Interchange)

USASCII is the only code on which seems to agree with everybody throughout the world. The code uses 128 characters, 7 bits per character. Often, users are not interested in the full 128 characters and need only the 64 characters subset boxed within the table in Figure 5. In this case, only 6 bit per character are needed, and either b_7 or b_6 may be dropped.

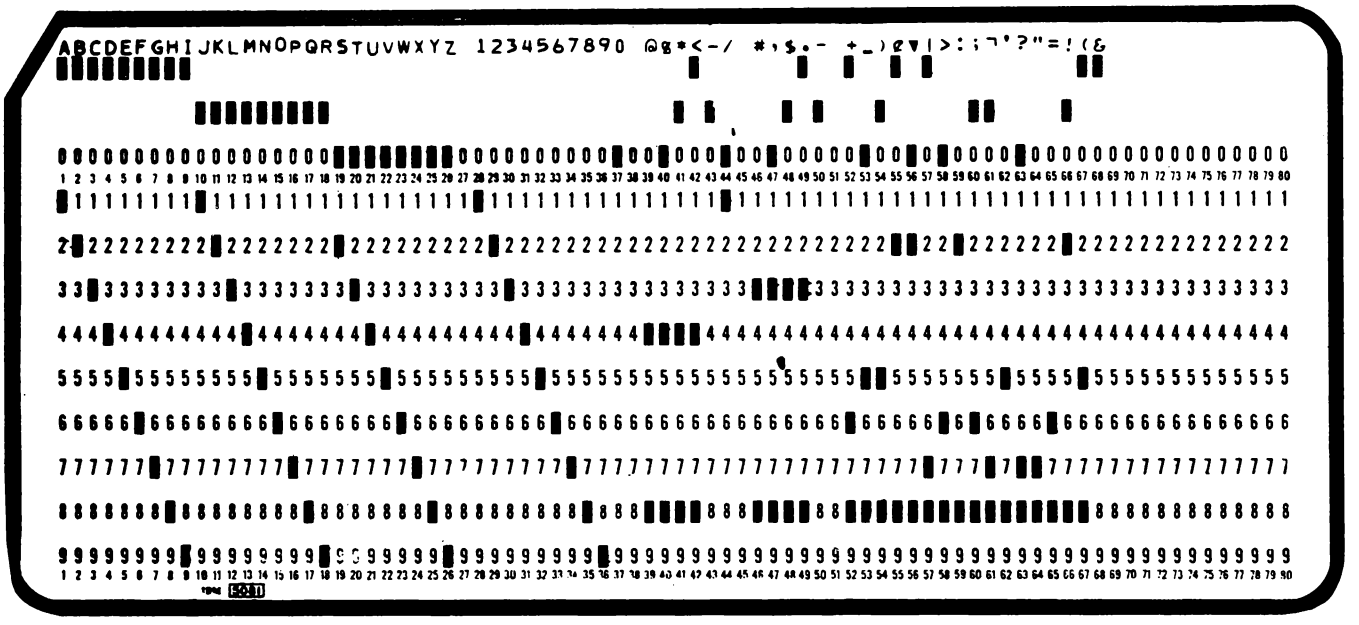


FIGURE 3. Card with Hollerith Code

Bits b7 b6 b5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 ↓	b3 ↓	b2 ↓	b1 ↓	Row ↓ Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	7	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	–	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	–	o	DEL

FIGURE 5. USA Standard Code for Information Interchange (USASCII)

b0 → / b1 → / b2 → / Bits b3 →					0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
b4 ↓	b5 ↓	b6 ↓	b7 ↓	Row ↓ / Column →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	NUL	DLE	DS		SP	&										0
0	0	0	1	1	SOH	DC1	SOS						a	j			A	J		1
0	0	1	0	2	STX	DC2	FS	SYN					b	k	s		B	K	S	2
0	0	1	1	3	ETX	TM							c	l	t		C	L	T	3
0	1	0	0	4	PF	RES	BYP	PN					d	m	u		D	M	U	4
0	1	0	1	5	HT	NL	LF	RS					e	n	v		E	N	V	5
0	1	1	0	6	LC	BS	EOB	UC					f	o	w		F	O	W	6
0	1	1	1	7	DL	IL	PRE	EOT					g	p	x		G	P	X	7
1	0	0	0	8		CAN							h	q	y		H	Q	Y	8
1	0	0	1	9		EM							i	r	z		I	R	Z	9
1	0	1	0	10	SMM	CC	SM		¢	!		:								
1	0	1	1	11	VT					$	,	#								
1	1	0	0	12	FF	IFS		DC4	<	*	%	@								
1	1	0	1	13	CR	IGS	ENQ	NAK	(	)	–	'								
1	1	1	0	14	SO	IRS	ACK		+	;	>	=								
1	1	1	1	15	SI	IUS	BEL	SUB	|	¬	?	"								

FIGURE 4. Extended Binary-Coded-Decimal Interchange Code (EBCDIC)

The international version of USASCII is called ISO. The 7-bit ISO is almost identical to the USASCII, except that certain characters may be replaced by national characters (£ instead of $ for instance). The 6-bit ISO is obtained by dropping b_6.

Selectric Line Code

Because IBM Selectric Typewriters are commonly used as terminals, several Selectric codes are being used. The most common is the IBM Correspondence Selectric Line Code. It is a 7-digit 128-character code. A certain amount of logic is necessary to go from Selectric Line Code to Selectric Bail Code shown in Figure 6.

Baudot Code

A very simple 32-character 5-bit code, the Baudot is used mainly in teletype equipment, illustrated in Figure 7.

Other common codes include: IBM System 360 8-bit code, Honeywell 64 characters, GE 64 characters, UNIVAC 64 characters, Burroughs 64 characters, and IBM 47 characters.

Custom Code Converters

Because of the proliferation of codes, TI has limited its device line to 3 standard devices, using the most popular codes. The ROMs are very adaptable to code conversion and can be programmed for this application. Because of the wide variations within a code family, in each case a truth table of the codes to be converted is needed before the device can be implemented.

The particular device is determined by the number of codes, the number of characters in a code, and the number of bits in a code word.

- TMS 2600 JC/NC (256 X 8)
  Code A → Code B
  Up to 256 characters
  Up to 8 bits per character
- TMS 2600 JC/NC (256 X 8)
  Code A → Code B
  Code C → Code D
  Up to 128 characters per code
  Up to 7 bits per character on A and C
  Up to 8 bits per character on B and D
- TMS 2600 JC/NC (256 X 8)
  Code A → Code B
  Code C → Code D
  Code E → Code F
  Code G → Code H
  Up to 64 characters per code
  Up to 8 bits/characters on Codes B, D, F, H
  Up to 6 bits/characters on Codes A, C, E, G
- TMS 4100 JC/NC (64 X 5 X 7)
  Code A → Code B, Code C, Code D, Code E, Code F
  OR
  Code A, Code B, Code C, Code D, Code E → Code F
  Up to 7 bits per character
  Up to 64 characters per code

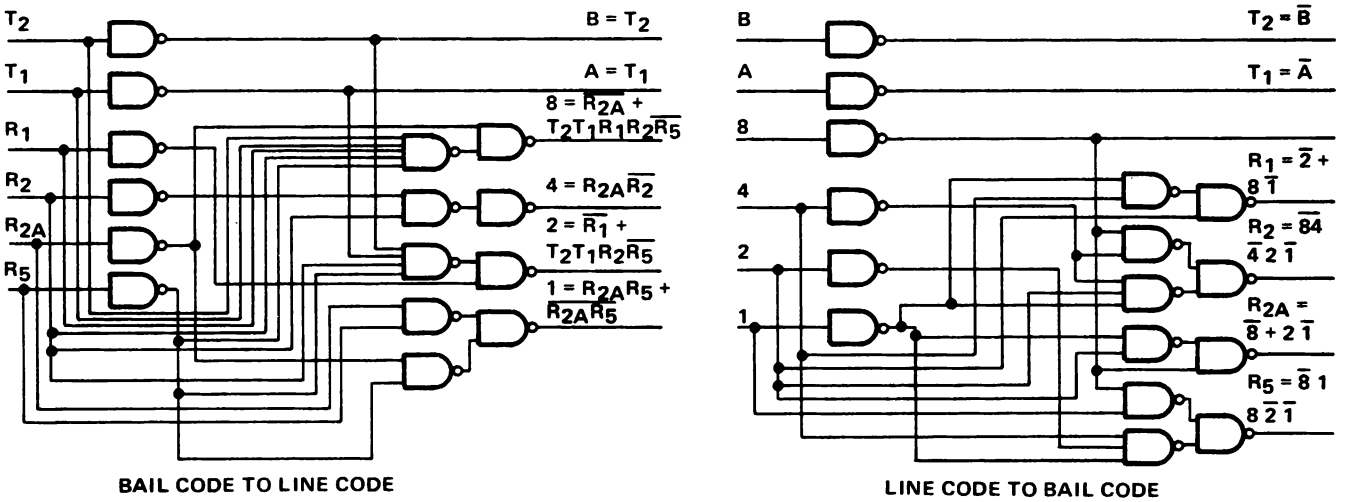


FIGURE 6. Conversion Necessary to go from Selectric Line Code to Selectric Bail Code and Vice-Versa.

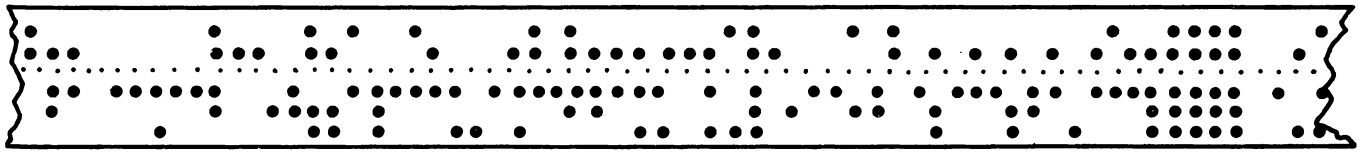


FIGURE 7. Example of Baudot Code

- TMS 4400 JC/NC (512 X 8)
  Code A → Code B
  Code C → Code D
  Up to 256 characters per code
  Up to 8-bits per character

- TMS4400 JC/NC (512 X 8)
  Code A → Code B
  Code C → Code D
  Code E → Code F
  Code G → Code H
  Up to 128 characters per code
  Up to 8 bits per character on Codes B, D, F, H
  Up to 7 bits per character on Codes A, C, E, G

DIGITAL STORAGE BUFFERS

It is often necessary to buffer information between the transmission line and a terminal. The rate of data transmission sometimes may be different from the rate of display. Such a function may be accomplished through storage registers but in this case the data is not always available at the output. A good solution for this problem is the use of an organized digital storage buffer also called Silo Buffer.

TMS 4006 JC/NC Digital Storage Buffer

The TMS 4006 JC/NC shown in Figure 8 is a data storage register with a capacity of 11 or 13 words of 6 bits each. It performs storage on a first-in first-out basis. The device employs a method of storage commonly referred to as "silo" mode.

Input and output of the digital storage buffer operate entirely independently. A word is transferred into the TMS 4006 JC/NC on the positive-going edge of the data input clock (DIC). A word is transferred out of the register on the positive-going edge of the data output clock (DOC).

The input and output clocks are completely independent of each other. There is no minimum clock rate. Logic used in the TMS 4006 JC/NC is purely static and the device has long-term retention.

Once a character is entered it will be stored temporarily in the first available register. A control logic associated with the next register will indicate whether or not that register already contains a valid word. If the next register is full, the input word will stay in the first register. If the next register is empty the word will fall down in parallel and be transferred. This operation will be repeated time after time until a full register is met. The operation is completely independent of the input, output clocks, and of all terminals.

The input word can be loaded either in serial or in parallel.

To load the device in parallel the serial parallel (S/P) control must be at a logic 1.

To load in serial, the S/P control must be at a logic 0. A marker bit will be loaded concurrently with the first shift pulse (data input clock). This marker bit will be a logic 0. In serial mode the input word will then be 7 bits (1 marker bit and 6 data bits). Parallel inputs should be held at less than −10 volts or left floating. In parallel operation, the serial input should be held greater than −1.5 volts or left floating.

The TMS 4006 JC/NC can store 11 words when operating in the serial mode and 13 words when operating in the parallel mode.

When in serial mode a word cannot be "all zero"; at least one of the data bits must be a 1.

Several outputs will allow the user to find out how much data is stored in the TMS 4006 JC/NC:

A Flag 1 output will indicate whether the first (first-in word) register is full.

A Flag 10 output will indicate whether the 10th register is full.

A flag 13 output will indicate whether the 13th register is full.

Flag outputs may be used to generate a readout command when a certain number of registers are full.

An ADIS (any data-in storage) output allows the user to detect lock-up, which may occur if power supplies are disconnected. Different outputs on ADIS and Flag 1 indicate lock-up. The register must then be cleared.

Taking the Clear input to a logical 1 clears all the TMS 4006 JC/NC register automatically.

TMS 4006 JC/NC can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: a next-register input clock (NRC), which provides the input clock signal to the next register in a cascaded string, and a previous-register output clock (PRC) which provides the output clock signal to the previous register in a cascaded string.

"TMS 4006 JC" is the part number for a unit mounted in a 28-pin ceramic dual-in-line package. In a 28-pin plastic package the device is numbered "TMS 4006 NC".

Memory Expansion

DSBs can be connected in cascade as shown in Figure 9 or in parallel as shown in Figure 10 to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions two controls are provided: an NRC which provides the input clock signal to the next register in a cascaded string, and a PRC which provides the output clock signal to the previous register in a cascaded string. There is no limit, in terms of performance, to the number of registers in a cascaded string. To extend the digit positions, the input and output control signals of a number of registers are tied in parallel. N registers tied in this fashion to store 6N digit characters can only accept characters serially in 6-bit sub-characters with the restriction that a marker pulse must proceed each 6-bit sub-character. There are no restrictions on input character format in the parallel mode.

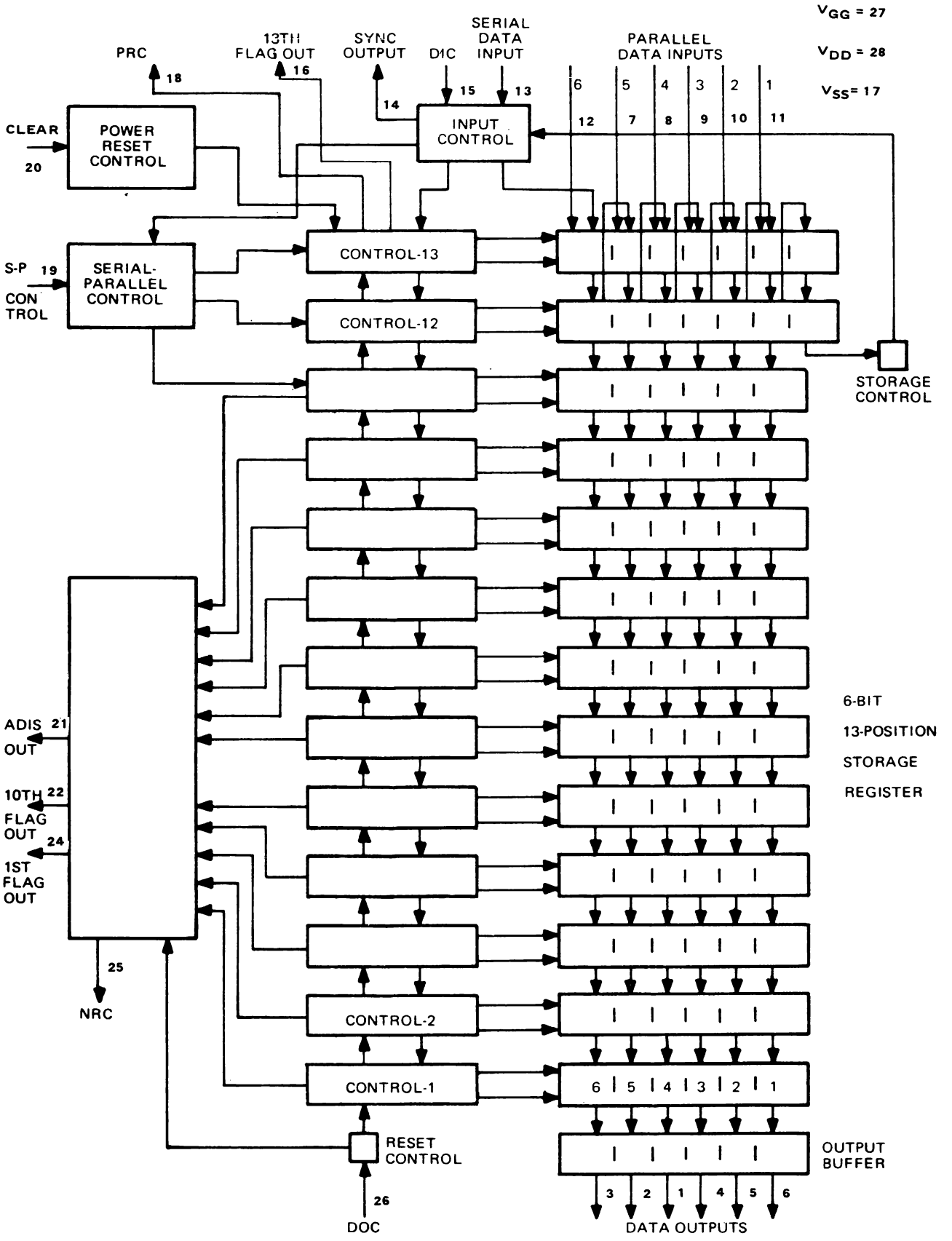


FIGURE 8. Functional Block Diagram of TMS 4006 JC/NC Digital Storage Buffer

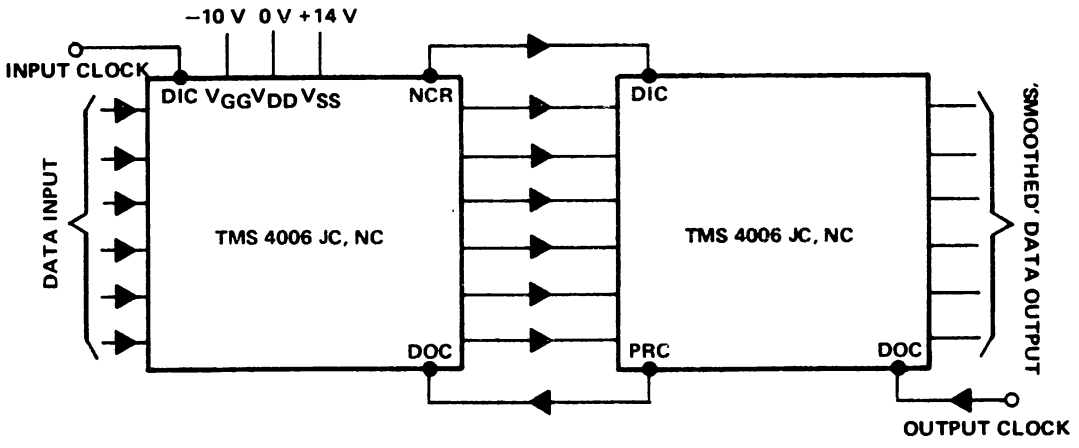


FIGURE 9. Digital Storage Buffers Cascaded

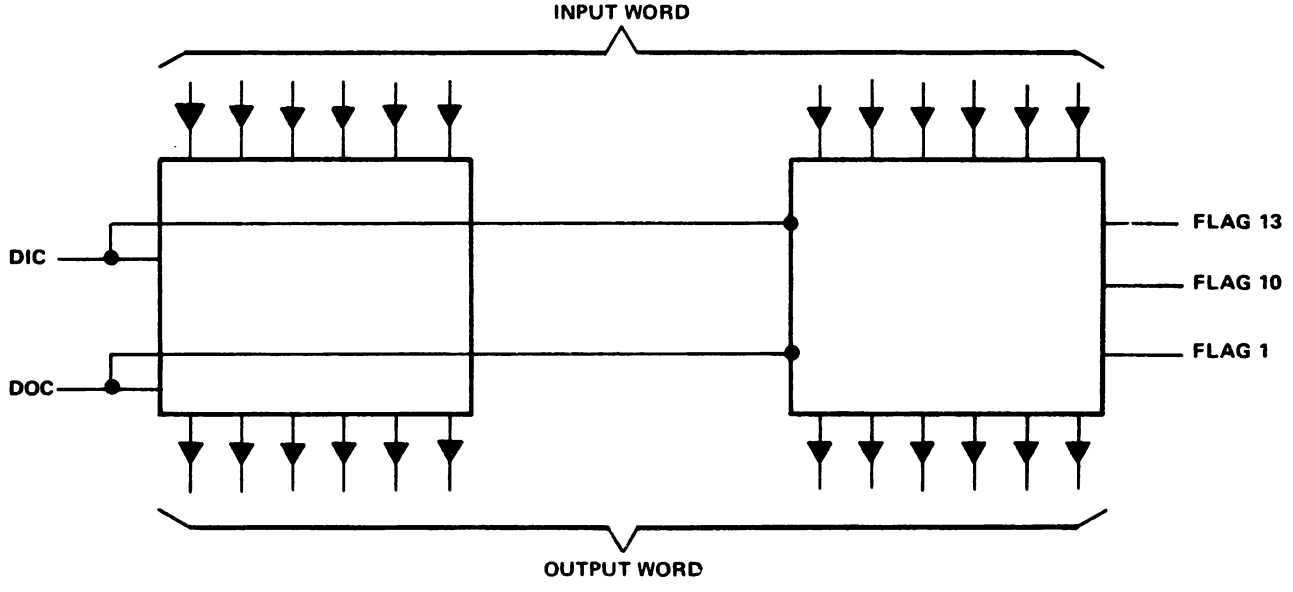


FIGURE 10. Digital Storage Buffers Paralleled

TMS 4024 JC, NC – 9 X 64 digital storage buffer (under development)

The TMS 4024 JC, NC operates as a first-in first-out store. Up to 64 words of nine bits may be stored. Data entry and data extraction are completely independent. The data is entered and extracted in parallel form. Data is always available to the outputs.

The maximum rate of data entry or extraction is 250 kHz. D-c storage of data is possible.

Terminals are provided to control data entry and extraction, to clear the entire register, and to indicate whether the register is completely empty or completely full.

The TMS 4024 JC, NC is fully TTL compatible and is mounted in 28-pin package.

MOS CHARACTER GENERATORS

MOS read-only memories (MOS ROMs) offer an extremely versatile approach to character generation. Their ease of programming allows the customer to choose without economic penalty the characters, character formats, coding and output format.

The ROM can be programmed during manufacture to store data which may be read out on command to create the image of letters, numerals, and symbols in some sort of display system such as a cathode-ray-tube (CRT), array of lamps, or matrix-type printer.

This report describes the MOS character generators now available from Texas Instruments and shows how they can be used to advantage in display systems. These miniature devices can store more than 2000 bits of data (enough for 64 characters in one device) and include addressing and decoding circuitry. The MOS circuitry is static rather than dynamic. No clocking is required.

Speed performance of static MOS ROMs is adequate for both low-speed applications and high-speed CRT data

displays. Their small size and low power consumption in addition to their low cost make them attractive replacements for existing character generators in many display systems.

As only one photo-mask needs to be changed during manufacture, quick response to customers' orders is possible. Standard devices with USASCII character coding are available off the shelf.

Character generators can be divided into two broad categories: tube types and digital memories. MOS character generators, an advanced type of the latter category, are supplanting generators of the former group.

Fundamentals of Character Generators

Tube-type character generators take various forms. Some like the *monoscope* consist of an electron gun, electrostatic deflection plates, and a target on which the characters are formed. In a character generator of this type, an incoming digital code specifying the character to be displayed is first converted to deflection voltages. The electron beam is deflected accordingly to the appropriate target location which contains a metallized image of the desired character. This beam then scans the target in synchronism with the beam in a cathode-ray tube (CRT) display. Secondary emission from the metal image provides a video signal for the CRT, reproducing the character on its face.

In some CRT displays the character generation is performed within the CRT itself. In this case, a thin metal *stencil* with character shapes etched through is used to extrude the beam to the desired character shape. After leaving the gun, the beam is deflected to a character location on the stencil, passes through the stencil, and is converged to the tube axis. It is then deflected again, this time to a position on the CRT face, where the shaped beam causes the selected character to appear.

With these tube-type character generators, the digital code specifying a character must first be converted to positional information before character selection can be achieved. On the other hand, digital character generators use a more direct approach than the tube type. Digital types generally consist of a read-only memory (ROM) in which a given input code produces a digital output describing a character specified by the user. This digital output is then converted into a visual image as described below. The use of ROMs for character generation eliminates the need for bulky tubes or special-purpose CRTs. They can also be used in non-CRT applications such as billboard displays and matrix type printers.

There are many different output code schemes that might be designed into an ROM character generator. However, the dot matrix output format is perhaps the easiest to visualize and use. Consider a 5 X 7 dot matrix used to present the letter A as shown in Figure 11. If each of the dot positions is a lamp, then the dots in the letter A are *on* lamps, while the others are *off*. The *on* lamps correspond to logical 1 outputs of an ROM with a 35-bit output word, while the *off* states correspond to a logical 0 output. In CRT displays, the same logical two-state output can be used to blank and unblank the beam. A sequential output from an ROM is generally more desirable than 35 parallel outputs because video information can be supplied as the beam is moving.

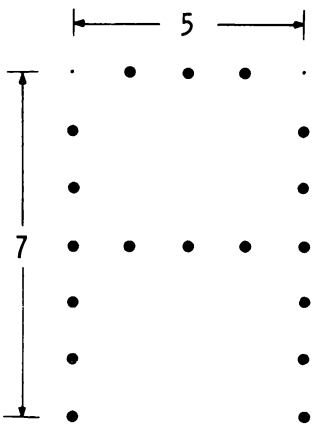


FIGURE 11. Letter "A" in 5 X 7 Dot Matrix

The dot matrix format is usable in display applications including billboards, print-head drivers, and CRT displays of both the X-Y and television raster-scan type. A 5 X 7 dot matrix is considered the minimum size necessary to display a normal keyboard complement of letters, numbers, and symbols with adequate legibility. Other matrix sizes, such as 7 X 9 or 5 X 14, may be required for special symbols or improved resolution.

MOS Character Generators From TI

In order to use a ROM to generate a variety of characters a large ROM is necessary. For most display applications 32 characters is a bare minimum. A 64 character alphabet corresponds to a wider range of applications. Certain data display applications will necessitate as many as 96 or even 128 characters. The size of the dot matrix used depends on the definition needed for the display. Most human factor experts agree on the fact that a 7 X 5 character font presents enough definition for most applications while a 7 X 9 character font is much more eye pleasing. A 7 X 9 font permits, for instance, a good representation of complex characters such as the dollar sign and the ampersand. The total number of bits needed is as follows:

32 characters 7 X 5	1120 bits
64 characters 7 X 5	2240 bits
128 characters 7 X 5	4480 bits
64 characters 7 X 9	4480 bits
128 characters 7 X 9	8960 bits

It would be costly and awkward to implement such a large number of bits through diode or classical bipolar logic. Core memories require special drive and sense circuits and are difficult to modify for different customer character requirements. In the past two years MOS ROMs have proved to be the answer as far as character generators are concerned. The cost per bit of MOS ROMs is very low (presently around 1/2 cent per bit in production quantities) and the fact that the shape of the characters can be easily modified by changing a single mask during the fabrication of the devices has proved to be extremely appealing to display manufacturers. MOS ROMs provide significant savings in cost, weight, size and power consumption.

Texas Instruments manufactures several series of ROMs specially architectured for displays.

Device	Characters	Matrix	Logic
TMS 2400 JC, NC	64	7 X 5	Row output
TMS 2500 JC, NC	64	7 X 5	Row output
TMS 2500 JC, NC	32	7 X 9	Column output
TMS 4100 JC, NC	64	7 X 5	Column output
TMS 4100 JC, NC	32	14 X 5	Column output

All these devices have been designed with static logic source permits the simplest system design and eliminates the need for the special clocking circuits required by dynamic MOS configuration.

The main differences between the different types of ROMs offered by TI lies in the way the characters are extracted out of the ROM.

Let's take a 7 X 5 dot matrix as an example. This corresponds to 35 dots; that is 35 bits of information.

One may want to extract all 35 bits at the same time. This will be called a parallel output character generator. Or one may want to scan through the character. This is what is done in most CRT displays. One may want to scan through the character one column at a time (column output) a one row at a time (row output). Each organization will be most suited for particular applications.

The TMS 2500 JC, NC series allow the user to display one out of 64 characters on a 7 x 5 matrix. Rather than having all outputs available simultaneously only one row of the dot matrix is available at a time. By addressing the 3 row select lines as shown in Figure 12 the corresponding row is displayed on the output. The direct character font of the TMS 2501 is represented in Figure 13.

The 3 bit row address input is internally decoded in 8 row select inputs. Only 7 of them will be used for most display applications. The TMS 2500 JC, NC will find its application in raster scan displays (TV monitor type displays). The TMS 2500 JC, NC may also be organised as 32 x 7 x 9 for 7 x 9 font column output applications.

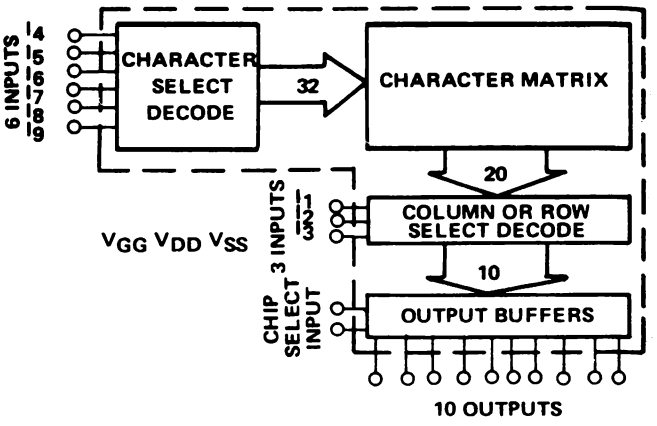


FIGURE 12. Functional Block Diagram of TMS 2500 JC/NC ROM

The TMS 2400 JC, NC series is similar in organization to the TMS 2500 JC, NC. The main differences between the two series lies in the process used during the manufacturing of the device. The TMS 2400 JC, NC is manufactured with high threshold process while the TMS 2500 JC, NC features a low VT process, providing easier interface with bipolar logic families such as TTL and DTL.

The TMS 4100 JC, NC series have been designed for use in CRT and billboard displays.

Rather than having all outputs available simultaneously, only one column of the dot matrix is available at a time. By driving one of the five column-select inputs shown in Figure 14, the corresponding column is made available at the output. The memory can be internally organized at the customer's option to provide 64 characters in a 5 X 7 dot matrix or 32 characters in a 5 X 14 matrix. In either case, a total of 2240 bits of storage is available for use.

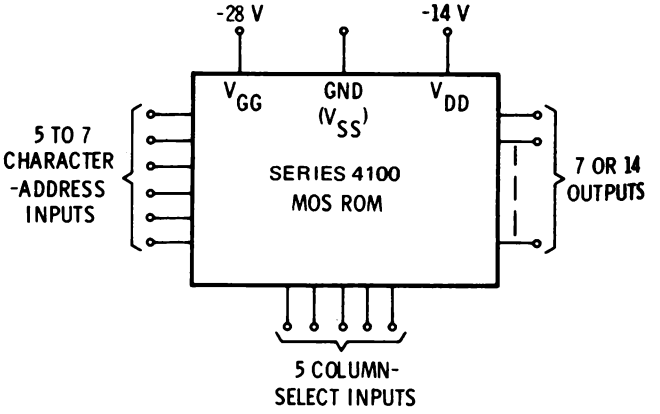


FIGURE 14. Pin Functions of MOS ROM from TMS 4100 Series

An alternate organization of the TMS 2500 JC, NC permits display 32 characters on a 8 X 10 (reduced to 7 X 7 for most applications) character font. The character is then extracted out of the ROM one column at a time.

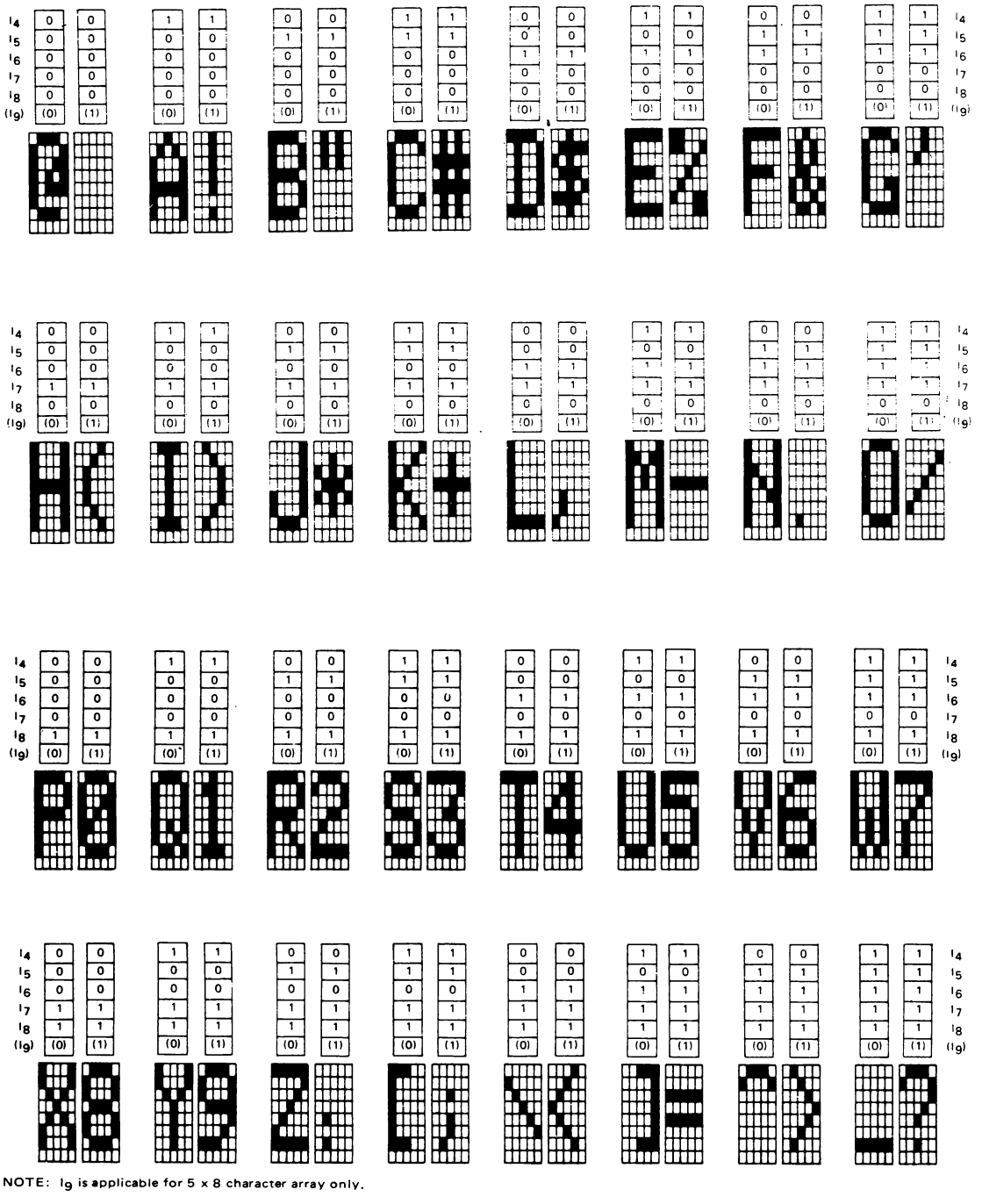


FIGURE 13. TMS 2501 JC/NC Character Font

The TMS 4100 JC, NC series is available in a 28-pin dual-in-line ceramic or plastic package. If a 5 X 7 output matrix is chosen, seven of the fourteen outputs are not used. One device in this series is a standard product. The TMS 4103 character generator accepts USASCII input coding and provides 64 standard characters in a 5 X 7 dot array. Two supply voltages are required, −14 V and −28 V as shown in Figure 14. Total power dissipation is under 40mW, and an entire character can be obtained in less than 1.5 μs.

Internal Circuitry and Construction

The memory matrix of the 4100 series consists of 2240 P-channel MOS devices arranged in a 32 X 70 array. As shown in Figure 15, the 32 horizontal lines drive the MOSFET gates, while their drains are connected to one of the 70 output lines. Every device has its source grounded. When one of the 32 gate lines is driven negative, those devices which have their gate connected are turned on, pulling down the voltage of the corresponding output line. Whether a gate is connected or not is determined by mask programming, with a connected gate corresponding to a dot in the output format.

The block diagram in Figure 15 shows the interconnection of all circuits in an ROM of the TMS4100 series: the decoder, memory array, and output selection circuitry. When 32 characters with a 5 X 14 matrix are desired, one character is coded on each of the 32 gate lines. The decoder accepts a 5-bit, 6-bit, or 7-bit input code and drives one of these lines negative. Application of a column-selects 14 of the 70 drain lines corresponding to one column in the 5 X 14 matrix. These 14 lines are connected through buffers to the output terminals.

If 64 characters with a 5 X 7 matrix are desired, two characters are encoded on each of the 32 gate lines. Five of the six bits (or six of seven) in the input code are used to drive the decoder, with the sixth bit as shown in Figure 15 connected to the output buffer to choose between the two characters.

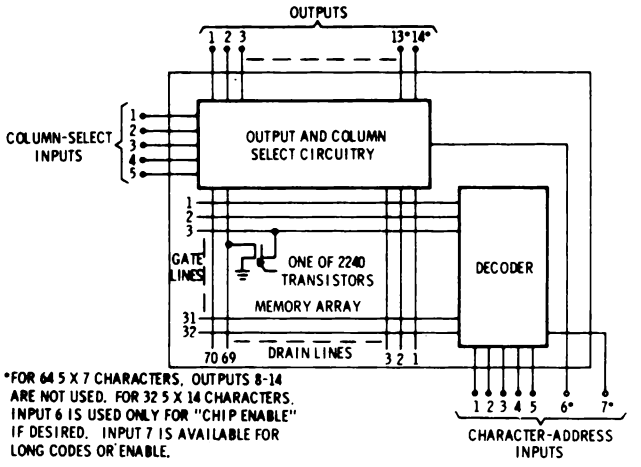


FIGURE 15. Functional Diagram of all Circuits within an MOS ROM of the TMS 4100 Series

The block diagram of the TMS 2500 JC, NC has previously been shown in Figure 12. The basic configuration of the device is 32 X 8 X 10. In this basic organization 5 inputs are decoded into 32 lines in the character select decode line then 32 metal lines are routed to the character matrix which presents 2560 (32 X 8 X 10) transistor locations, 80 lines emerge from the machine. The column or row select decoder determines which group of 10 lines is sent to the output buffers. Finally a 2 bit chip select word is used to determine whether the true output will appear on the output buffers or if they will be left floating. This permits one to build much larger memory systems with the TMS 2500 JC NC.

If a 64 X 8 X 5 organization is chosen the outputs are hardwired two at a time. A sixth character input will be used to determine which character must appear on the outputs.

Programming of the MOS ROMs is done at the second-oxide-removal processing stage. Unused transistors have a layer of thick oxide over their gate regions (Figure 16). The other masks used during the process are the same for all the devices in one series. Fully computerised methods

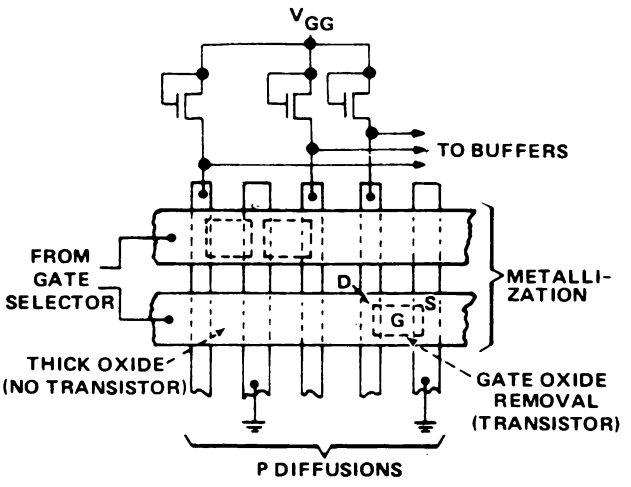


FIGURE 16. An MOS Transistor can be Either Constructed or Omitted by Growing Either a Thin-Gate Oxide or a Thick-Gate Oxide

are used to cut the second-oxide removal mask ensuring fast turnaround time and completely eliminating code errors. The customer fills input sheets representing the desired patterns. After encoding, a computer printout is overlayed on the customer inputs for checking purposes. The artwork is then cut on a computerized table.

Power Supply Requirements

Two power supplies are required, V_{DD} and V_{GG}. The TMS 2500 JC, NC uses a V_{DD} of −5 V and a V_{GG} of −17V. In most systems the designer will want to translate all power supplies up by 5 V and the following voltage V_{SS} +5 V, V_{DD} = 0 V, V_{GG} = −12 V. This will permit a TTL device interface. The typical power dissipation of this device at 250°C is 280 mW. V_{DD} and V_{GG}, are nominally −14 V and −28 V for the 2400, 4100 and 4800 series devices. No current is drawn from the −28 V V_{GG} supply, since it is internally connected only to MOS gates. About 25 mA is drawn typically by the memory array from the −14 V V_{DD} supply at 20°C ambient temperature, resulting in a 350-mW power dissipation. Additional power is dissipated in the output buffer devices, depending on the external output conditions. In most cases the designer will translate all power supplies by 14 V, and use V_{SS} = +14 V, V_{DD} = 0 V, V_{GG} = −14 V as power supplies. This will also simplify TTL interface.

Address and Select Inputs

The TMS 2500 JC, NC series use an exhaustive decoder (6 inputs in 64 x 8 x 5 organisation, 5 inputs in 32 x 8 x 10 organization). It uses a 3 input address for the row (or column) select.

All of these inputs are connected to MOS gates. Each input is protected by a field-plate zener diode against gate damage due to static charge accumulation. Because only gates are being driven, the inputs appear capacitive and require no current other than the small leakage current associated with the protective zener.

The 4100 series devices have five to seven character-address and five column-select inputs. The 2400 series devices have the same five to seven character-address inputs but only three row-address inputs.

The nominal logic voltage on the inputs are the following:

Logic High V_{SS}
Logic Low V_{DD}

In the case of a custom programmed device the user can choose either positive or negative logic. TI has chosen to use positive logic (high=1) for all low threshold devices such as the TMS 2500 JC, NC series and negative logic for high threshold devices such as the TMS 4100, 2400, series. This leads to the following input definition:

TMS 2400, 4100, 4880 Power supply +14 to −14

	MIN	NOM	MAX
High = 0	+11 V	+14	14.3
Low = 1		0	3 V

TMS 2500 JC, NC Power supply +5 to −12

	MIN	NOM	MAX
High = 1	3.5	5	5.3
Low = 0		0	3 V

Output Characteristics

The TMS 2500 JC, NC features a triple-state push-pull output buffer connected between V_{SS} and V_{DD}. This will permit direct TTL capability. The fan-out of the TMS 2500 buffer is 2 TTL gates.

The 4100 series character generators have a single transistor with an open drain at the output which can be returned to a negative voltage through external circuitry. The 2400 series can be programmed to have either a single transistor open drain output or a MOS push-pull output. A schematic showing a portion of the relevant internal MOS circuitry for the 4100 series appears in Figure 17. When a dot is to occur, the output device is turned on, pulling the drain toward ground. Otherwise, the device remains *off*.

As in a discrete MOSFET, the drain current of the output buffer is affected by its drain-to-source voltage V_{DS} and gate-to-source voltage V_{GS}. The value of V_{DS} is dependent on the external circuitry being driven, whereas V_{GS} is determined internally.

Speed Performance

The output current of an MOS character generator does not change instantaneously after a new input is applied. A delay occurs which is dependent on the following factors: the character program within the memory; whether a character-address, row-address or column-select input is changed; the characters involved if character address is altered; the direction of output change-*on* to *off* or *off* to *on*.

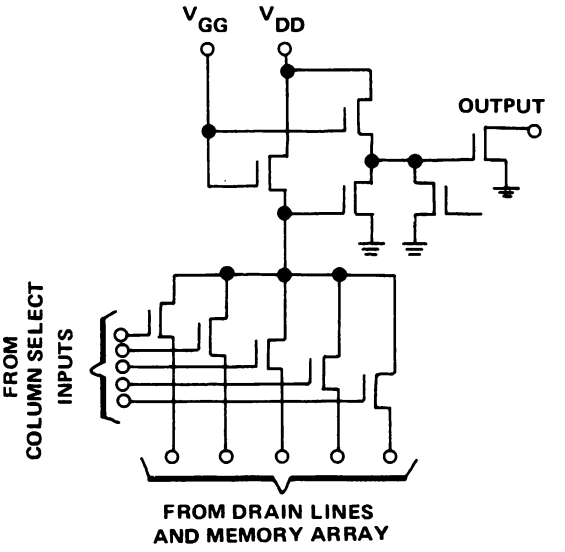


FIGURE 17. Portion of Output Circuitry in TMS 4100 Series MOS ROMs

A primary source of delay is the charging of the gate lines in the memory array. The more gates connected or the more dots programmed in the character, the larger the capacitance and the longer the time required to charge the line. Position of the character storage area in the matrix also affects delay due to the distributed-RC nature of the diffused drain lines.

Response to a character-address change involves the longest delays. Beginning with an output initially *off*, if a column or row is selected and an input code is applied that will result in the output turning *on*, the resulting output current has the appearance in Figure 18(a). If the output is initially *on* and being turned *off*, Figure 18(b) is applicable.

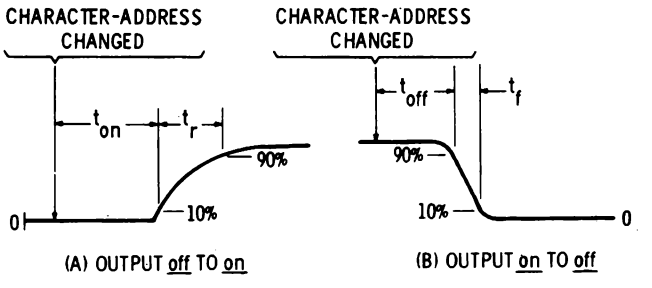


FIGURE 18. Voltage Response of an MOS ROM Output When Switched by a Character-Address Change

For a given character, t_{on} is always greater than t_{off} because the output resistance of the decoder is greater when charging a gate line than when discharging it. Because these delay times are dependent on the particular character format desired by a customer, no definite values can be assigned to t_{on} and t_{off} for all memories.

Within a given memory, both t_{on} and t_{off} can vary, depending on the character chosen. Variations from 200 ns to 350 ns for t_{on} and from 60 ns to 160 ns for t_{off} have been observed in one member of the 4100 series.

Turn-on and turn-off delays also exist when a column is enabled or disabled with a character-address input already applied. Both of these delays are typically less than 100 ns for the 4100 series.

The current rise time at an output is always greater than the fall time. Rise times can be as long as 200 ns while fall times are generally less than 100 ns.

The discussion of the speed is not only theoretical. There are many cases when the system design makes a maximum access time mandatory. When a plain TV monitor (625 lines) is used, the image is regenerated 25 times per second. If the desirable 80 characters per line of test is to be used a character must be obtained every 625ns.

At 400 ns over this temperature range the TMS 2500 has speed to spare. The access times of the different character generators offered by TI are as follows:

	TMS 2400	TMS 2500	TMS 4100
Characteristics	900 ns	400 ns	700 ns
Row (column) select	750 ns	300 ns	300 ns

Input and Output Interfacing

The TMS 2500 JC, NC interfaces directly to TTL, DTL as seen in Figure 19. All inputs, outputs, chip select and column select lines are directly TTL compatible without external components.

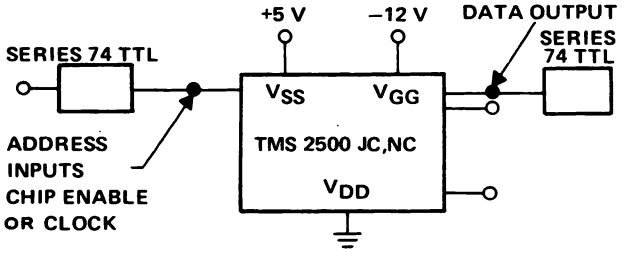


FIGURE 19. Interfacing TMS 2500 JC/NC With Series 74 TTL

As far as the TMS 4100, 2400 series are concerned interfacing is most easily achieved when the ground of the MOS device is brought above the TTL ground as shown in Figure 20 and Figure 21. In this configuration the character-address, row-address and column-select voltages do not have to swing below ground. Consequently, TTL open-collector gates or MSI decoders can be used at the character-address, row-address and column-select inputs. The SN7416 open collector TTL gates are ideal for this purpose. Discrete NPN transistors may also be used with their bases driven by a TTL output; The 2N3014 or its plastic version the 2N4420 is recommended for this application.

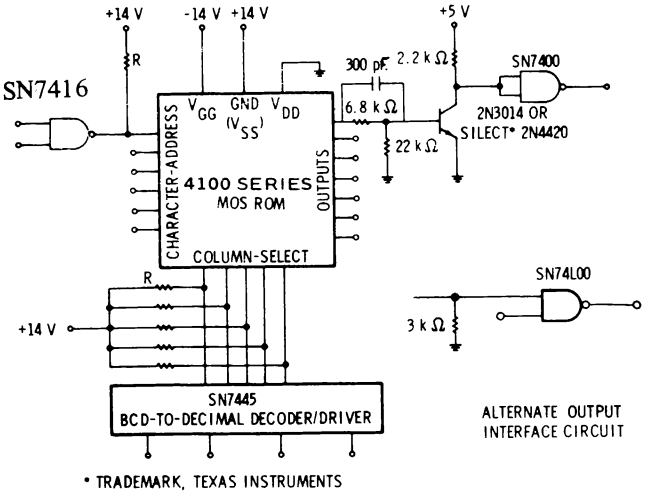


FIGURE 20. Interfacing a 4100 Series MOS ROM with 54/74 TTL

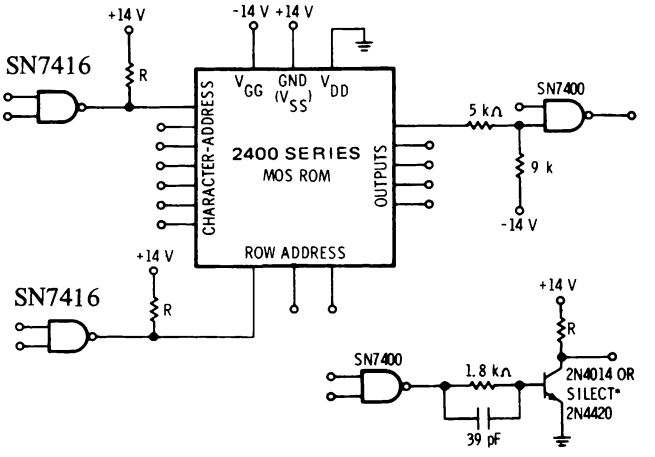


FIGURE 21. Interfacing a 2400 Series MOS ROM with 54/74 TTL

While either the open-collector gates or NPN drivers could be used at the column-select inputs, an MSI decoder such as the SN7445 may be more convenient since only one output at a time needs to be enabled. The value of load resistance R should be about 2 kΩ for high-speed operation. It may be increased at lower speeds to lessen current drain.

Output interface circuitry must convert the current output of the character generator to a voltage swing capable of driving a 54/74 TTL input. It should not respond to the maximum leakage current for an *off* output, but must respond to the minimum current for an *on* output.

A simple circuit which meets these requirements for the 4100 series is the NPN transistor inverter shown at an MOS ROM output in Figure 20. The 22kΩ base resistance assures that the transistor will not be turned on with an ROM output leakage current and transistor leakage current (I_{CBO}) of 20 μA. A 2.2-kΩ load resistance assures that a good logical 0 appears at the TTL input when the ROM

output current is *on*. A 6.8-kΩ resistance has been added in series with the MOS output to limit power dissipation in the memory, while the 300pF capacitor maintains switching speeds. As an alternative, use of low-power 54/74 TTL for the output interface circuitry only requires a 3-kΩ resistor to ground, to convert the character generator output current into acceptable logic voltages.

Interfacing from the 2400 series outputs to 54/74 TTL inputs requires 5-kΩ and 9-kΩ resistors from the MOS ROM output to −14 V, as shown in Figure 21.

In some applications not every output needs a separate interface circuit. The system in Figure 26 which is discussed in the next section, requires only one interface circuit for seven outputs.

MOS CHARACTER GENERATORS IN DISPLAY SYSTEMS

In most display applications, parallel outputs are neither necessary nor convenient and the 4100 series of MOS ROMs, with their column output capability, are useful in a wide variety of areas from billboard displays to high-speed CRT data terminals.

A moving billboard display could be arranged as shown in Figure 22. The seven character-generator outputs each drive one lamp in the far right column. Each pattern

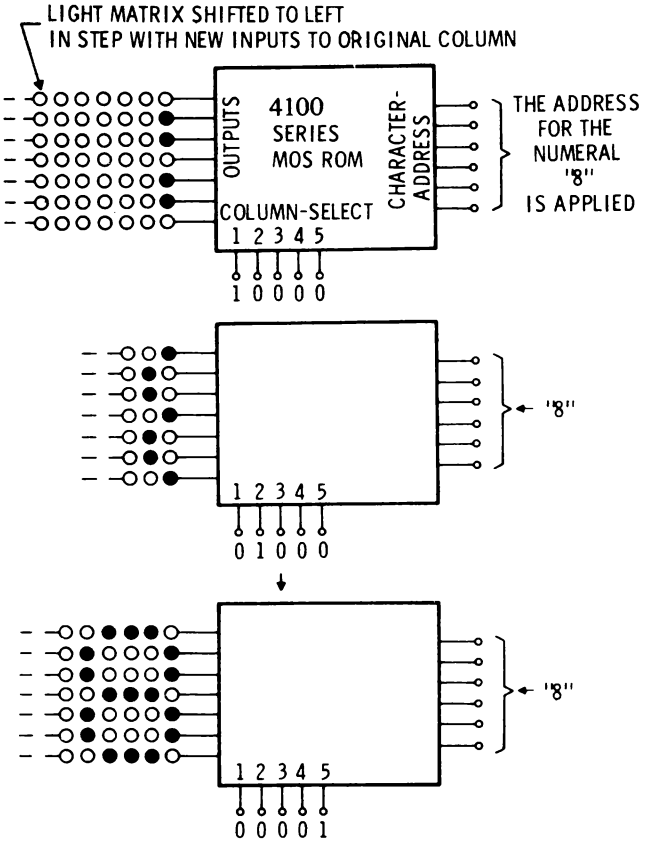


FIGURE 22. Functional Diagram of a Moving Billboard Display Using One MOS ROM for Character Generation

entered at the right is shifted to the left by other logic circuits in synchronism with the changes of column-select inputs. After five shifts the entire character is visible. All column-select inputs are then disabled so that spaces can be entered in the light matrix between characters.

A column-output character generator can also be used to obtain printed characters. The seven outputs can be connected to a column of seven light-emitting diodes arranged over a strip of moving, light-sensitive paper or film. Movement of the paper provides the spacing between columns as the column-select inputs are sequenced.

The logic block diagram of a system for displaying a single character on a CRT is shown in Figure 23. Two

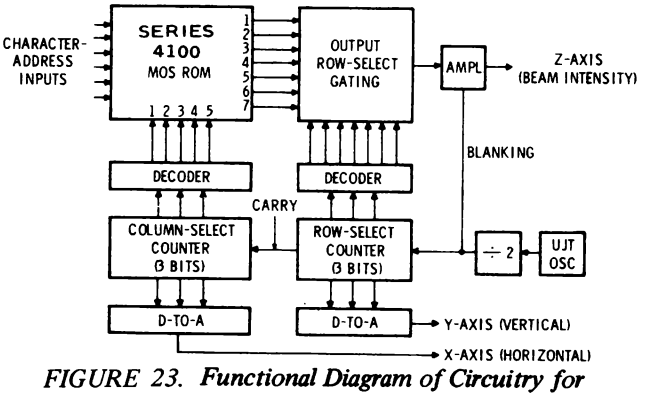


FIGURE 23. Functional Diagram of Circuitry for Projecting One Character on a CRT Using an MOS ROM

counters are involved; one sequences through the seven outputs of an MOS character generator while the other selects a column. A digital-to-analog converter connected to each counter provides a staircase waveform for vertical or horizontal deflection. The scanning sequence is shown in Figure 24. It begins at the bottom-left dot position of

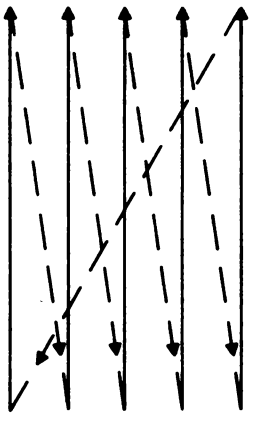


FIGURE 24. Scan Pattern for Single Character CRT Display Generated by an MOS ROM Using Method in Figure 23

the 5 X 7 dot matrix and ends at the top-right position before retrace. At the end of each vertical column scan, the row-select counter resets and advances the column-select counter to the next column position. An entire scan over the 35 dot positions must be repeated rapidly enough so

that flicker of the display is not apparent. A rate of 60 Hz is generally considered adequate for all standard CRT phosphors and brightness levels.

Waveforms showing the relationship between the deflection signals, Z-axis output, and counter conditions are shown in Figure 25 for the first two columns of the number "8". The Z-axis output is always low while the beam is being stepped between dot positions and remains low for a portion of the dwell time at a dot position. This blanking allows the display system to be used with an ordinary laboratory oscilloscope having an ac-coupled Z-axis input. It also eliminates all potentially visible retrace lines. Without blanking, the output would not fall when stepping between *on* dots. The beam would stay turned on between steps, creating dc restoration problems with an ac-coupled Z-axis.

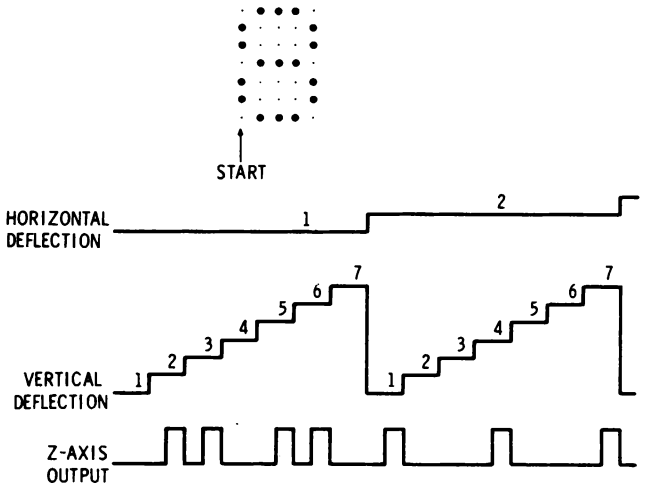


FIGURE 25. Deflection and Z-Axis Signals for Single-Character CRT Display as in Figure 13.

The single-character display system just described is implemented in Figure 26 using TTL for the counters. decoder, and D-to-A conversion. A UJT oscillator running at 4.2 kHz is first divided by two to produce the blanking signal for the Z-axis amplifier. As the blanking signal is applied, the row-select binary counter is clocked. The resultant count is converted to an analog voltage by a 3-bit D-to-A converter consisting of three open-collector TTL inverters and a modified binary ladder network, causing a vertical movement of the beam. When the row-select decoder senses the eighth state of the binary counter, it resets this counter and clocks the column-select counter. An identical D-to-A converter provides the horizontal deflection signal.

The decoder, a SN7445N, used for the column-select counter, interfaces directly with the MOS character generator, using load resistors. The decoder outputs have a 30-V breakdown potential and can sink up to 80 mA.

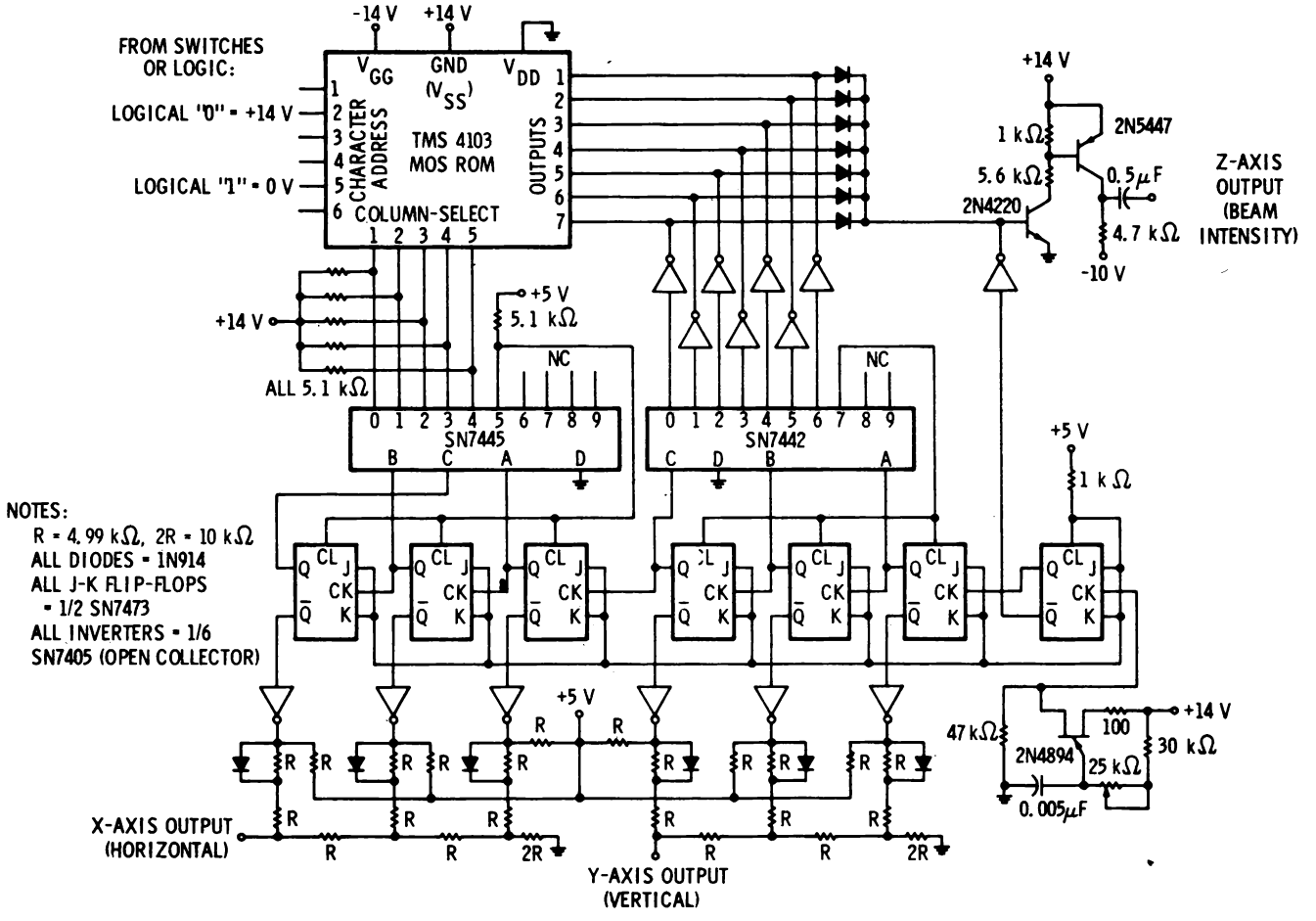


FIGURE 26. Complete Circuit for Single Character CRT Display System in Figure 23

The decoder for the row-select counter drives open-collector TTL inverters which together with the diode array allow only one output from the character generator to drive the output amplifier. This simple arrangement eliminates the need for separate interface circuits on each output and can be used at high speeds as well as the speeds encountered in this system.

In Figure 27 is shown a photograph of the number '8' obtained with this system and an ordinary oscilloscope having decoupled X and Y inputs and an a.c. coupled Z input. Size and aspect ratio of the character can be adjusted by the gain controls on the scope, and dot size can be varied with the focus and astigmation controls.

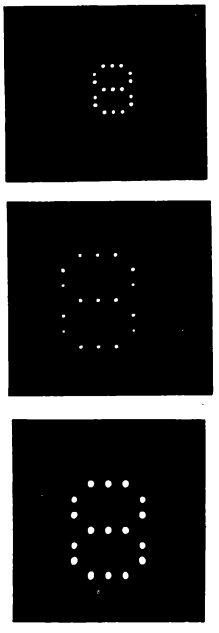


FIGURE 27. Scope Photos of Numeral "8" Obtained Using an Oscilloscope and the Circuit of Figure 26
Different sizes and appearances result from adjusting oscilloscope gain, focus and astigmation controls

The extension of the single-character display system just discussed to a system capable of displaying one entire line of characters is relatively straightforward. The column-select decoder must first be modified so that spaces can be inserted between characters. Two column widths are sufficient, and are easily obtained without extensive modification as shown in Figure 28. All columns are disabled for the first two counts of the column-select counter so that no Z-output can occur during this time. (The spacing delay may be used to address a new character in the ROM.) A character-address counter is advanced when the column-select counter resets. The binary outputs of this counter drive a D-to-A converter with as many output voltage steps as there are characters, each step having a height equal to seven column-select steps. Summing of the column-select and character-select D-to-A converter outputs results in the total horizontal deflection signal.

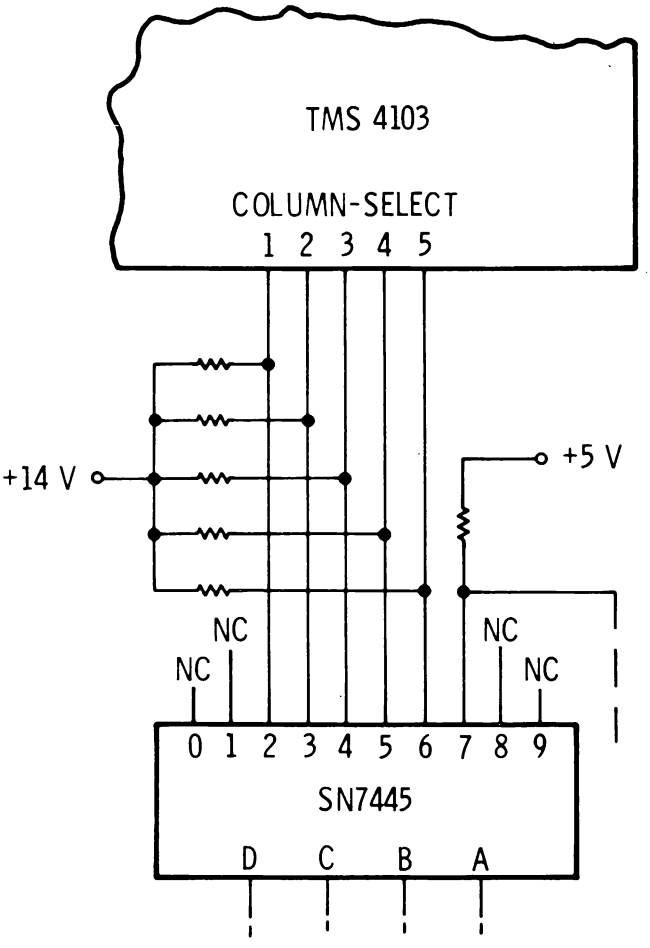


FIGURE 28. Modification to Column-Select Decoder in Figure 26 for Character Spacing

A new character input is applied to the MOS character generator each time the character-address counter advances. This may be achieved by clocking MOS shift registers containing the character codes of the characters to be displayed at each reset of the column-select counter.

As the number of characters on a line becomes large, the horizontal deflection voltage approaches a sawtooth waveform. In practice, a sawtooth can actually be used, eliminating the need for two D-to-A converters. A linear ramp generator which is reset when the character-address counter resets, provides a suitable horizontal signal if a slight tilt to the characters is permissible.

By adding still another counter, several lines of characters can be displayed. This line-address counter is advanced when the character-address counter resets. A D-to-A converter provides a staircase waveform with as many steps as there are lines. This staircase waveform is summed with the staircase waveform from the row-select converter to provide the total vertical deflection signal. The basic organization of this system is apparent from the above.

TV Character Displays

Most CRT displays presently being built use raster scan. This is a TV type of sweep. A raster type CRT is very similar to a TV monitor. As a matter of fact, some manufacturers actually use TV monitors for their displays. The CRT beam is swept in a raster of lines by applying a synchronized voltage range to the X and Y deflection circuits.

The image is formed by modulating the beam intensity with a video signal at appropriate times during the raster sweeps.

Typical commercial TV video is essentially an analog signal. There are many shades of gray between pure white and jet black. For a display, we can simplify the video and use only two levels of intensity – black and white. Thus, the video signal can be fed into the CRT as a series of Os and 1s and the image can be made up of a series of dots and blanks that are interpreted as lines, characters, etc.

NOTE: The price of colour TVsets has also come down and for this reason several manufacturers have put four-colour CRT displays on the market.

Advantages

- Economical hardware (TV)
- Simple deflection circuits
- Simple digital logic
- Economical refresh
- Constant flicker rate independent of information

Disadvantages

- Use of light pen is difficult
- Need storage even for blank areas of the screen
- If data is not alphanumeric, data preparation is cumbersome

The most common character fonts for raster scan CRT displays employ 5 X 7 or 7 X 9 matrices.

In a CRT display, only one dot of a character can be presented at a time. For this reason, video information to blank and unblank the beam must be completely serial. Therefore any parallel outputs of a character generator must be sequentially inspected.

In a raster-scanned display like that in conventional television the CRT beam moves vertically after a complete horizontal sweep. Control of the beam to obtain the scanning pattern in Figure 24 for each character is not readily available. It therefore becomes desirable when using a dot-matrix MOS character generator to display only a portion of a character at a time, rather than scan over a complete character before going on to the next one.

One row from each character in a line of characters can be presented during one horizontal sweep as shown in Figure 29. A total of seven sweeps is required to display a character with 5 X 7 dot matrix. Since conventional TV displays use interlaced scanning, alternate rows must be displayed in each field, i.e. rows 1, 3, 5, and 7 in one field and rows 2, 4, and 6 in the other.

The character generator output for this kind of display should consist of five parallel outputs chosen on a row-selectable basis. Speed requirements prevent a column-selectable ouput, such as provided by the 4100 series MOS ROMs, from being used effectively. For this reason the 2500 series of row-selectable devices has been developed.

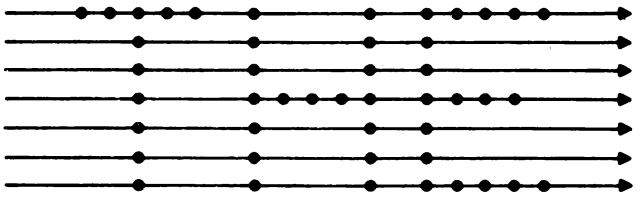


FIGURE 29. Raster Scanning of Dot Matrix Characters as in a Television Picture Tube

The 2500 series character generators are functionally very similar to the 4100 series. The TMS 2500 contains 2560 bits of storage with 2240 bits used in most applications. Both decode character-address inputs into 32 characters, each containing 70 bits. As with the 4100 series, one input can be programmed so that the ROM organization becomes the equivalent of 64 characters, each with 35 bits of information. However, the 2500 series also has 2 chip-enable input which can open (turn off) all outputs simultaneously. The outputs of the 2500 series consist of five output lines, one for each column of a 5 X 7 matrix. Row selection is achieved by three coded inputs, I_1, I_2 and I_3, which are decoded by the 2500 series device into eight lines – one for each row of the matrix. In most applications only seven will be used. As shown in Figure 19, interfacing to 54/74 TTL is simpler than with the 4100 series, due to the higher output currents of the 2500 series devices.

TV character displays are popular because of the inexpensive monitors available. Additional logic costs above those required for a simpler X-Y display system must be considered along with other system requirements before a decision is made on the scan technique and monitors to be employed.

CRT Stroked-Character Generation

A CRT character display can be obtained by generating a sequence of vectors or strokes on the CRT to describe a desired character. Instead of using a dot matrix to represent the character, the image is formed from a series of connected lines. Control of these lines comes from information stored in several 4100 series MOS ROMs used together. Consider an 8 position X-Y stroke representation of the character 'A' as shown in Figure 30. The initial point of operation is at the coordinate X = O, Y = O. The first stroke (1) goes to X = 1, Y = 1 with Z = 0; therefore, the CRT beam would move diagonally to the new position with the beam off. The second stroke (2) moves the beam from its last position (X = 1, Y = 1) to the next position X = 1, Y = 5 with the beam on, thus drawing a vertical line on the CRT four units high as the beam moves. The strokes continue to describe the character until completed, with the last stroke returning the beam to the initial position. A block diagram of a display system using this technique is

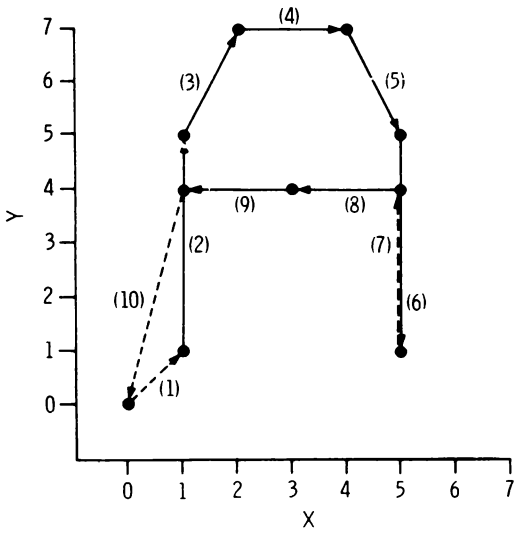


FIGURE 30. Letter "A" in 8 Position, 10 Stroke Matrix

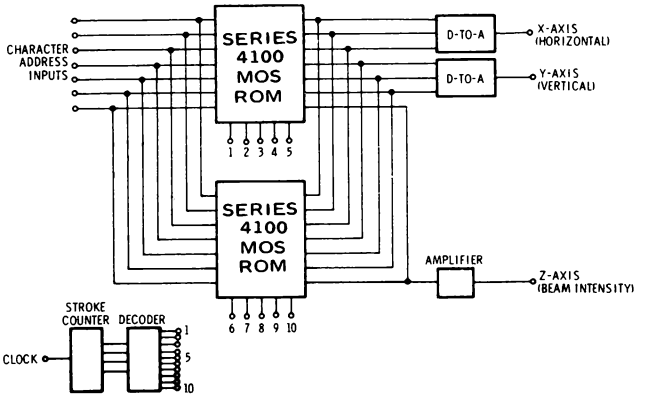


FIGURE 31. Functional Diagram of Circuitry for Projecting One Character on a CRT Using Stroke Generation

shown in Figure 31. Note that of the seven outputs from the 4100 series MOS ROMs, three outputs are used to designate the Y coordinate and one output controls the CRT beam intensity. By using more MOS ROMs, the number of strokes per character can be increased resulting in a displayed character with finer resolution.

A somewhat different approach greatly increases the resolution of the displayed character. Instead of generating the absolute coordinates X and Y at each stroke time, as shown in the system of Figure 31, only the changes in coordinate locations need be generated at each stroke time. The seven outputs from the 4100 series MOS ROMs would be coded to represent the X axis by 3 outputs (sign and 4 lengths), the Y axis by 3 outputs (sign and 4 lengths) and the Z axis by one output (beam blanked or unblanked). The character begins at an initial position on the CRT. During the first stroke time the CRT beam can move in any direction in increments of 0, 1, 2, or 3 units with the beam blanked or unblanked. During the second stroke time the beam can again move in any direction in 0, 1, 2, or 3 unit lengths with the beam *on* or *off*. The initial position of the beam for the second stroke time is the final position of the beam at the end of the first stroke time. Implementation of the above requires some means of holding the D-to-A output voltage at the end of a stroke time, and then summing this voltage with the change in voltage required during the next stroke period. A second method of implementation would be to use two 3-bit registers to store the absolute coordinates of X and Y and two 3-bit adders that would add the change in locations from the MOS ROM outputs to the location held in the registers, arriving at the new location in absolute coordinates. To maintain the CRT line at the same brightness, the beam intensity can be modulated by observing the unit lengths the beam must move during one stroke time and controlling the Z-axis voltage correspondingly. By using more MOS ROMs from the 4100 series, displays having 10, 15, or perhaps 20 strokes per character can be obtained.

OTHER APPLICATIONS

The flexibility of the devices mentioned is sufficient to make them useful in more applications than may be immediately apparent. Their programmability allows them to be combined, producing larger dot matrices even to the extent of using an entire memory for only a portion of a character. Not only characters but look-up tables, code converters, micro-programs for computers and process control, and even random logic can be programmed.

If a 7 X 10 dot matrix is desired instead of a 5 X 7, two 4100 devices can be programmed. Then what is normally a column output becomes a row output, making the 4100 series useful in TV displays. If a column output 7 X 10 display was desired an easy way to achieve it would be to use the TMS 2500 in its 32 X 8 X 10 configuration.

Test Pattern Generator

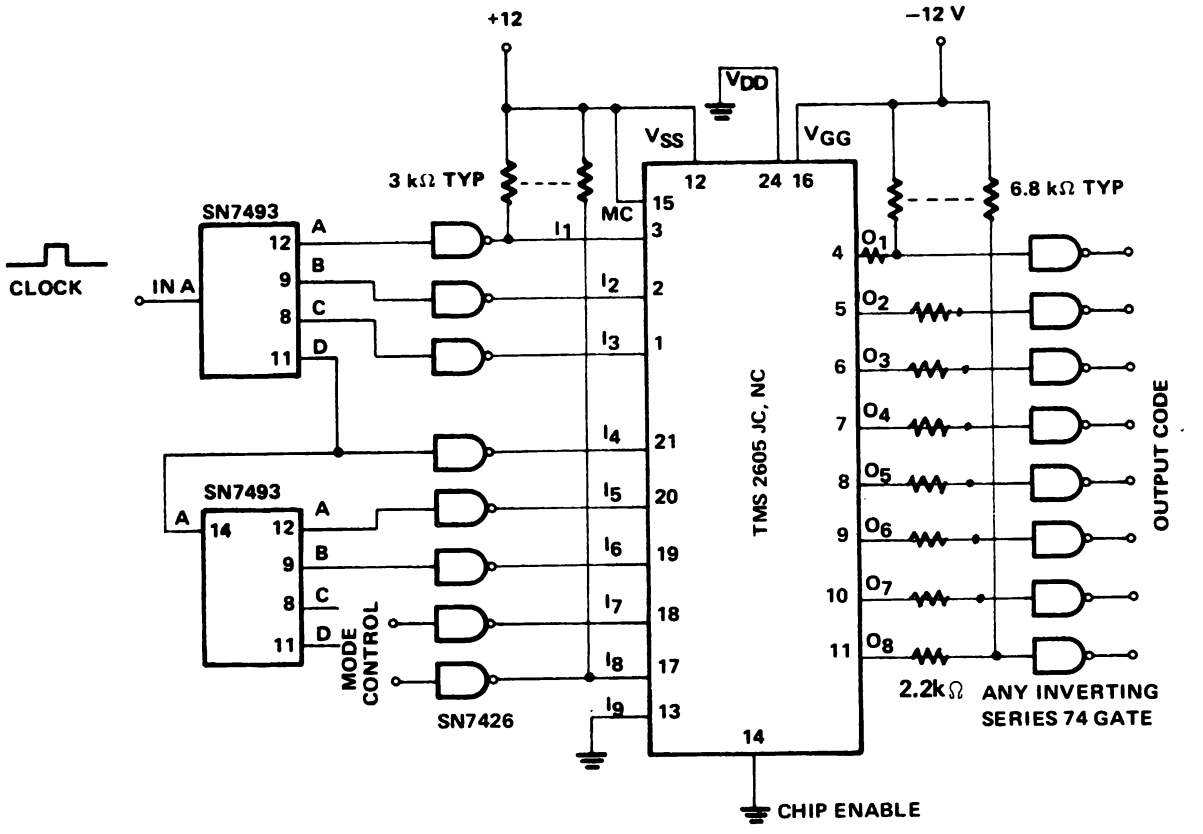
In a terminal it is often necessary to obtain a generator system checkout. The TMS 2605 has been programmed for this function.

TMS 2605 JC GENERATES "QUICK BROWN FOX" MESSAGE IN FOUR CODES

The TMS 2605 JC is a programmed TMS 2600 JC. When a binary count is applied to the input, a standard message is generated on the output (Figure 32). Two inputs are used to select the output code. Four different codes are available USASCII, Baudot, Selectric and EBCDIC.

The message generated is the international sentence – "The quick brown fox jumps over the lazy dog." A message generator like the TMS 2605 JC is extremely useful to test peripheral equipments such as keyboards, displays, printers, etc.

The TMS 2605 JC can be used any time there is a need to fully exercise an alphanumeric equipment by testing out all possible characters in the alphabet. Of course that could be done by generating all code words in binary order, but because there is no logical progression of characters as the count goes up, it would be very difficult to check out the equipment at a glance. The message



NOTE: A binary counter furnishes the inputs for the ROM. The selected code word appears in negative (MOS) logic at the output of the ROM, and is inverted to positive (TTL) logic at the output of the TTL gates.

FIGURE 32. Interface and Typical Applications Data for TMS 2605 JC/NC

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 1234567890 DE

is easier to inspect than the jumble of letters and numerals that would result if a pure binary count was used.

All electrical characteristics are identical to those of the parent device, the TMS 2600 JC. The device features: 2048-bit capacity, static operation, maximum access time under 1 microsecond, open-drain output buffers, TTL compatible, and 24-pin CDIP.

MOS KEYBOARD ENCODER SYSTEMS

The purpose of a keyboard encoder is the generation of a coded word when a key is depressed. While this may, in effect, appear relatively easy, anyone who has worked with keyboard encoders knows that it is complex and fraught with problems. Presently there are basically two types of keyboard encoder technology: 1) bipolar [discrete diodes and an integrated circuit] and 2) MOS.

MOS keyboard encoders provide many advantages compared to bipolar circuits and therefore, are becoming used more and more. MOS provides greater system simplicity. One reason for this is that because of the high level of integration achieved through MOS/LSI, an entire keyboard encoder can be implemented on one single package – direct contrast to the numerous discrete devices and/or integrated circuits used with bipolar techniques. Because it employs fewer components MOS/LSI allows considerable savings in hardware in addition to the simpler, more reliable design.

Furthermore, more cost savings arise from MOS encoders through the savings in related costs, such as printed circuit boards, labor and testing – all again directly related to fewer components. With MOS keyboard encoders, all codes can be changed easily through one mask artwork change. A fixed printed circuit board design can be used. It does not have to be changed when the codes are changed.

Higher degrees of system performance can be achieved. With MOS keyboard encoders, two and N-key rollover are obtained easily. Data-ready terminals, storage flip-flops and other elements can be easily incorporated in the design. In addition, the code words associated to 1 key in the different modes need not be related. To better enable you to understand how theoretical concepts are actually implemented with MOS technology, this discussion will examine the basic elements involved in good keyboard encoder design considerations. It will also describe both a static and dynamic MOS keyboard encoder utilizing many beneficial and unique features possible only because MOS technology is used.

KEY – THE BASIC ELEMENT OF A KEYBOARD

Activation

Generally, a key controls a simple switch which is open when the key is at rest and closed when the key is depressed. A common variation is a reed switch controlled by a magnet mechanically attached to the moving part of the key.

In addition to switches there are other ways to detect the depression of a key. The depression can change the capacitance of a capacitor, the ohmic resistance of a resistor or the inductance of a winding. Hall effect (semiconductor) devices also may be used for the activation of a key.

Number

The number of isolated outputs per key varies. Generally, there is only one output per key. But some coding schemes necessitate two, attained by implementing two switches per key or by using two diodes at the output of the switch.

The number of keys in a keyboard varies depending upon the equipment in which the keyboard is used. MOS techniques are applicable to any number of keys. It is believed, however, that MOS techniques are of special interest for numbers of keys between 32 and 128. This is an area in which the considerable cost savings gained by MOS techniques compared to bipolar techniques are most evident. It must be remembered that the total of 128 keys is not a limit imposed by MOS techniques – it is the practical limit of the size of keyboards.

Key Bounce

When a mechanical switch is closed, the contacts do not come to rest immediately. There is a definite "key bounce." Frequency of this contact bounce and the settling time vary according to the characteristics of the switch itself. The encoder must consider this key bounce phenomenon to avoid spurious encoded outputs. Well-designed keyboard encoders provide ways of adjusting for key bounce.

Data Ready Terminal

For indication that the contacts have settled and that the bounce has ceased, an output terminal should be included in the encoder design. A logical signal on this terminal indicates that the output data is valid.

Mode

Depression of a key may result in more than one output word. In many keyboards, for example, depression of the same key generates an upper-case or a lower-case letter (and the corresponding codes at the output of the keyboard encoder). The number of words generated by the depression of a single key is defined as the number of modes. Shift keys (also called mode select keys) are used to determine which mode corresponds to the depression of a key. Most keyboards employed in computer equipment use two, three, or even four modes. Most keyboards used in calculator equipment, however, use only one mode.

It must be noted that an MOS keyboard encoder places no restriction on code words associated with the different modes on any given key. There may be no relation whatever between these coded outputs because MOS keyboard encoders use read-only memory techniques. It is comparatively easy to implement a multimode keyboard encoder with bipolar techniques as long as the words associated with the different modes for any given key differ by only one or two bits. If such is not the case (which is very common with keyboards used in terminal equipment) the amount of logic needed with bipolar techniques becomes very cumbersome.

Simultaneous Key Depression

It is common for a keyboard operator to depress two or more keys simultaneously. Obviously, this can cause problems with the generation of an output signal. Most keyboards do not include a mechanical key interlock which prevents the depression of more than one key at a time. Therefore, some type of electronic "lockout" or "rollover" must be a necessary part of a keyboard encoder to ensure that only one output – the proper output – is generated despite the fact that two or more keys were depressed simultaneously.

N-Key Lockout

One way of overcoming the problem of output determination when two or more keys are depressed together is known as N-key Lockout. Such a circuit is a part of certain keyboard encoders.

If this is designed as a part of the circuit, when two or more keys are depressed at the same time, within the settling period of the contacts or the sampling period of the keyboard encoder, the keyboard encoder will not generate any data output. When one key is depressed, the keyboard encoder generates the proper output. But when a second key is depressed while the first one is also depressed, the keyboard encoder does not generate any output as long as the first key is not released. When the first key is released, the output corresponding to the second key is generated. Thus, if N keys are depressed simultaneously no output will be generated until all keys are released except one.

N-Key Rollover

Another way of overcoming the problem of simultaneous key depression is N-key rollover. In an N-key rollover system, when a key is depressed the corresponding output is generated. If the first key remains depressed while a second key is depressed, the output corresponding to the second key is generated. When a third key is depressed while the two first keys (or one of them) are still depressed, the output corresponding to the third key is generated. In an extreme case, all of the keyboard keys except one may be depressed. When the last key is depressed, the corresponding output is generated.

N-key rollover, which has been shown increases typing speed considerably, is commonly found on electric typewriters. Because most typists are accustomed to electric typewriters, it is extremely desirable to include these same features on keyboards used for terminals.

Generally, it may be assumed that N-key lockout is sufficient when a visual indication CRT screen, paper printout, and other methods corresponds to the depression of a key. N-key rollover, while desirable in all instances, is absolutely necessary when no visual indications corresponding to the depression of a key are provided.

Fairly difficult and complicated to attain with bipolar techniques, N-key rollover is, however, relatively easy to implement with MOS techniques.

Output Wire ORing

A system may include more than one keyboard. Or if a very large number of keys are desired, it may be necessary to use several encoders for one keyboard. The design of the encoder output circuits must be such that the corresponding outputs of several encoders may be directly tied together and that the resulting output be the logic sum of the connected output. In an MOS keyboard encoder, this can be achieved by using single-ended buffers or special enable logic.

Output Latches

It is often desirable to keep the output word corresponding to a key available on the outputs of the keyboard encoder until the next key is depressed. To accomplish this, latches must be provided in the encoder. The MOS encoders discussed later detail how this is accomplished with MOS techniques.

STATIC KEYBOARD ENCODERS

Static MOS keyboard encoders make use of static ROM techniques. Except for the key bounce circuits and the output latches, an MOS static keyboard encoder essentially consists of a large MOS read-only memory with as many outputs as there are bits in the desired output code.

As shown in Figure 33 a possible implementation would be to assign one key to each read-only memory input. This is not desirable because:

1) The number of input terminals would become much too large (the largest package commonly used in MOS has 40 pins while most keyboards have from 40 to 90 keys). This would force the utilization of several ROMs in a wire-ORed configuration.
2) If an off-the-shelf ROM were to be used, the number of bits would become ludicrous. In a normal ROM the n inputs are decoded in 2^n terms. If a custom ROM were to be used, it would, of course, be possible to forego the decoder and to access directly the read-only memory matrix. This is possible since only one switch could be closed at a time.

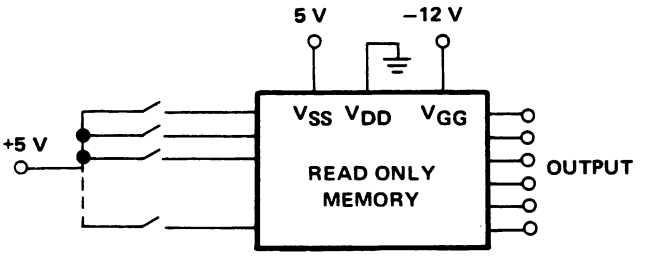


FIGURE 33. Assigning One Key to Each ROM Input is not Desirable

Static keyboard encoders automatically provide N-key lockout. The decoder section of the ROM is programmed to accept only input words which consist of specific patterns of logic "1" and logic "0". No other combinations will be accepted by the decoder, nor result in an output.

N-key rollover may be obtained easily with a static keyboard encoder if the switches are wired to produce a voltage pulse instead of a voltage level upon closure. The width of the voltage pulse must be at least equal to the access time of the ROM.

Static keyboard encoders do not necessitate clock. They are simple to use and N-key rollover is easily obtained. Their only drawback is that two diodes per key are necessary when one-contact switches are used. However, computer-type diodes are inexpensive and can often be mounted in the reed-switch housing, taking the place of the wire going to the upper part of the reed, as shown in Figure 34.

DYNAMIC KEYBOARD ENCODER

Scanning techniques are commonly employed when bipolar logic elements are used to implement keyboard encoders. The same techniques are applicable to MOS keyboard encoders.

Basically, a dynamic keyboard encoder consists of these five elements:

1) A binary counter.
2) A decoder driven by the most significant bits of the counter (slow count).
3) A multiplexer driven by the least significant bits of the counter (fast count).
4) A one shot fed by the output of the multiplexer.
5) A ROM for mode select and code conversion.

The key switches are used as cross points in a matrix, the lines of which are the outputs of the decoder, and the columns of which are the inputs to the multiplexer. All of the columns of the matrix are scanned for each step of the decoder. Such a system is shown in Figure 35.

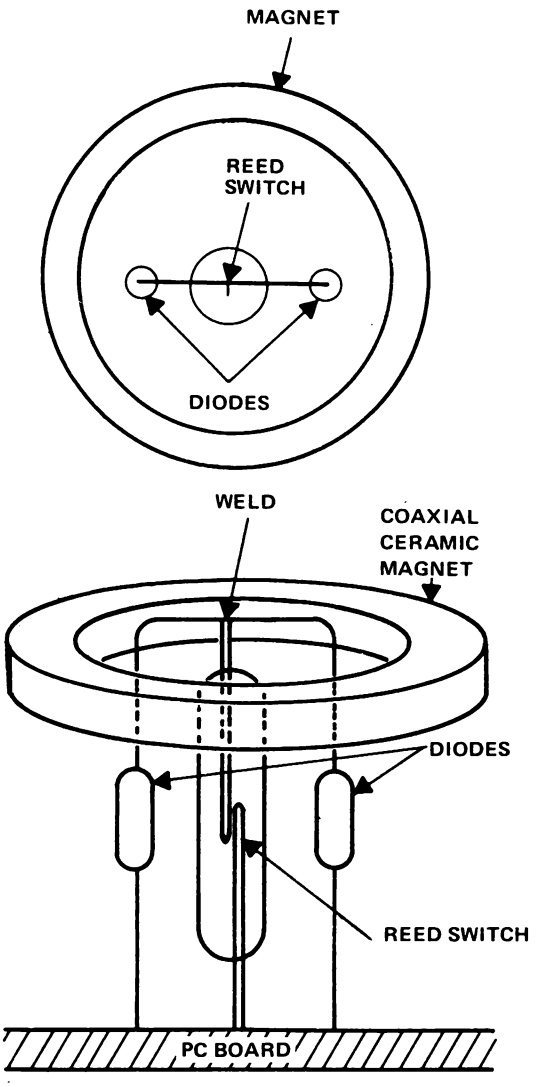


FIGURE 34. Method of Mounting Diodes in the Reed-Switch Housing When One-Contact Switches Are Used

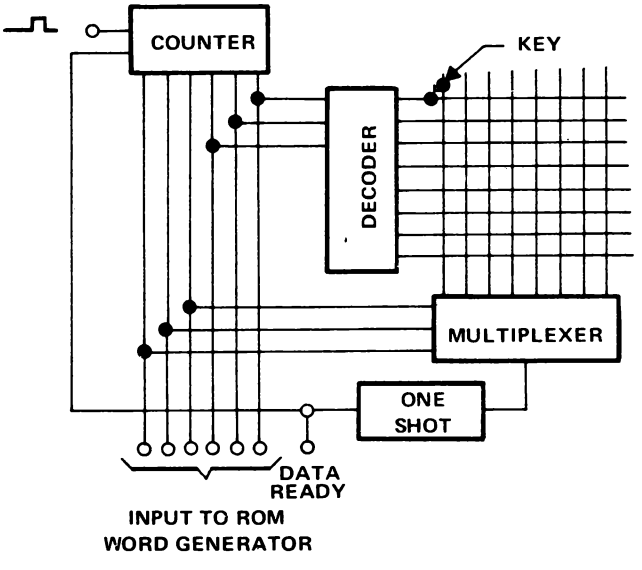


FIGURE 35. Block Diagram of a Typical Dynamic Keyboard Encoder

A key closure results in logic 1 at the output of the multiplexer and the output is used to stop the counter. The output of the counter, when stopped, is the ROM input address. A 1 on the output of the one-shot signifies that the data is valid (data ready).

The MOS scanning keyboard encoders used in such systems offer many advantages compared to their bipolar counterparts:

1) The high level of integration allows the designer to implement the entire circuit in one package instead of several packages.
2) The ROM section of the MOS keyboard encoder can be expanded to store several unrelated modes/key.
3) Codes can be modified by a single-level artwork change on the MOS device instead of a printed circuit board change.
4) A clock generator can be incorporated on the chip easily.
5) Two-key rollover is inherent to the scanning approach. N-key rollover may be obtained simply through shift-register techniques in the MOS scanning approach, and this circuitry can be incorporated on the chip.

TYPICAL MOS KEYBOARD ENCODER

To better understand the concepts and benefits of MOS keyboard encoders, two encoders utilizing this technology will be detailed.

TMS 5000 JC/NC 90 Key, Four Mode MOS Dynamic Keyboard Encoder (Under Development)

This encoder has been designed for keyboard of up to 90 keys. Scanning techniques are used in connection with read-only memory techniques. It has four modes. The output word has 10 bits which are stored on MOS flip-flops. The output remains valid as long as no other key is depressed. It also features N-key rollover, N-key lockout, 10 parallel outputs per character, any key down output, data-ready output, latched outputs, key bounce adjustment through delay node input, operational clock range from 10 kHz to 50 kHz and TTL compatibility on control inputs and data outputs.

Operation

The system is illustrated in block diagram form in Figure 36. The sequence of events is as follows:

During ϕ_1 time, a particular row and column are selected. Also during ϕ_1 time every row and column line of the array is charged to a negative voltage.

During the following ϕ_2 time, the row and column driving devices are turned off except for very high impedance devices associated with the column lines. (These high impedance devices are used to compensate for slight external leakages of the printed circuit boards.) The selected row is switched to V_{SS} and the selected column input logic is enabled. A key depression is detected if the column line voltage has changed significantly from its precharged negative voltage to a level close to V_{SS}. The

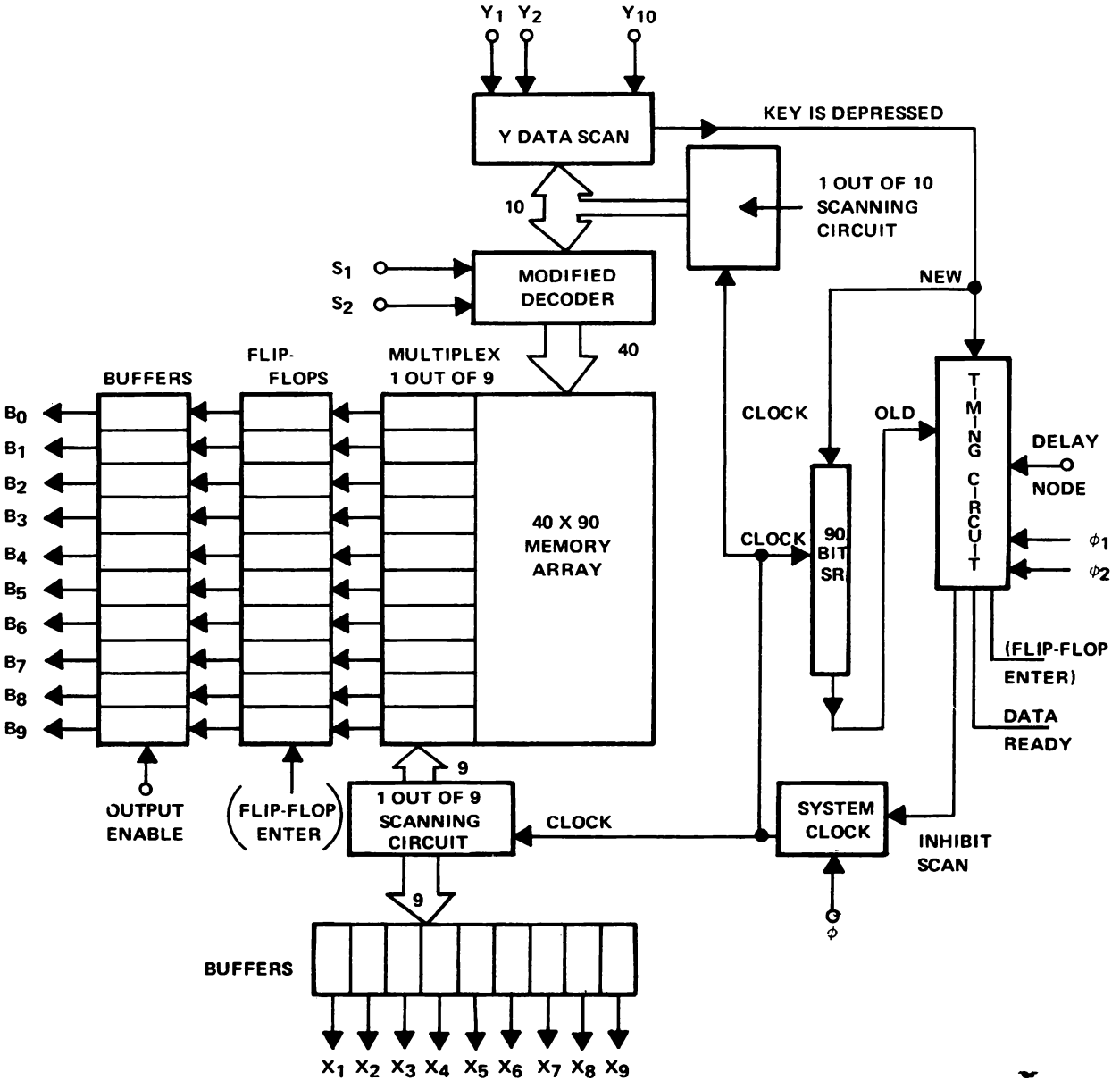


FIGURE 36. Block Diagram of a 90-Key, Four-Mode MOS Dynamic Keyboard Encoder

information is made available at the input to a 9-bit shift register.

At this particular moment, the continuing sequence of events is dependent on whether N-key lockout or N-key rollover is desired.

N-Key Lockout

If N-key lockout is desired, a key depression will set an RS flip-flop which controls the counter and shift register clocks. All counting and shifting ceases.

During the subsequent ϕ_1 time data is loaded from the ROM into the output flip-flops. At ϕ_2 a Data Ready signal is generated. This signal will either persist as a level output or it can be made to last only for a one clock period. The actual time will depend upon which option is chosen by the customer and is designed into the custom gate mask used in processing wafers.

At this point in sequence, an external delay node comes into play. This node causes a delay from a minimum of 2 clock periods to a maximum of 10 milliseconds depending upon the external capacitance involved. After the delay has occurred, the clock control flip-flop is allowed to reset pending the release of the key. The counter clocks remain static until the ϕ_1 after the key is released.

Once reset has occurred, the array is precharged again and the timing logic initialized for a new cycle.

An array suitable for N-key lockout is illustrated in Figure 37. Note that this type of array is not suitable for N-key rollover. In the system as shown, assume keys (a), (c), and (i) are depressed. When the system scans through the array it will eventually come to location C1, R3. Instead of key (g) being "up," a current path exists through switches (a), (c) and (i) and the system senses (g) being depressed. This problem is solved by including a series diode with each key switch.

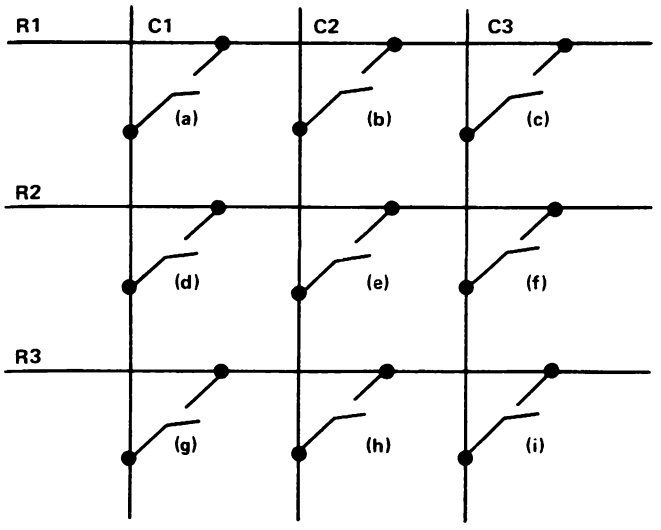


FIGURE 37. Array Suitable for N-Key Lockout

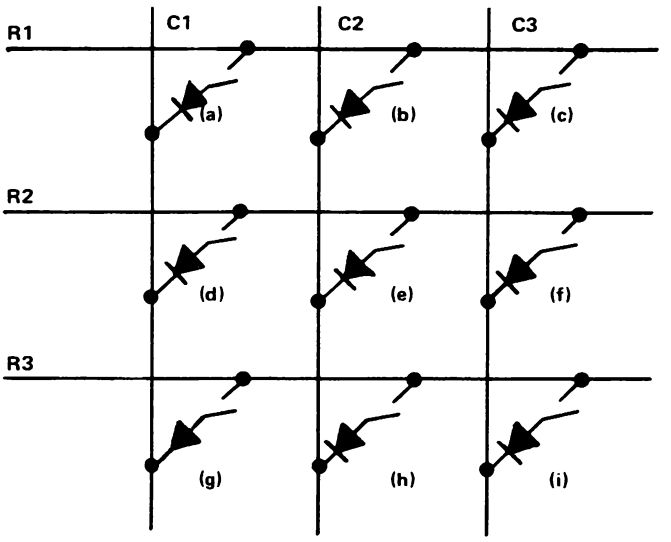


FIGURE 38. Array Suitable for N-Key Rollover

N-Key Rollover

If N-key rollover is desired, a key depression will set an RS flip-flop which controls the counter and shift register clocks *only* if the output of the 90-bit shift register indicates that no depression of that particular key has occurred during the previous scan. If the flip-flop is set, all counting and shifting ceases.

During the subsequent ϕ_1 time, data is loaded from the ROM into the output flip-flops. The Data Ready signal is generated in a manner similar to that described in the previous discussion of N-key lockout.

Again the external delay node is used. After the desired delay has occurred, the clock control flip-flop is reset and system scanning is resumed. *Note that the key did not have to be released.* The key will be ignored on all future scans until it is released and then depressed again.

An array suitable for N-key rollover is illustrated in Figure 38

Memory Array

The memory array utilized in this system is a static read-only memory array of 3600 bits organized as a 40 X 90 pattern. This particular memory array is programmed by a single level mask change.

The 90 outputs from the ROM are fed into a multiplexer controlled by the R decoder outputs. The 10 outputs of the multiplexer are fed to the storage flip-flops upon command from the timing circuits.

Memory Driver and Mode Select

The memory drive and mode select circuit is shown in Figure 39. The memory driver is a modified ROM

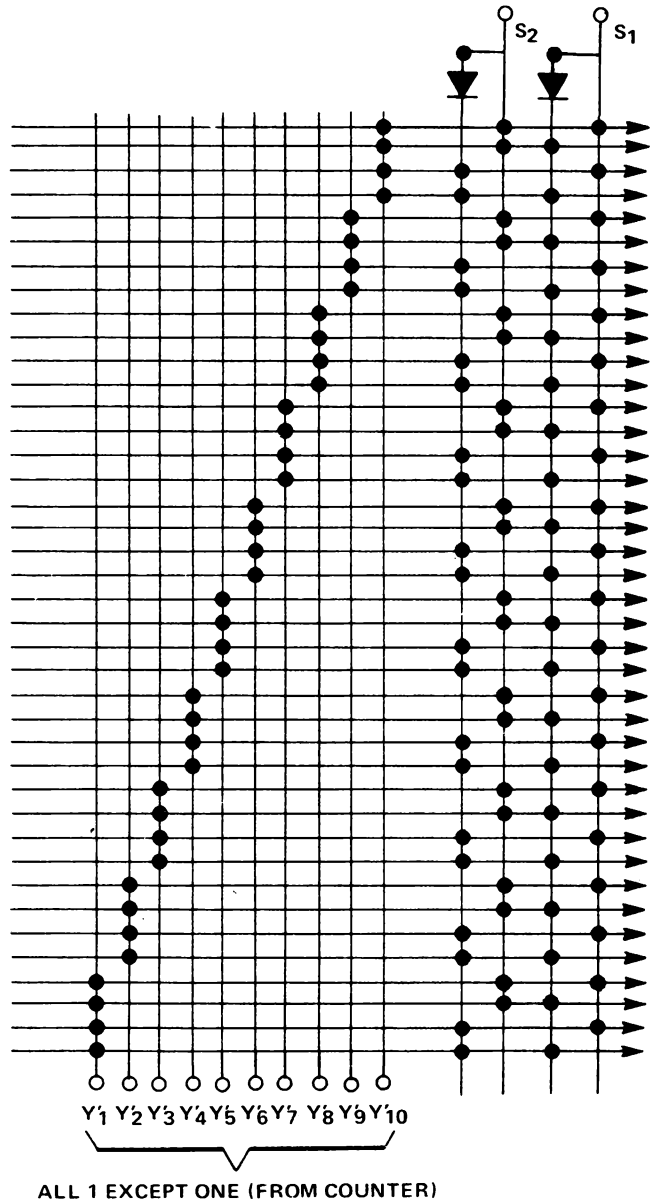


FIGURE 39. Memory Drive and Mode Select Circuit of 90-Key MOS Dynamic Keyboard Encoder

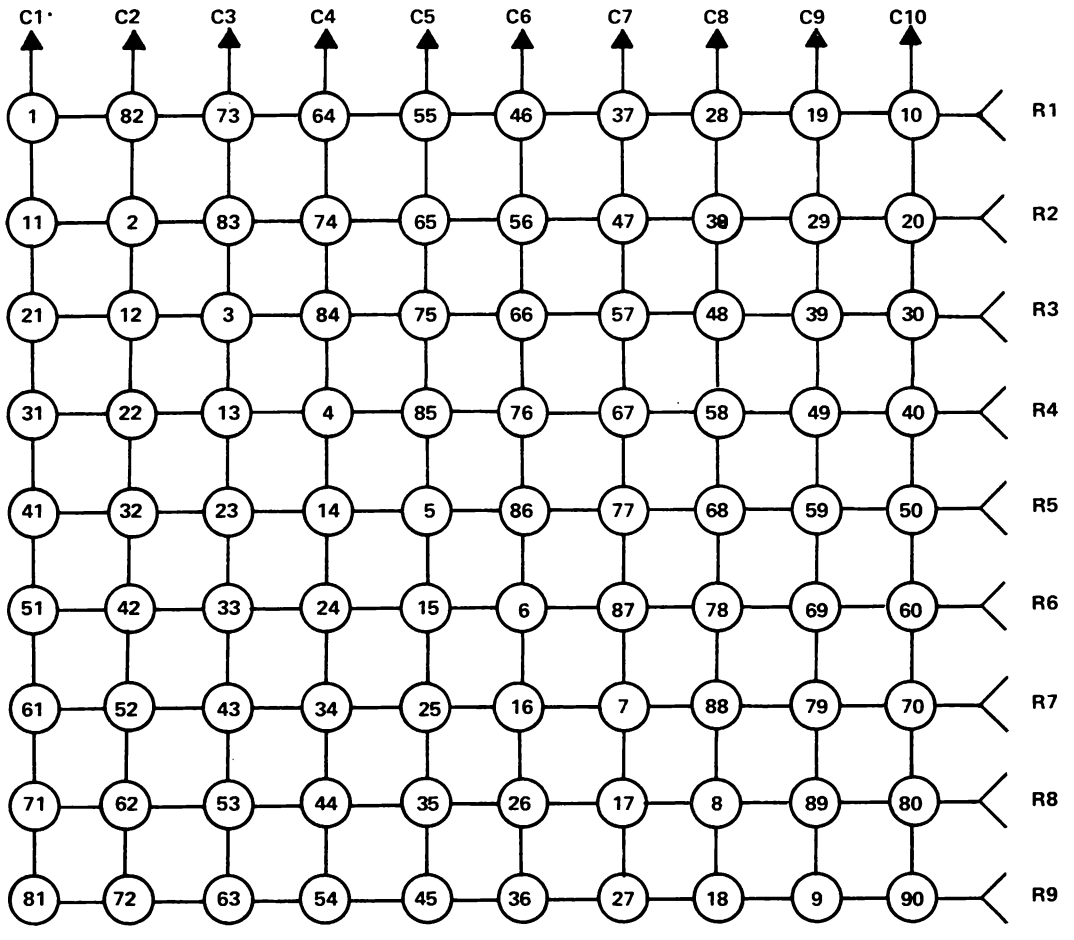


FIGURE 40. 9 X 10 Key Matrix

decode. Inputs are the 10 C inputs from the C counter, the S1 and S2 inputs in true and complement form. This need not be an exhaustive decoder because the Y inputs are already decoded and only one C input at a time can be at a logic 1. The S1 and S2 mode select inputs are decoded and used in conjunction with the C inputs to create 40 product terms, which are fed to metal lines running over the ROM. One, and only one, of the metal lines will be at logic 1 at any given time.

Switch Matrix – Inputs and Outputs

The switch for this system is shown in Figure 40. The keys are arrayed on a 9 X 10 key matrix. The device has been designed mainly for use with reed switches; but many other types of switches can be used. The bounce is non-critical and there are provisions for adjusting the key bounce delay (switching circuit). The matrix is fed by R1 and R9 device outputs on one side and feeds the C1 through C10 device inputs on the other.

Inputs S1, S2, Lockout/Rollover Control, Output Enable, and ϕ can be compatible with TTL. Each input going to an MOS transistor will be protected from static damage by proper internal protection, shown in Figure 41. Inputs C1 through C10 are to be used with reed switches. A switch closure is defined as a voltage greater than +3.5 volts. An open switch is defined as a voltage less than 0.0 volts.

Outputs R1 through R9 are to be used with reed switches. As shown in Figure 42 they are capable of supplying enough current so that when 10 switches associated with the same output are closed, the output voltage will be greater than +3.5 volts. If not selected, these outputs will be an impedance of greater than 1MΩ returned to the V_{SS} supply. Every output is protected from static charge build-up. During ϕ_1 time all outputs (R) and all inputs (C) connected to the key array are precharged to a voltage within a few volts of the V_{GG} supply. This precharging initializes the array so that a key depression can be detected during ϕ_2 time.

Mode Select

The device contains four modes which are selectable by two mode-select lines, S1 and S2 shown in Figure 39. There are 10 code bits per mode per key These bits are programmable by a single-level mask change. Outputs are B0, B1, B2, B3, B4, B5, B6, B7, B8, and B9.

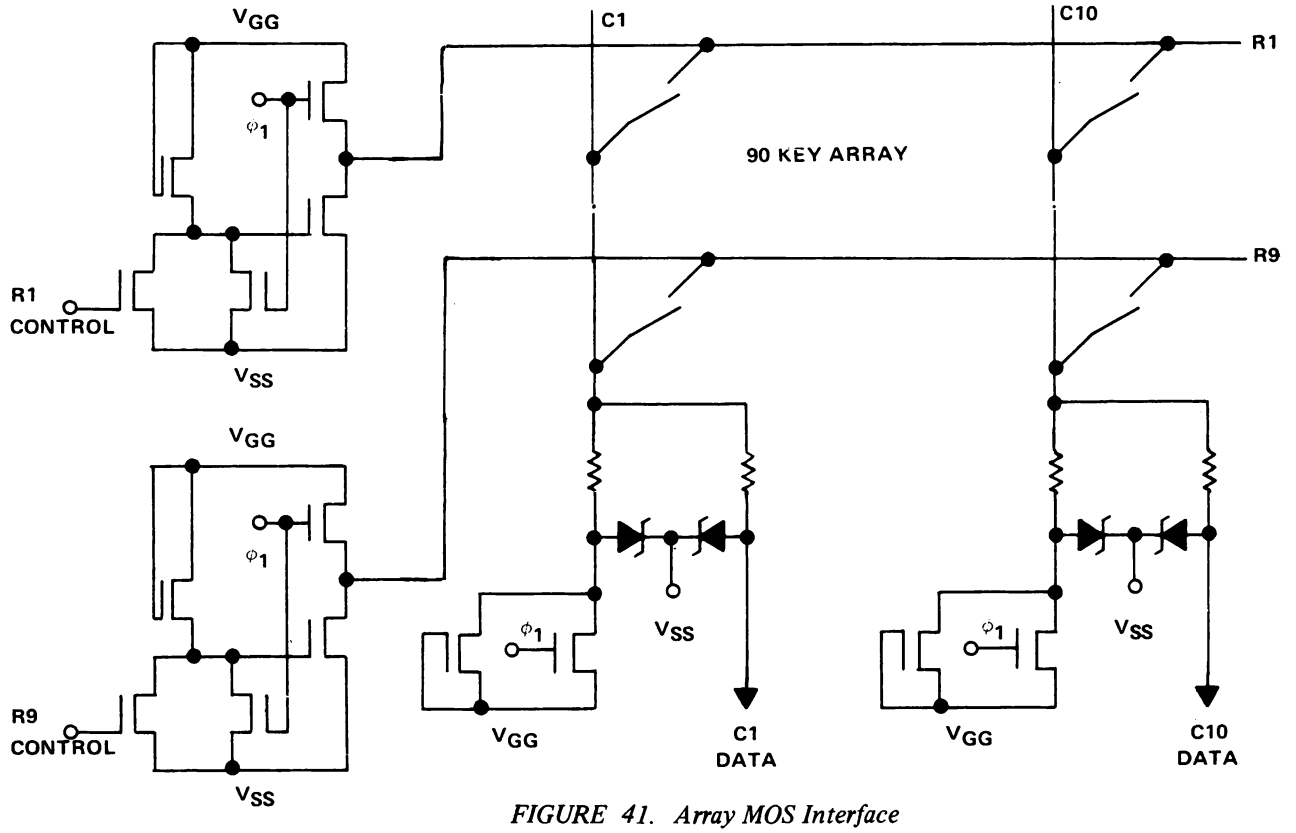


FIGURE 41. Array MOS Interface

Output Storage

The outputs are equipped with flip-flops. Data corresponding to the depression of a key remains on the output when the key is released until the next key is depressed. The flip-flops are clocked internally.

Output Enable

The device contains an "output enable" input. When the device is disabled, all outputs are floating. This permits wire-ORed multiplexing of keyboards.

Data Ready Signal

The device contains a "data ready" output which is programmable by a simple mask change as a pulse or level signal. It is generated each time new information is available on the data outputs. When programmed for a pulse, the pulse width will be one clock time.

Critical Timing

The data ready signal will occur a minimum of 300 nanoseconds after all output data has stabilized to within 0.2 volts dc of its final values. The minimum time between data-ready signals is effectively the externally controlled (IS) delay pluse three clock cycles. This is used to adjust the key bounce settling time.

Any Key Output

A new output is provided which becomes a logic 1 whenever a key is depressed. This output remains a logic 1 until a complete keyboard scan occurs in which no key depressions are sensed. This output has a number of uses. It is the inverse of the signal commonly known as Data Key Idle. One particular application is to use Any Key in conjunction with Data Ready to control a "repeat-character" function externally.

Extra Output B9

An extra output has been added which is primarily intended for system control. Sometimes a mode associated with a particular key is not a valid condition on the keyboard. This additional output could be connected externally to inhibit the system from receiving the Data Ready signal generated by the particular key in question.

Hysteresis

A unique circuit is incorporated in the column line inputs and the timing delay node which creates a minimum 0.5 volts hysteresis. Once an input has achieved the proper threshold to be sensed as a depressed key, the threshold will shift 0.5 volts. To be sensed as a released key, the input must be changed by more than 0.5 volts.

Lockout/Rollover Control

An input is provided which allows the device to be used as an N-key rollover encoder when the input is at V_{DD}. The device can be used as an N-key lockout encoder when the input is at V_{SS}.

Output Buffers

Two different output techniques can be employed with this circuit. One method, shown in Figure 43

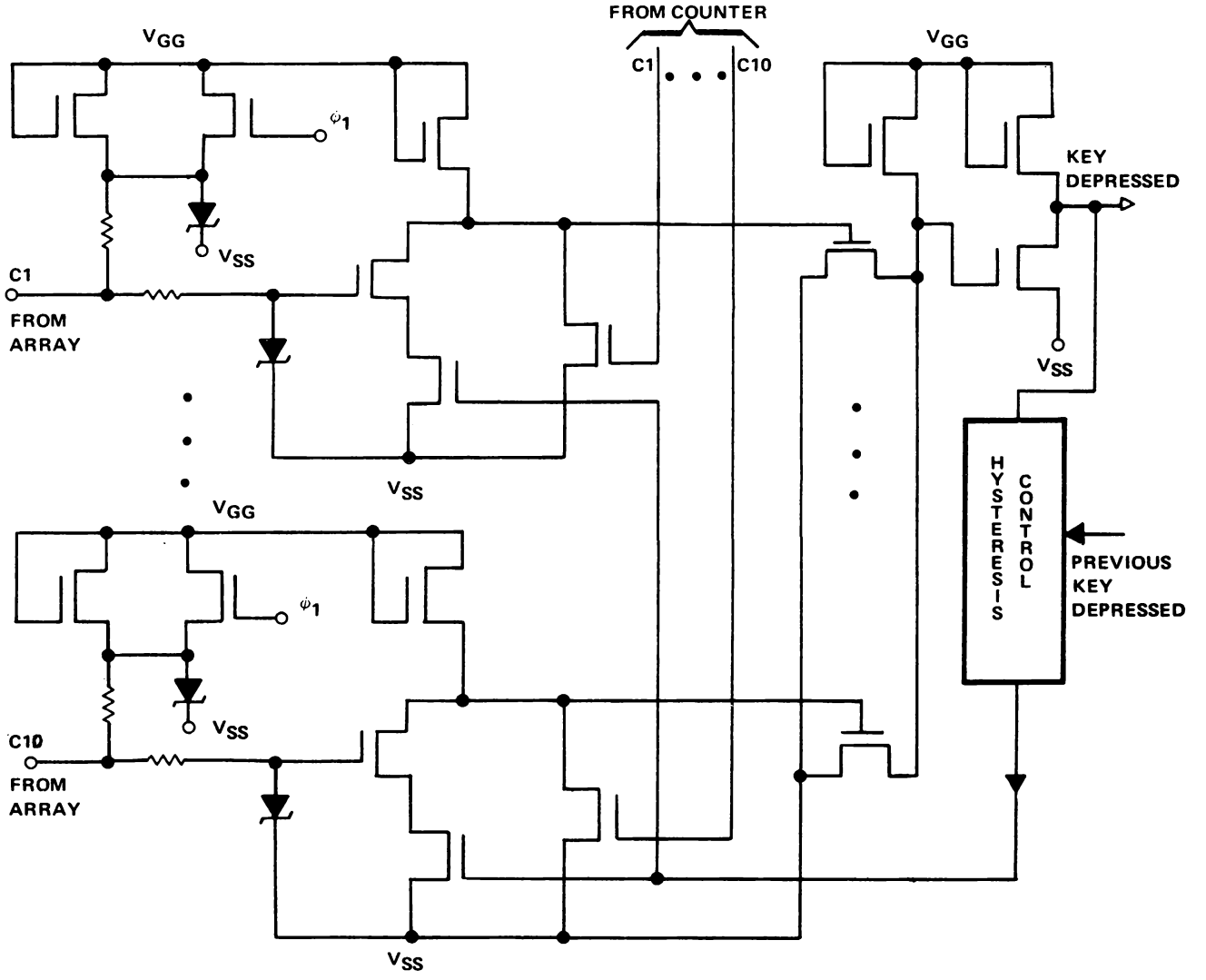


FIGURE 42. Column Data Scan

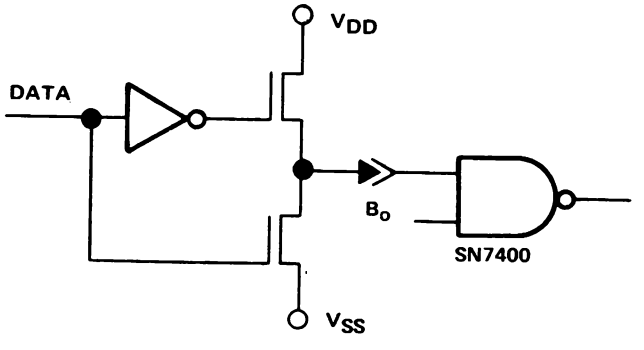


FIGURE 43. Push-Pull Any Key and Data Ready Outputs

uses the B80 through B9, Any Key, and Data Ready outputs in a push-pull configuration. Their drive capability will depend on the V_{DD} supply. For example: if V_{DD} = 0 volts and V_{SS} = +5 volts ±5%, then the outputs will be capable of driving two SN74L00 TTL inputs. If V_{DD} = −5 volts ±5% and V_{SS} = +5 volts ±5%, the outputs will be capable of driving one SN7400.

A different output method may be employed as shown in Figure 44 if it is desired to drive TTL gates with no −5 volt supply. This can be achieved by making V_{DD} = 0 volts and using an external 6.8 kΩ resistor on each output.

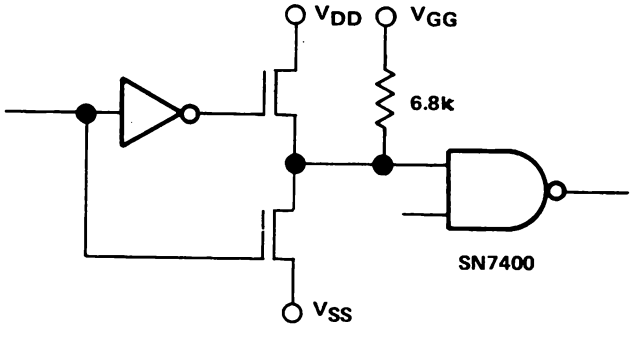


FIGURE 44. Circuit for Driving TTL Gate With No Minus 5 Volt Supply

TTL to MOS and MOS to TTL Interface circuits (CA 170)

TTL TO MOS AND MOS TO TTL INTERFACE CIRCUITS

by Dale Pippenger

Many types of high performance MOS memories presently available have drive requirements and output levels not directly compatible with TTL circuits. Typical MOS circuits requiring special drive and sense circuits necessary to interface with TTL circuit levels are MOS shift registers used as circulating memories, MOS random access memories and MOS calculator chips.

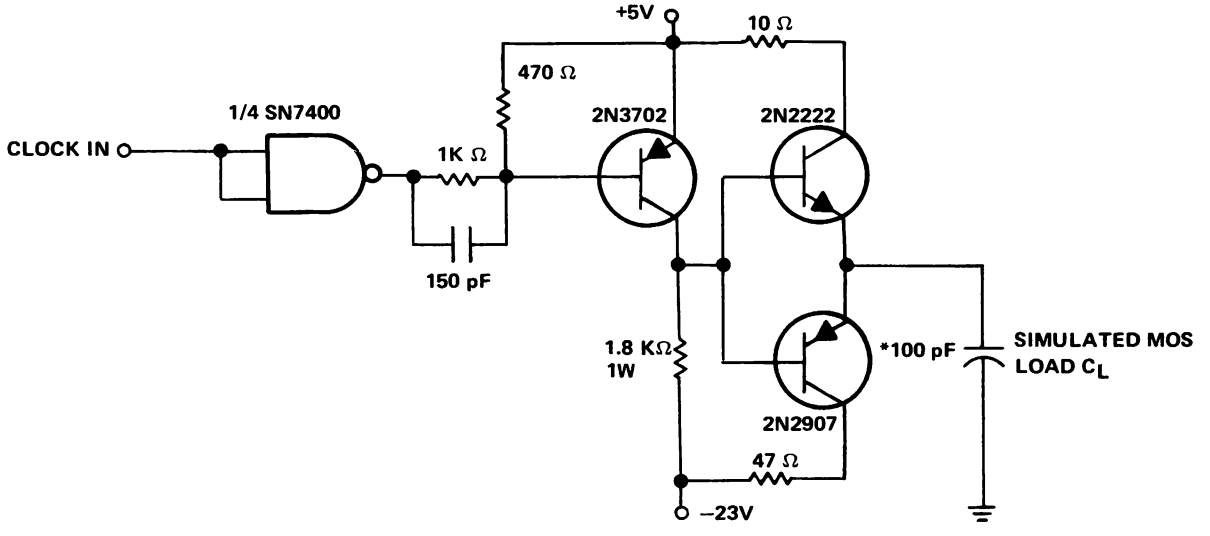
Interfacing between MOS and TTL circuits may be accomplished with any one of a variety of discrete device or integrated circuit level shifters. Often it's desirable to use a device that is readily available to perform the interfacing function. Many times device types being used elsewhere in the system are available and can perform the task adequately. Choice of the exact type of interface circuit necessary will depend on the system performance desired and the input-output requirements of the system.

Since there can be great variation in system requirements, characteristics and devices available, this report describes applications of a wide variety of devices. Included in this report are MOS/TTL interface circuits using bipolar transistors, JFETs, MOSFETs and special integrated circuits known as interface circuits.

TTL TO MOS INTERFACE

MOS input circuits look capacitive. Clock inputs are generally more capacitive than data inputs and may have as much as 60 pF input capacitance. Drivers must be capable of operating into such loads and, in some cases, of driving several clock inputs in parallel.

For maximum switching speeds (T_R and T_F), it's desirable to have both an active pull-up and an active pull-down output for the MOS driver. The drivers shown in the circuits in Figures 1, 2, 3, 4, 5, and 6 have active pull-up and pull-down outputs allowing large capacitive MOS loads to be driven.



*C_L MAY BE CHANGED TO SIMULATE DIFFERENT MOS LOADS.

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FIGURE 1. TTL to MOS Clock Driver Using Discrete Devices. Provides an Active Pull-Up and an Active Pull-Down Output.

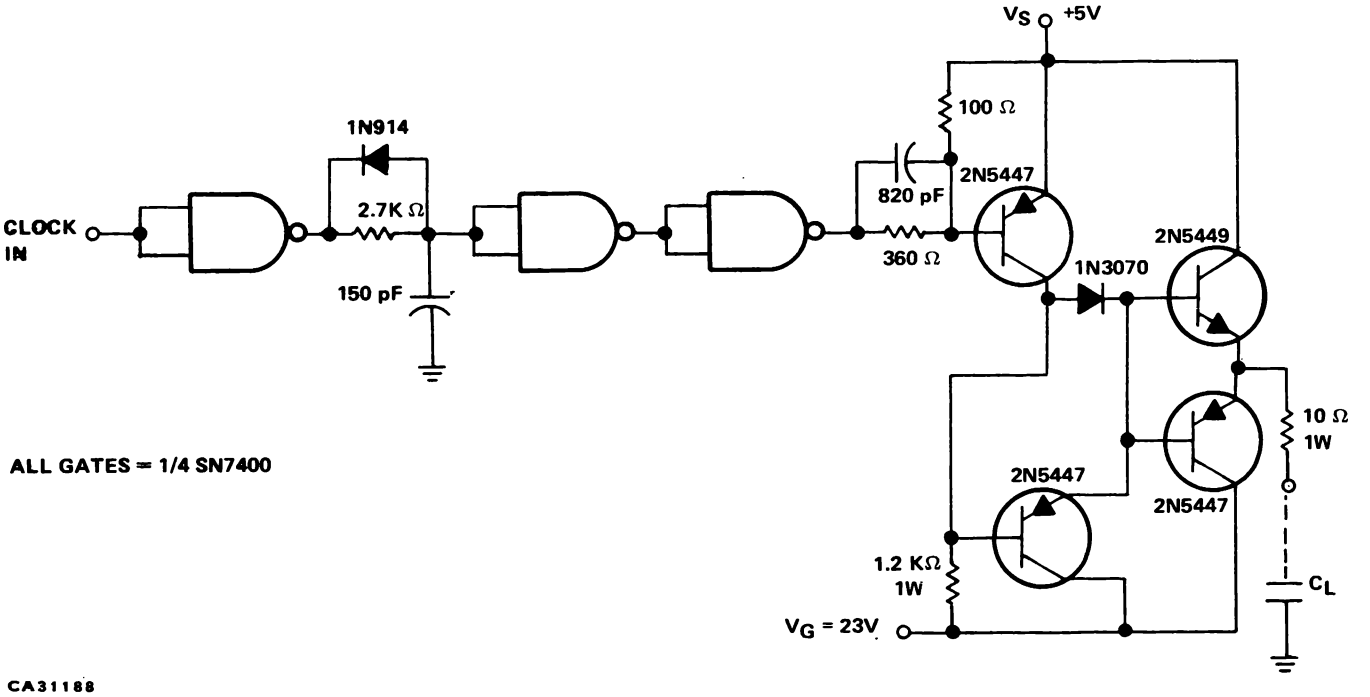

FIGURE 2. TTL to MOS Clock Driver Using Discrete Devices. Provides an Active Pull-Up and an Active Pull-Down Output.

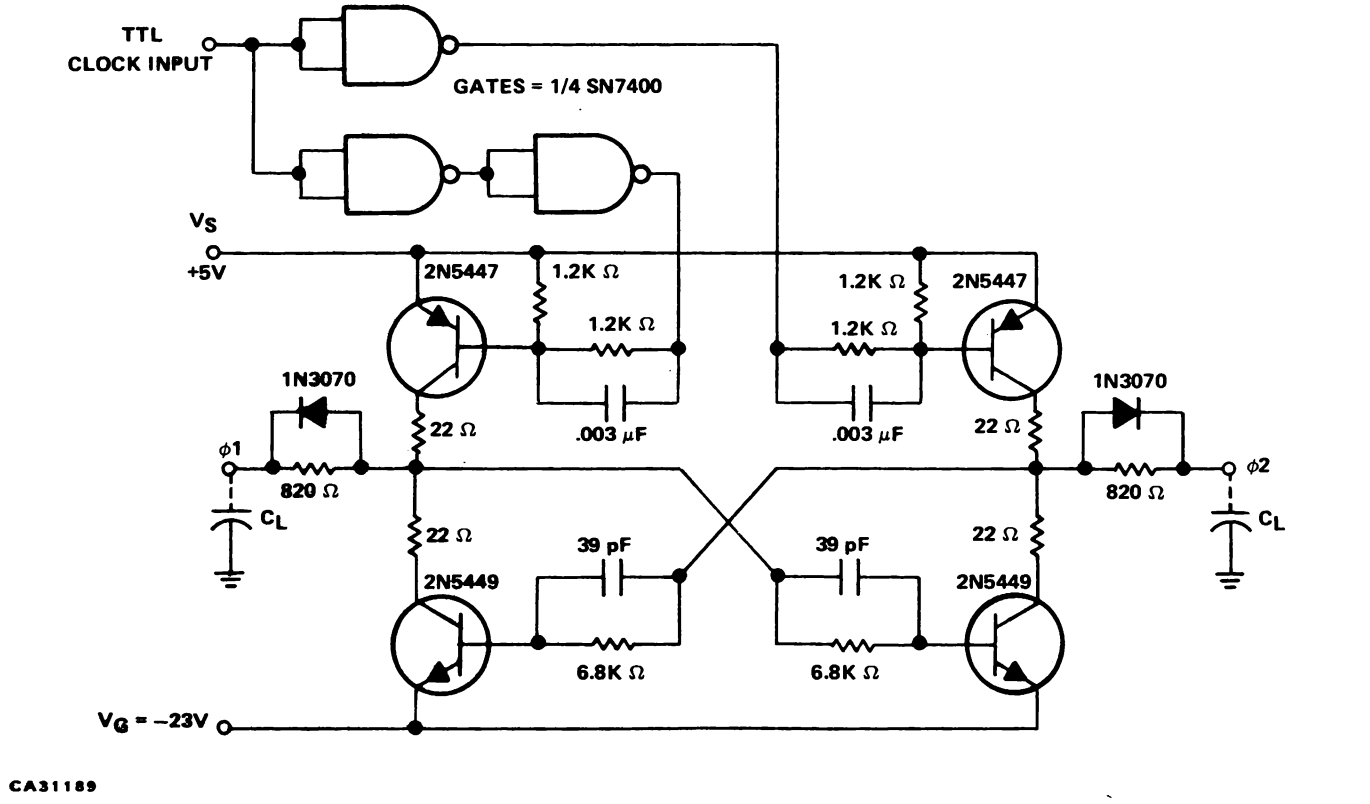

FIGURE 3. TTL to MOS Clock Driver Using Discrete Devices. Provides an Active Pull-Up and an Active Pull-Down Output.

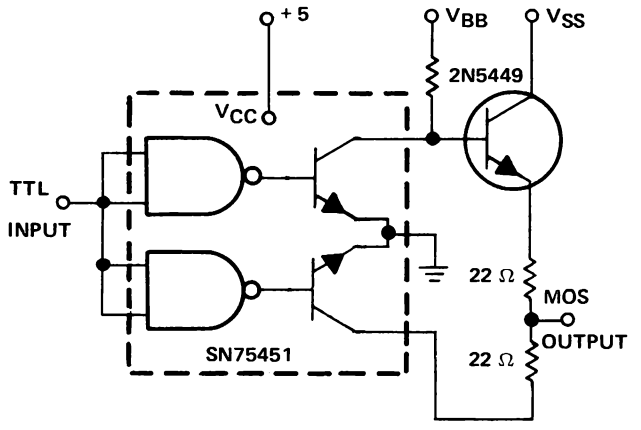

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FIGURE 4. TTL to MOS Clock Driver Using Discrete Devices. Provides an Active Pull-Up and an Active Pull-Down Output.

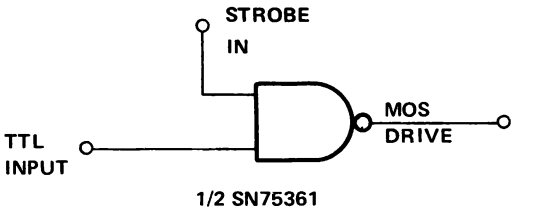

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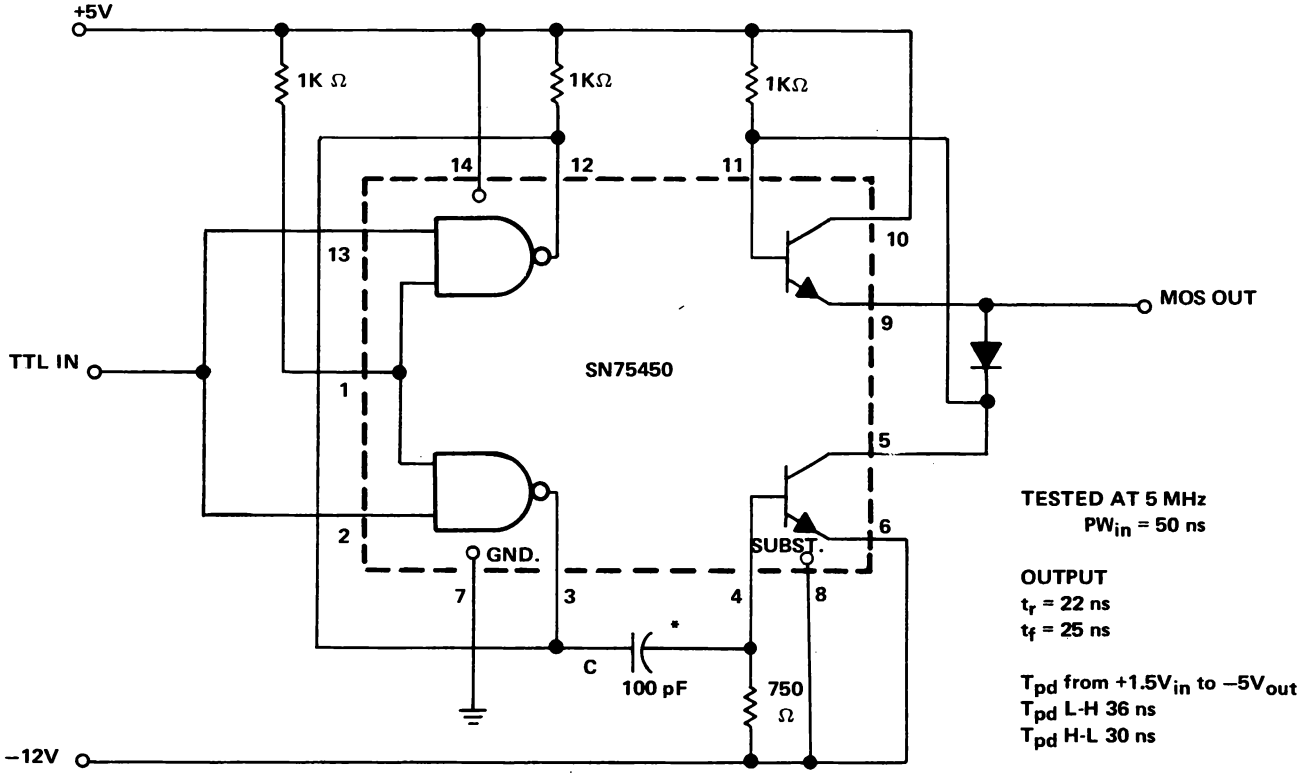
FIGURE 5. TTL to MOS Clock Driver Using Discrete Devices. Provides an Active Pull-Up and an Active Pull-Down Output.

Figure 7 shows a very basic and inexpensive interface using an active pull-down only. This circuit is satisfactory for a low-speed system, or where the MOS load capacitance is low.

Table 1 provides comparative performance data for various discrete devices and power supplies that can be used in the circuits in Figures 1, 2, 3, 4, 5, 6, and 7. Note the output fall time and maximum frequency versus load "C" of circuit 7.

The discrete circuits in Figures 1, 2, and 3 are typical of combinations of bipolar circuits that have been designed for driving relatively high speed systems. These circuits, plus the circuit shown in Figure 6, interface to MOS voltage levels that are negative. The circuits illustrated in Figures 4 and 5 have positive output levels for use in MOS systems in which, for example, V_{SS} is +16 volts.

As can be judged from the performance data shown in Table 1, these circuits are adequate for highly capacitive clock inputs as well as data inputs. The data in Table 1



*** VALUE OF COUPLING CAPACITOR MAY NEED TO BE ADJUSTED FOR FREQUENCY OF OPERATION.**

CA31192

FIGURE 6. TTL to MOS Clock Driver Using Discrete Devices. Provides an Active Pull-Up and an Active Pull-Down Output.

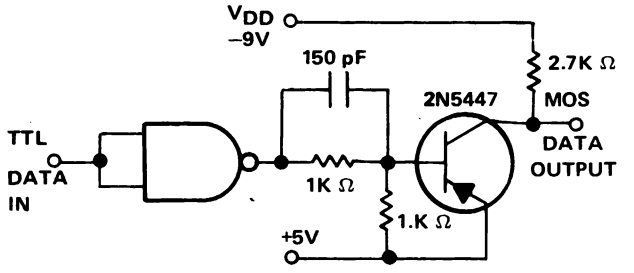


FIGURE 7. TTL to MOS Data Driver Using Discrete Device. Provides Active Pull-Down Output Only.

shows the switching speed and frequency limitations of each TTL to MOS circuit. Comparing the information provided in the Table with desired specifications and comparing component counts should help deciding which interface is best to use.

The SN75361 dual driver, is a very economical driver with high speed capability. It is compatible with many of the new MOS memory systems. Due to it's drive capability and output surge protection it can also be used as a universal peripheral driver for lamps, relays and so forth.

MOS TO TTL INTERFACE

The main requirement for MOS to TTL interfacing is that of level shifting as output requirements are not so severe.

A bipolar transistor can be used to provide a MOS to TTL level shift. If used in conjunction with a gate, an enable terminal is available for timing purposes. This circuit is shown in Figure 8. Comparative performance data for the circuit is shown in Table 2.

A similar type of interface circuit can be constructed using one-half of a SN75450 peripheral driver. A circuit using the SN75450 is shown in Figure 9. This circuit has the advantage of combining the gate and transistor in an integrated circuit. With two channels available per package, component costs and assembly costs are reduced significantly.

The high input impedance of FET amplifiers make them useful as MOS to TTL level shifters. Figures 10 and 11 show a MOSFET and a JFET, respectively, used in interface circuitry. Although these circuits are somewhat limited in frequency, they are simple and easy to use.

Many random access memories available have low level output signals of 50 to 400 mV. The TMS4003 and

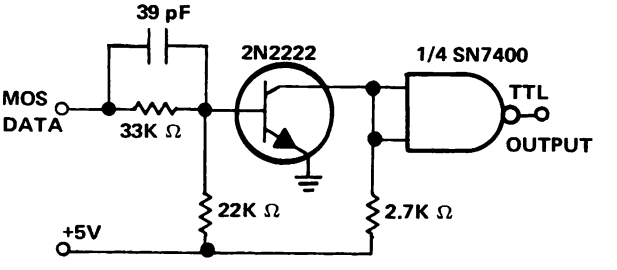


FIGURE 8. MOS to TTL Level Shift Circuit Using a 2N2222 Bipolar Transistor

Table 1. Comparative Performance Data for the TTL to MOS Circuits Shown in Figures 1, 2, 3, 4, 5, 6 and 7

Circuits	1 2N2222/2N2907				2 1φ–2N5447/5449				3 2φ–2N5447/5449				4 SN75451				5 SN75361				6 SN75450				7 2N5447			
Load "C" (pF)	50	100	700	2K	50	100	700	2K	50	100	700	2K	50	100	700	2K	50	100	700	2K	50	100	700	2K	50	100	700	2K
Output T_R (ns)	6.0	8.0	22	58	11	15	26	54	352	355	360	370	29	30	55	114	9.5	11	26	53	75	75	150	330	8.3	12	47	135
Output T_F (ns)	104	120	143	268	38	40	50	70	121	223	400	3900	8.2	11	37	79	7	10	25	66	22	26	200	330	403	630	4000	11K
T_{PD} L-H (ns)	11.4	12.4	20	41	42	43	51	69	80	81	99	140	29	31	47	79	15	16.5	26	51	25	25	30	50	12	14	29	66
T_{PD} H-L (ns)	87	113	153	290	122	125	131	150	72	100	460	1180	21	23	33	50	7.0	8.6	19	40	30	30	50	200	211	384	1500	3800
Max. Freq. (MHz)	4.5	4.1	1.7	1.0	4.1	4.0	4.0	zot	1.2	0.71	0.33	0.14	9.1	9.0	5.0	2.3	12.5	12	6.2	1.2	8.0	8.0	1.2	0.71	1.5	1.2	0.19	0.04
Storage Time (ns)	53	63	103	212	117	119	121	121	42	50	130	260	20	21	24	31	6.6	6.7	9.6		20	20	33	40	107	201	430	1200
+Supply-V (V)	5				5				5				5 19 16				5 16				5				5			
+Supply-I (mA)	28				43				36.9				28 10 38				11 9.3				30				1.67			
−Supply-V (V)	23				23				23				–				–				23				−9			
−Supply-I (mA)	13.5				22				21.1				–				–				21				3.2			
V_{OL} No Load	−21 V				−21 V				−23 V				+0.1 V				+0.1 V				−21				−9 V			
V_{OL} I_L = 3 mA	−20 V				−20 V				−20 V				+0.1 V				+0.1 V				−20				−.9 V			
V_{OH} No Load	+4.9 V				+4.1 V				+4.9 V				+15.9 V				15.5 V				+4.6				+4.9 V			
V_{OH} I_L = 3 mA	+4.1 V				+3.9 V				+4.2 V				+15.9 V				14.5 V				+4.0				+4.9 V			

Table 2. Comparative Performance Data for the MOS to TTL Circuits Shown in Figures 8, 9, 10, 11, 12, 13 and 14

Circuits	8 2N2222	10 3N160	9 SN75450	12 SN75107	13 SN75207	11 2N3819	14 SN75270
T_{PD} L-H (ns)	10.3	10.3	11.6	12.2	10.6	11.2	11.2
T_{PD} H-L (ns)	31.2	7.8	51.6	11.2	10.2	8.9	13.7
Max. Freq. (MHz)	12.2	0.91	8.3	12.5	12.5	1.0	14.0
V_{IN} for "O" Volts Over Ref. V	−5.17	−4.23	−5.16	+7 mV*	+2 mV*	0	−6.1
V_{IN} for "1" Volts Under Ref. V	−5.04	−3.63	−5.03	−9 mV	−2 mV	−19.5	−3.95
Enable Terminal Available	Yes	Yes	Yes	Yes	Yes	No	No
Supply Volts (V)	+5.0	+5.0	+5.0	+5 −5	+5 −5	+5 −16	+5
Supply Current (mA)	15.1	13.2	6.5	13.6 7.8	11.4 7.0	13.3 6.4	20.8

*Reference voltage for circuits 12 and 13 was about 25 mV for this test.

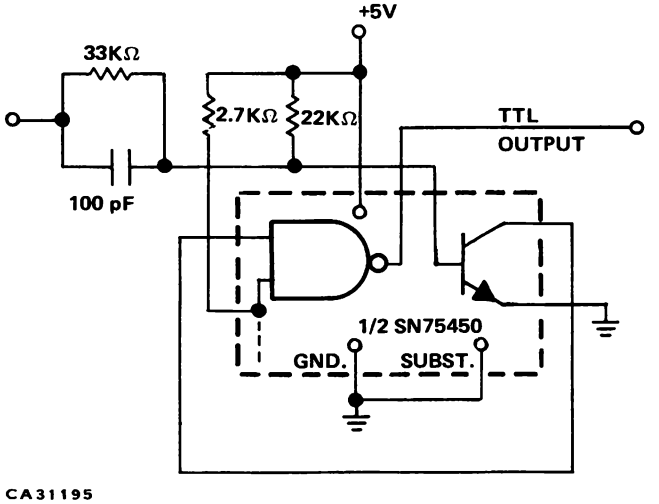


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FIGURE 9. MOS to TTL Level Shift Circuit Using a One-Half of a SN75450 Peripheral Driver

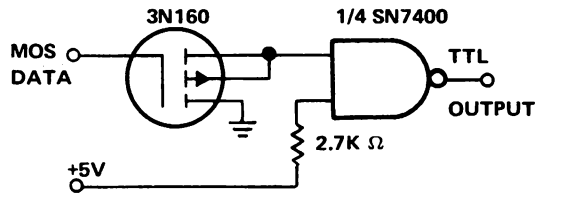

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FIGURE 10. MOS to TTL Level Shift Circuit Using a 3N160 MOSFET

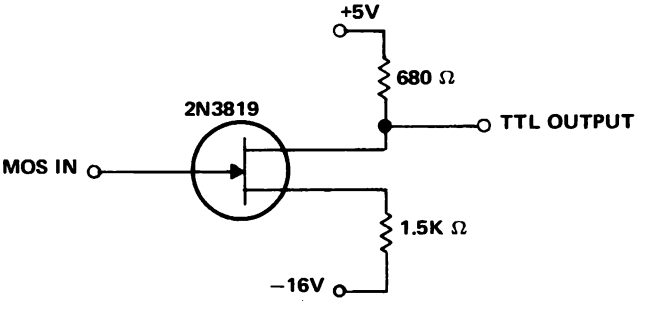

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FIGURE 11. MOS to TTL Level Shift Circuit Using a 2N3819 JFET

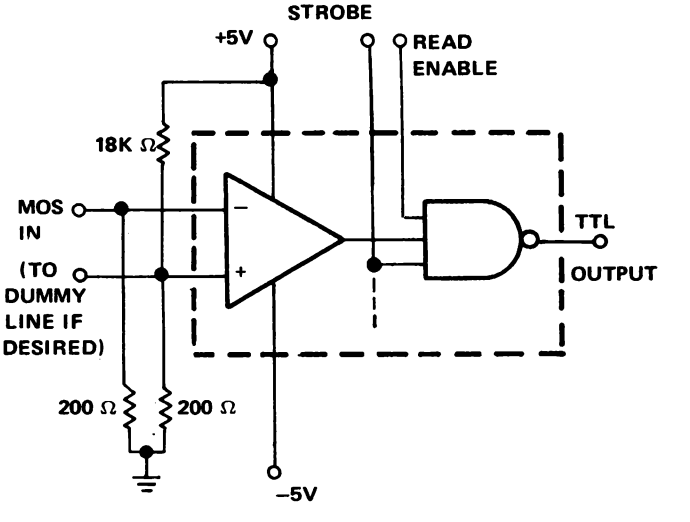

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FIGURE 12. MOS to TTL Level Shift Circuit Using a One-Half SN75107 Data Line Receiver

the TMS1103 are two such circuits. A sensitive high speed circuit is required with these circuits. The SN75107A/108A or SN75207/208 data line receivers meet these requirements. Figures 12 and 13 show the two circuits being used in this configuration.

The SN75107A has a standard TTL output and an input sensitivity of $\leqslant \pm$ 25 mV. The SN75108A is the same, but it has an open collector output. The SN75207/208 are similar to the SN75107A/108A but they have input sensitivities of $\leqslant \pm$ 10 mV. In this application, the interface is acting as a memory sense amplifier. The speed, sensitivity, temperature stability, and stability with supply variations make the SN75207 or SN75208 most desirable for these applications.

Another unique and versatile interface device is the SN75270 and is shown in a circuit configuration in Figure 14. The SN75270 is a seven channel MOS to TTL

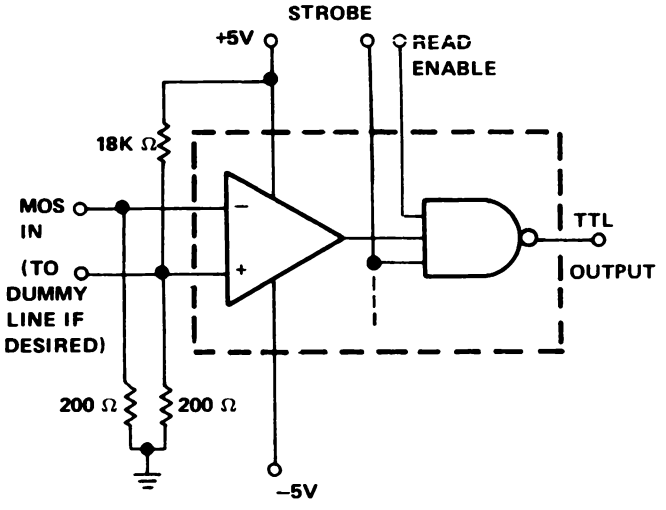

FIGURE 13. MOS to TTL Level Shift Circuit Using a One-Half SN75207 Data Line Receiver

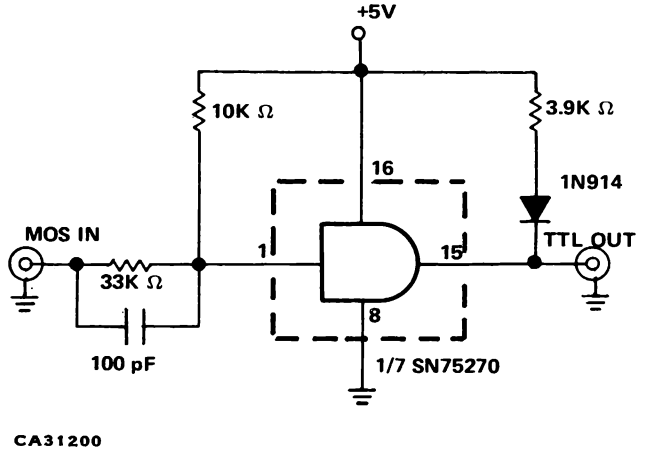

FIGURE 14. MOS to TTL Level Shift Circuit Using One-Seventh of a SN75270 MOS to TTL Converter

converter with each channel capable of converting an MOS output current to TTL logic levels at its outputs. The low standby power of 100 mW and high operating speeds make this multichannel device very desirable for many MOS to TTL applications.

Table 2 provides a comparison of the performance characteristics of the MOS to TTL interface circuits shown in Figures 8, 9, 10, 11, 12, 13, and 14.

TTL COMPATIBLE COMBINATION MOS DRIVER SENSE AMPLIFIERS

The circuits shown in Figures 15 and 16 are combination write (or drive) and read (or sense) circuits. Their compactness, speed of operation, and control features make them particularly suited for more complex memory systems incorporating MOS circuits like the TMS4062JC 1024 word by 1 bit dynamic RAM.

Figure 15 shows a circuit that uses a combination of discrete and integrated circuits. Figure 16 is a completely monolithic approach. The SN75370 is a self-contained dual channel sense-digit driver. A component comparison provides some revealing information. It requires two SN75451 packages, one SN72711 package, four 2N4401 transistors, and 16 resistors to duplicate the function of one SN75370. Performance comparisons of the two circuits shown in Figures 15 and 16 are shown in Table 3.

For typical applications care should be taken to insure the loading conditions of the system being considered do not exceed the circuit parameters listed in Tables 1, 2, and 3.

A typical configuration using one-half of a SN75370 is shown in Figure 17. With a V_{SS} of 20 volts, and a V_{REF} of 7 volts, the following typical characteristics can be expected:

Bit driver propagation delay is ≈ 30 ns (60 pF load).

Sense amplifier/converter propagation delay is ≈ 40 ns.*

Power dissipation is ≈ 550 mW with both channels in read mode.

Power dissipation is ≈ 700 mW with both channels in write mode.

Standby power dissipation is ≈ 350 mW with the chip disabled.

* The output current from the TMS4062 approximates the characteristics of a ramp function rather than a step function. This ramp characteristic causes the SN75370 to respond within 10 nanoseconds as compared to the typical 40 nanoseconds for a step function.

Figure 18 is a block diagram of a 17 X 18K memory using TMS4062, SN75361 and SN75370 devices. Dual channel SN75361 circuits are used to drive the clock, reset, and address inputs. Read/write inputs are driven and sensed by SN75370 dual bit driver/sense amplifier/converters.

Figure 19 shows a basic circuit illustrating the use of SN75361 drivers and SN75208 sense amplifiers operating with a TMS1103 to form a 4096 9 bit bytes system.

Table 4 is a tabulation of the interface circuits discussed, cross-referenced with a list of typical MOS circuits each may be used with. It is important to note that system performance requirements as well as economics will effect exactly which interface may be best suited in any particular application.

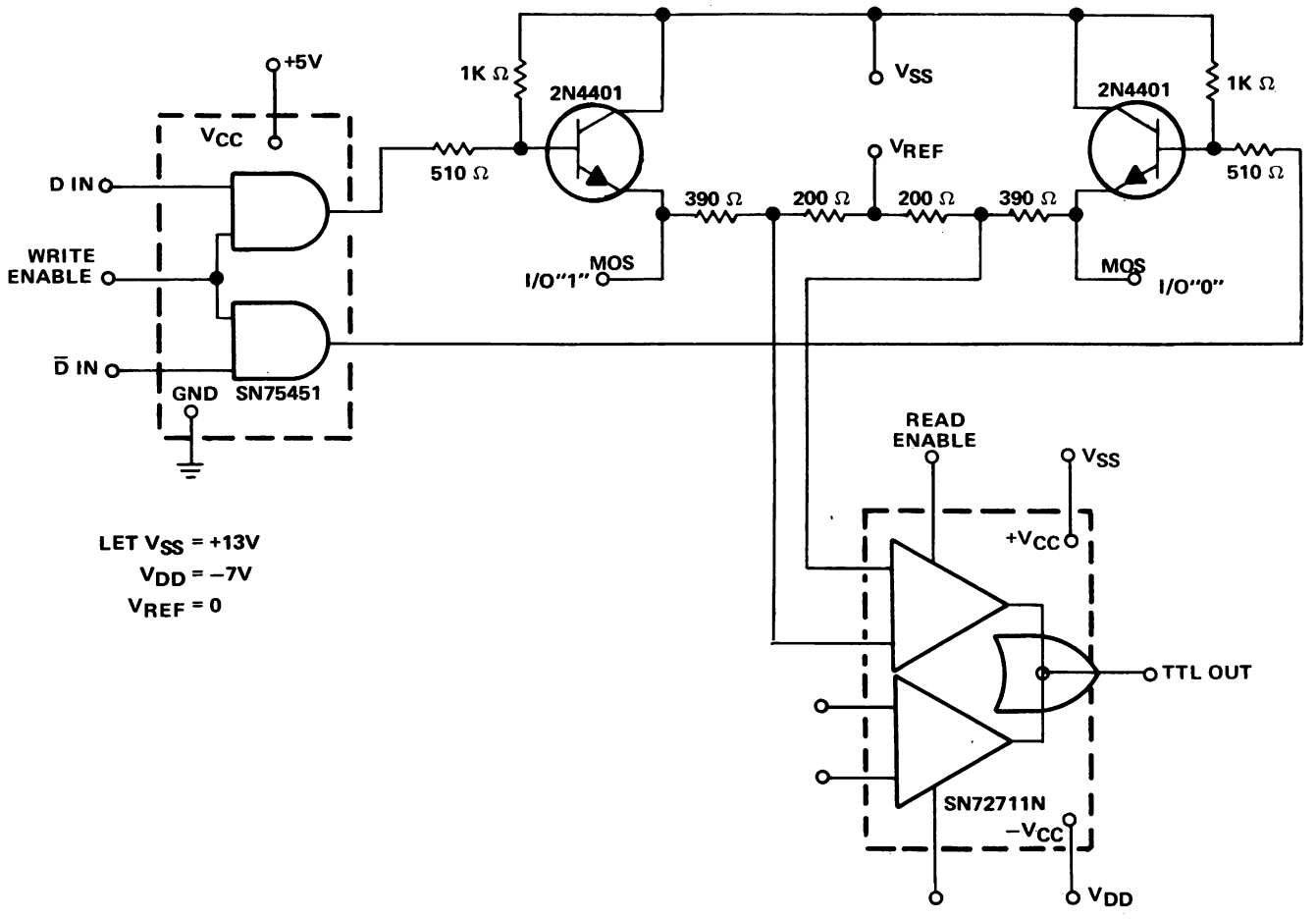

FIGURE 15. MOS to TTL Interface Using a SN75451 Sense-Driver

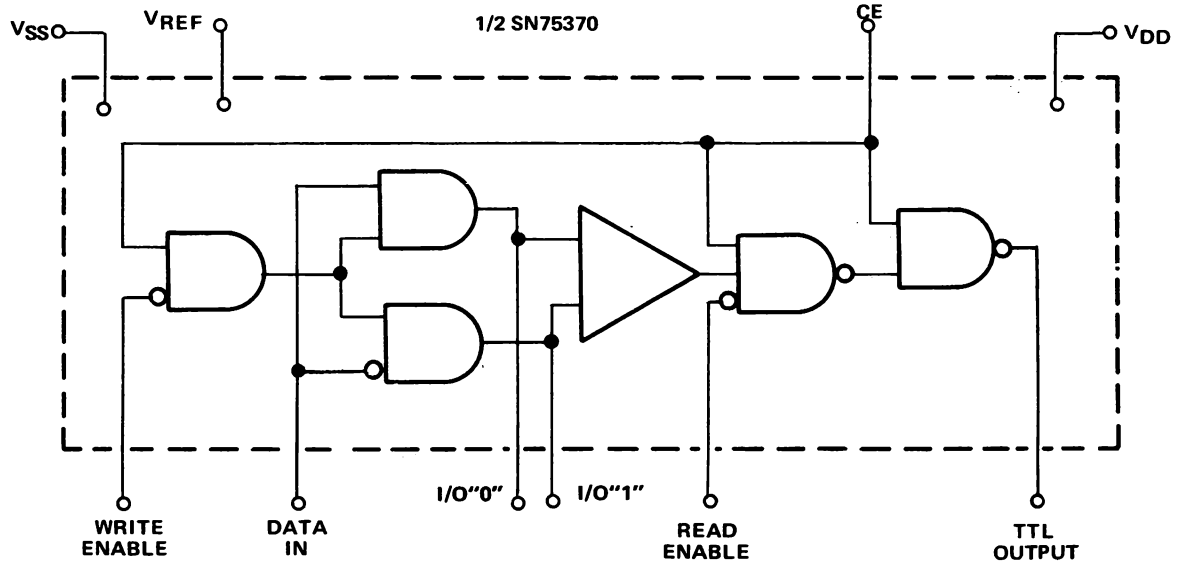

FIGURE 16. MOS to TTL Interface Using One-Half of a SN75370 Sense-Driver

Table 3. Comparative Performance Data for the Circuits Shown in Figures 15 and 16

Circuit	SN75370 (Circuit 16)					Discrete (Circuit 15)				
	Write		Read			Write		Read		
	T_{PD} to I/O Line		T_{PD} to Output		Max.	T_{PD} to I/O Line		T_{PD} to Output		Max.
MOS "C" Load	L-H (ns)	H-L (ns)	L-H (ns)	H-L (ns)	Freq. (MHz)	L-H (ns)	H-L (ns)	L-H (ns)	H-L (ns)	Freq. (MHz)
50 pF	19.2	20.2	20.4	32.1	6.6	48.3	59.6	21	33	3.3
100 pF	21.0	24.7			6.6	55	95			3.3
700 pF	48.1	48.6			3.3	85	129			1.6
2K pF	113	105			1.3	168	320			0.67

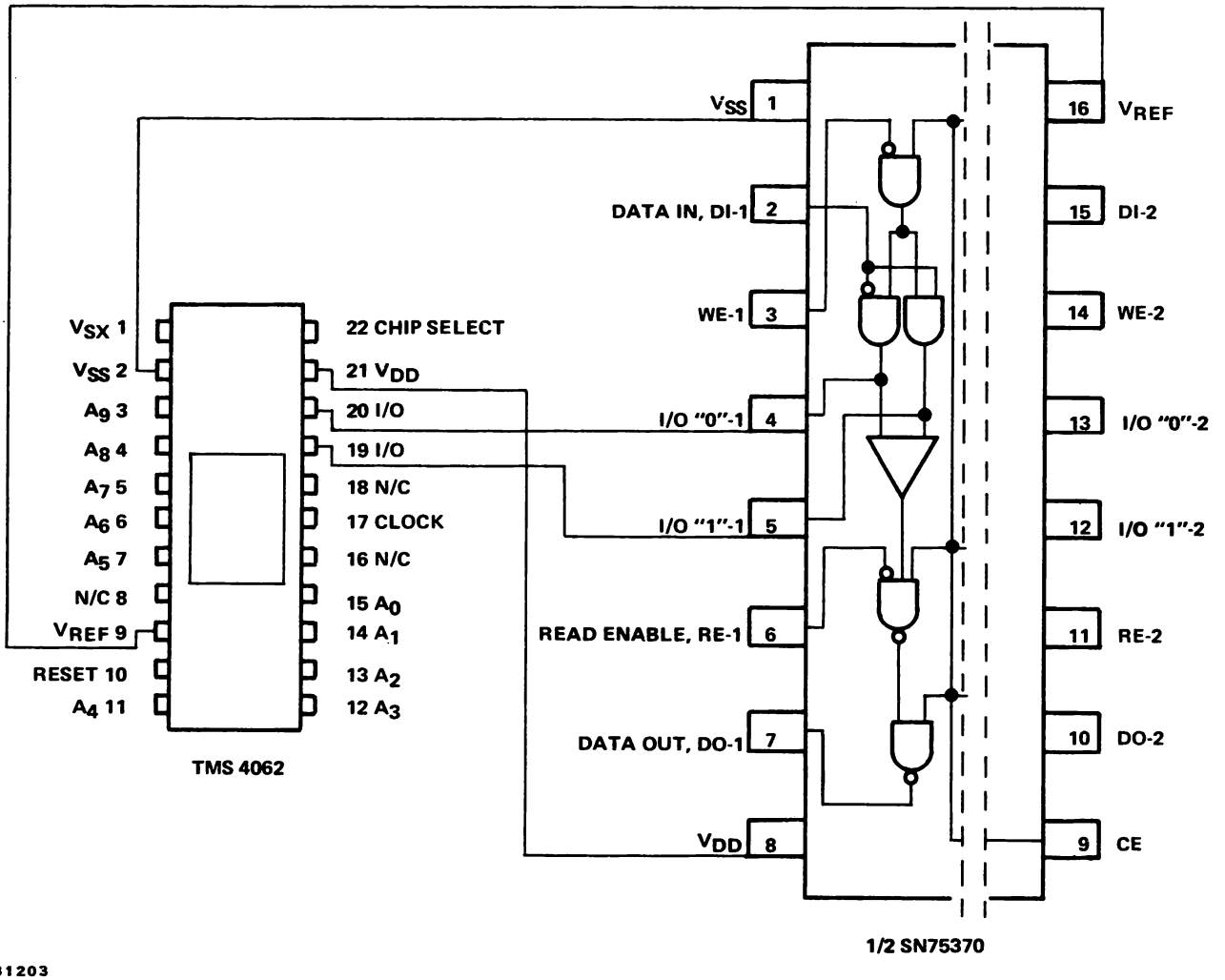

FIGURE 17. Circuit Configuration Using One-Half SN75370 to Interface a TMS4062 RAM

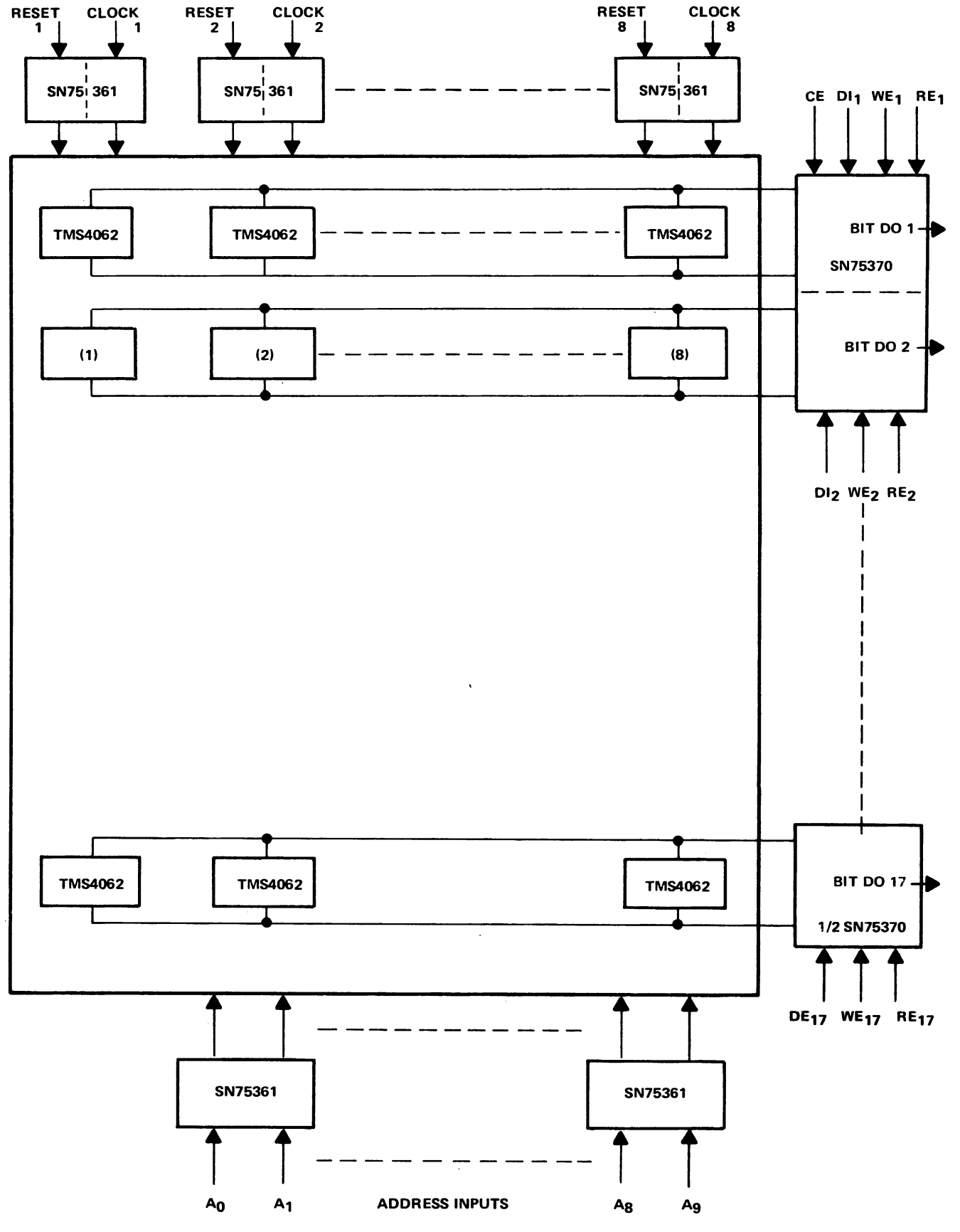

FIGURE 18. Block Diagram of a 17 X 18K Memory Using TMS4062, SN75361 and SN75370 Devices

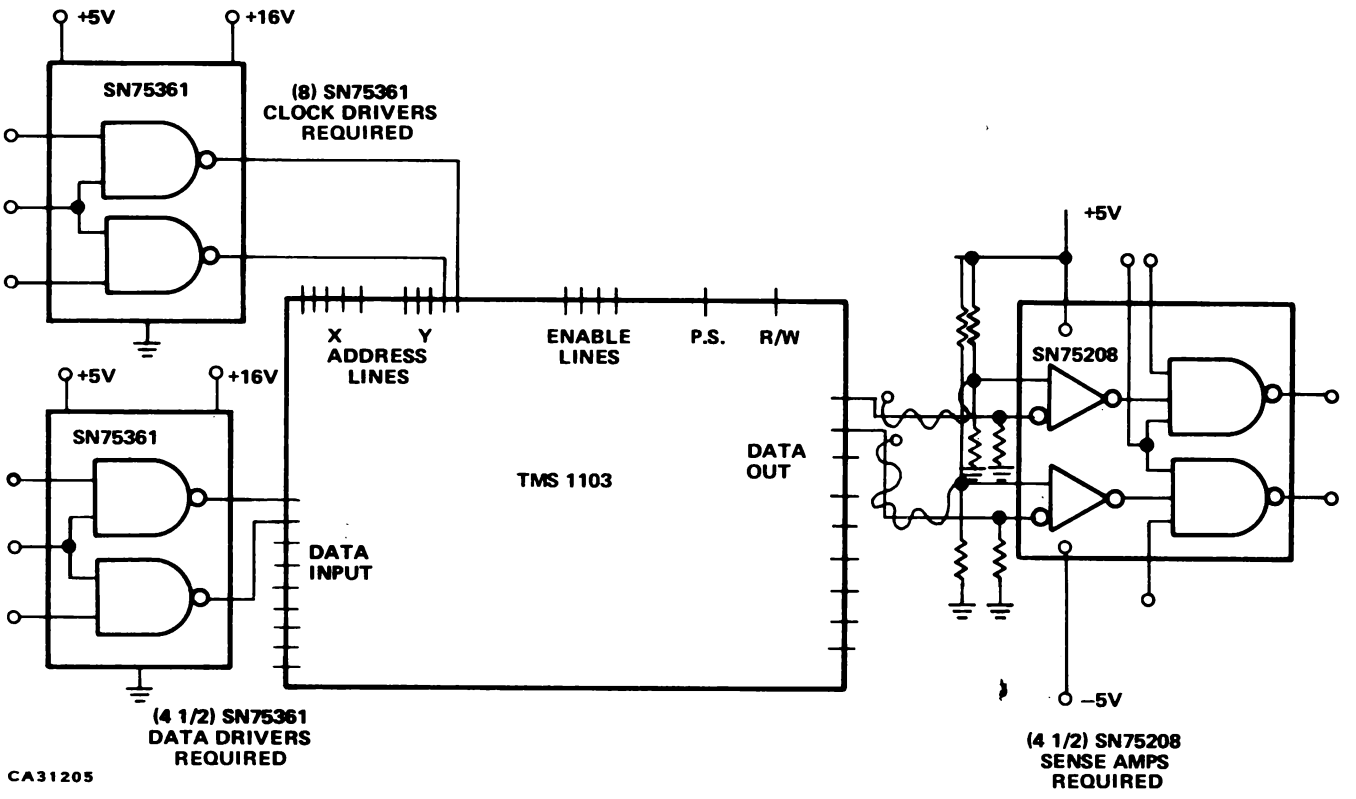

FIGURE 19. A 4096 9 Bit Bytes System Using TMS1103, SN75361 and SN75203 Devices

Table 4. Specific Drivers and Sense Amplifiers That Can Be Used As Interface Circuits With Some Typical MOS Shift Registers and Memories

	Driver Circuit Number							Sense Circuit Number							Sense-Digit Driver Number	
MOS Circuits	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TMS1101 TMS1103				X	X							X	X			
TMS4062															X	X
Series 3000	X	X	X			X		X	X	X	X			X		
Series 3100	X	X	X			X		X	X	X	X			X		
Series 3400	X	X				X		X	X	X	X			X		
Series (TTL) 2000											X			X		
Series 2600	X	X	X			X	X	X	X	X	X			X		
Series (TTL) 2700											X			X		
Series 2800/2900	X	X	X			X	X	X	X	X	X			X		
Series 4000	X	X	X			X	X	X	X	X	X			X		
Series 4100/4400	X	X	X			X	X	X	X	X	X			X		

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Reduction in Power Dissipation of MOS Static Shift Registers By Pulsing Device Supply Rails

(B 97)

REDUCTION IN POWER DISSIPATION OF MOS STATIC SHIFT REGISTERS BY PULSING DEVICE SUPPLY RAILS

By Derek Skinner

INTRODUCTION

Power dissipation of MOS Static Shift Registers is necessarily high to allow 1MHz operation of the cross-coupled latch within each cell of the register. In many applications where only a small number of registers are used, total power dissipation is small enough to be of no consequence. However, in some systems, as used in satellite, airborne or standby equipment, a large number of shift register packages may be necessary and the attendant high power dissipation is intolerable. Hence a means of reducing the power dissipation of static MOS shift registers was investigated by application of a pulsed, rather than a constant, power supply to the shift registers. All measurements were made using TMS 3002 LR, dual 50 bit static shift registers; power dissipation reduction by the above method being practicable only during the time that the shift register clocks are in the correct state for long term data storage. Note, however, that the above technique may be applied to the majority of the current range of T.I. MOS Static Shift Registers and most probably a similar method may be applied to other MOS devices such as Read Only Memories and Random Access Memories.

CIRCUIT OPERATION

The TMS 3002 LR requires two power supply rails of nominally $-14V$ (V_{DD}) and $-28V$ (V_{GG}) with respect to the device substrate (V_{SS} rail). For the purpose of the investigation the following supply voltages were used.

$V_{SS} = +28V$ $V_{DD} = +14V$ and $V_{GG} = 0V$

Determination of which supply rail should be pulsed can be made if the circuit of each storage cell within the register is considered. See Figure 1.

Each cell comprises 6 p-channel enhancement mode MOS transistors, a series coupling device being included between cells. A device is thus 'off' (high impedance) when the gate to channel potential is zero and 'on' when the gate to channel potential is more negative than the threshold voltage. The action of each cell, comprising a cross-coupled latch, is as follows:–

1. Device VT1 is turned on, thus allowing data to be stored in the cell on C1, devices VT4 and 5 being off, so that the cross-coupling is undone.

2. New data now appears at the drain of VT2, previous data being still present on C2 and at the drain of VT7. VT1 is now turned off, locking data out of the cell.

3. After a slight delay, VT4 turns on, transferring new data onto C2 and hence to the drain of VT7. VT5 is then turned on, thus completing the cross coupling and the latch is actively held in the desired state. Clock pulse $\phi 1$ is now held at V_{SS} potential and $\phi 2$ and $\phi 3$ at approximately V_{DD} potential. Under these conditions data is stored indefinitely in each cell of the register. However, it is possible to utilise the inherent gate-source capacitance of devices VT2 and VT7 to store information temporarily when the clock is stopped without supplying any power to the register.

Pulsing the V_{GG} power supply rail produces the desired condition by turning off devices VT3 and VT6 within each cell, which act as load resistors for devices VT2 and VT7. The drain terminals of VT2 and VT7 are effectively isolated from the V_{DD} rail via a very high resistance and information

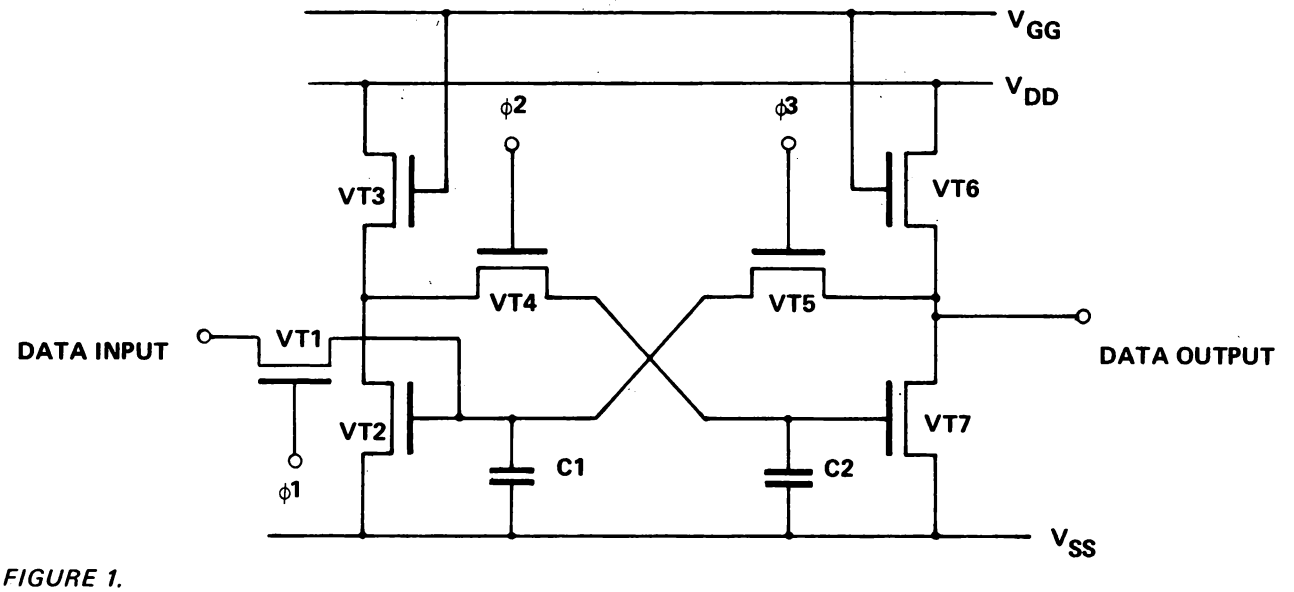


FIGURE 1.

within each cell is stored on capacitors C1 and C2 for some appreciable time. As all MOS devices in the register are of insulated gate construction, the leakage current flowing in the gates of VT2 and VT7 is of the order of a few pico amps, this representing a very high impedance discharge path to V_{SS}. In addition for, say, capacitor C1 charged towards V_{DD} there is a further discharge path through VT5 which is on and VT7 which is off. The drain to source leakage current of VT7 when off is of the order of a few nanoamps, and hence C1 will predominantly discharge through this path.

If information is entered into a storage cell in the register and devices VT3 and VT6 are turned off, then capacitor C1 or C2 is still sufficiently charged after 100μs for the cell to remain latched in its original state when the V_{GG} supply is restored, and VT3 and VT6 return to their normal state of conduction. The repetition rate of the pulse applied to the V_{GG} rail is, therefore, chosen as nominally 10kHz.

A simple pulsing circuit comprising one transistor and resistor was initially tested, as shown in Figure 2.

With V_{GG} supply applied and the clock running the register was filled with either all logical zero information (+28V) or logical one information (+14V). The clock generator was then stopped with $\phi 1$ at a logical zero (+28V) and the $\phi 2$ clock at logical 1 (+14V). The V_{GG} supply was then restored to a constant voltage of 0V, the input data changed to the opposite logic level, and the clock restarted. The ensuing data output of the register, together with the $\phi 1$ and $\phi 2$ clock pulse trains were measured on a storage oscilloscope. The stored traces were then checked to ensure that no data in the register had been lost during the time that the V_{GG} rail was pulsed. This test was repeated for decreasing intervals of time, t1, applying both a continuous logic 1 and subsequently a logic 0 at each increment until the point was reached at which data was lost. The value of t1 (min) <100ns. Hence a value of t1 = 200ns is chosen.

It was found that in order to ensure that devices VT3 and VT6 were completely off, the V_{GG} rail should be pulsed to +22V approximately and hence the value of t1 was measured at this voltage. For simplicity of design it is recommended that the V_{GG} rail should be pulsed between 0V and +28V, this causing no damage to the device, and ensuring safe operation with device parameter variation.

The above tests were then performed again at +80°C to ensure that the inevitable increase in leakage currents within the device caused negligible change in the above results. This was found to be the case.

From examination of Figure 1 and the data sheet of the TMS 3002 LR it is seen that the V_{GG} rail of the shift register is connected solely to 200 individual device gates. The inherent capacity between each gate and its associated substrate is approximately 0.25pF. Hence the V_{GG} pulsing circuit must be capable of charging and discharging 50pF capacity for each package in the system. For a system comprising, say, 24 x 50 bit shift registers it is therefore necessary to drive 600 – 700pF capacity and retain fast pulse rise and fall times.

On the basis of the above results a suitable pulsing circuit dissipating the minimum of power was designed. See Figure 3.

The action of the circuit is as follows:–

Transistors VT1 and VT2 and components R1, R2, R3, R4 and C1 comprise the main oscillator. VT1 and VT2 perform the same function as a unijunction transistor with the advan- of a very high off impedance as compared with the static interbase resistance of the unijunction (typically only 6kΩ). This is important as a true unijunction transistor will thus inevitably dissipate a significant amount of power during the time it is 'off'. The use of two bipolar transistors also improves the stability of operation of the circuit with temperature variation and parameter spread from one device to another. The output pulse from the emitter of VT2 has a fast risetime but a rather slow fall time. This pulse is fed to the base of VT3 via R5 and associated speed up capacitor C2, VT3 having the effect of providing a wider pulse width and decreased fall time, hence squaring off the waveform. VT4 provides the necessary phase inversion and relatively low output impedance to drive the capacitively coupled output stage via capacitor C4 and C5 to the bases of transistors VT5 and VT6. Resistors R9 and R10 hold both output devices normally off. Low power dissipation as well as the capability to drive highly capacitive loads are achieved by the inclusion of transistor VT5. This device is pulsed 'on' at the moment when VT6 is turned 'off' thus quickly charging the V_{GG} rail capacitance. VT5 then turns 'off' due to capacitor C4 charging via the base current of VT5 and the current through R9, the 33kΩ resistor to +28V then holding the V_{GG} rail capacitance charged during the 100μs 'off' time. Diode D1 clamps the V_{GG} rail voltage to approximately –0.7V – should overshoot or ringing occur, thus protecting the shift register against over voltages. The diode should be connected directly between the V_{GG} terminal on the register and the true 0V power supply.

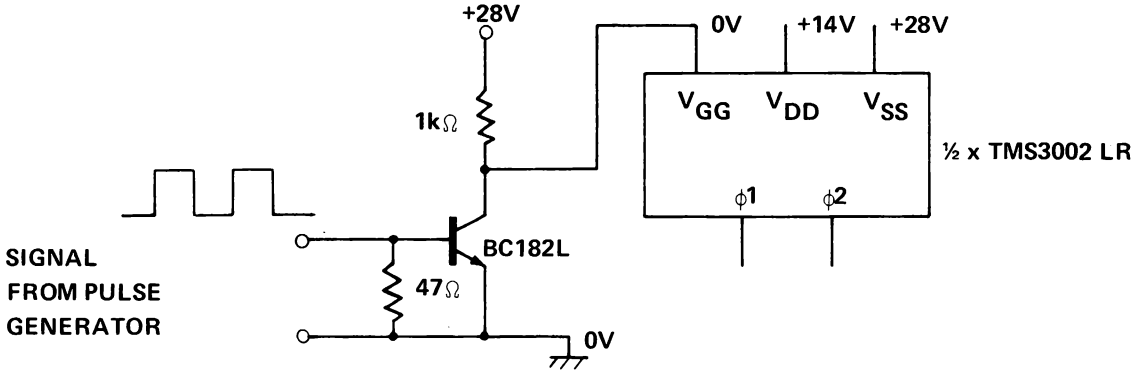


FIGURE 2.

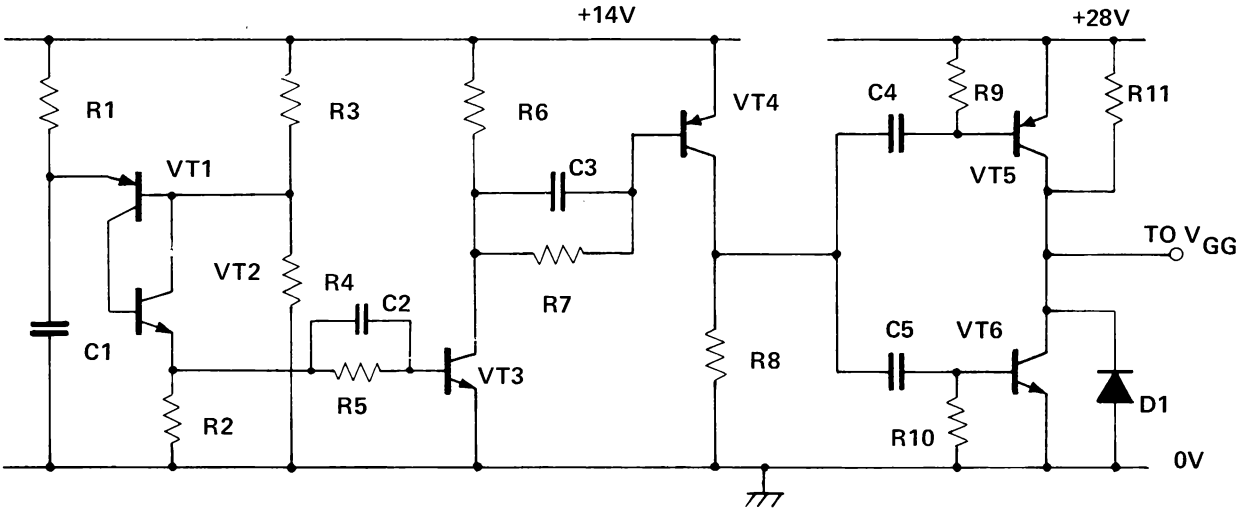


FIGURE 3. **See List with Figure 7 for component values**

The rise and fall times of this output pulse are shown below in Figures 4 and 5.

Figure 6 shows the repetition rate of the pulsing circuit.

It seems that the effective pulse width (t1) at +22V (where I_{DD} is ≃ 0) is approximately the same for both figures 4 and 5, and hence the effective mark space ratio is 1 : 500 for each case.

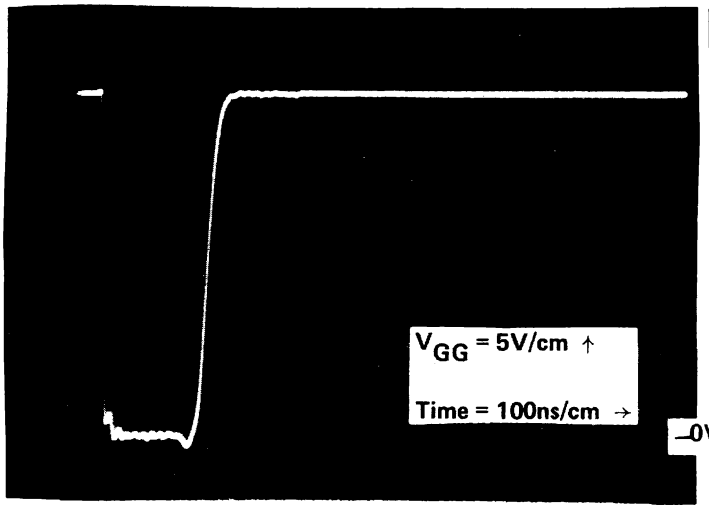


FIGURE 4. Output of Pulsing Circuit Driving 10MΩ and 7pF

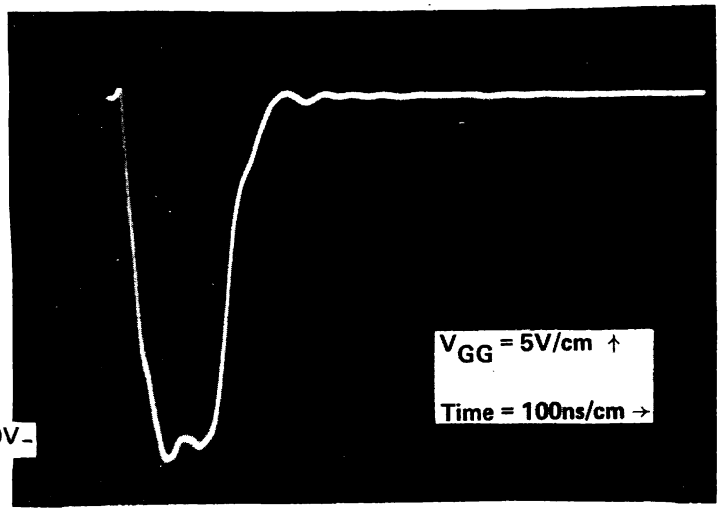


FIGURE 5. Output of Pulsing Circuit Driving 1 Package and a 470pF Capacitor to Simulate a Further 11 Shift Registers

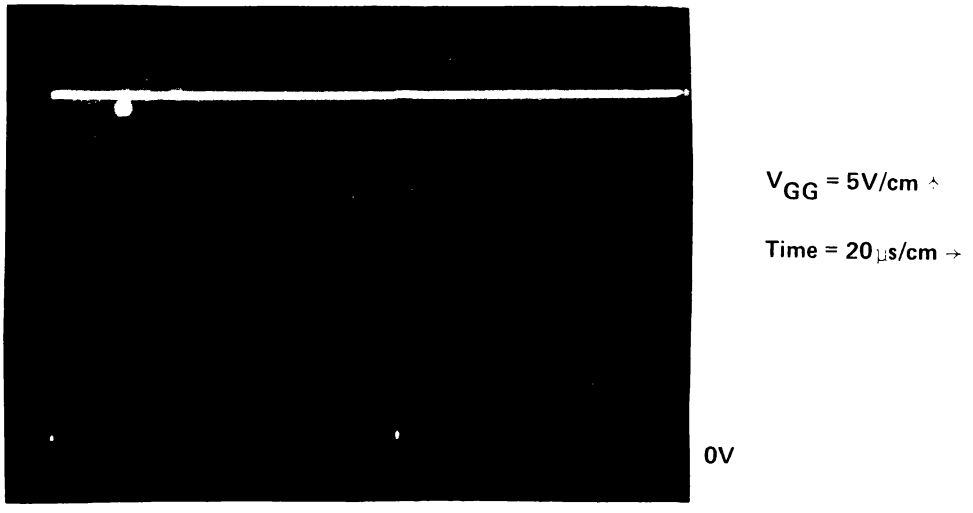


FIGURE 6. Output of Pulsing Circuit Showing Repetition Rate.

POWER DISSIPATION WITHIN THE SYSTEM

The described pulsing circuit was constructed and connected to 1 x TMS 3002 LR as shown below in Figure 7.

In order to meaningfully measure power dissipation without affecting the operation of the circuit, both the +28V and +14V rails were decoupled by 100μF and 0.1μF capacitors on the actual circuit board. An avometer was then inserted in series with the wire from the power supply to the decoupling capacitors. A reading of the mean current drawn from the supply was thus obtained and hence the mean power input to the system. The measured current and power dissipation are set out below:–

1. V_{GG} rail = 0V = constant, (S1 in position 2), Pulsing Circuit running

Note that shift register supply current was found to be substantially independent of data in register

$I_{(28)} = +9.2mA$ $I_{(14)} = +6.8mA$

$I_{GG} = +1.4mA$ $I_{(2)} = +1.60\mu A$ $I_{(1)} = +1.03mA$

Power dissipated in Device due to V_{DD} rail =

$P_{(V_{DD})} = (V_{SS} - V_{DD}) \times I_{DD}$

$I_{DD} = I_{(14)} + I_{(1)} = +6.8 + 1.03$

$= +7.83mA$

$\therefore P_{(V_{DD})} = 14 \times 7.83mW = 110mW$

Power dissipated in device due to V_{GG} rail

$= (V_{SS} - V_{GG}) \times I_{GG}$

$= 28 \times 1.4mW = 39mW$

Total shift register dissipation = 150mW

Power dissipation in first part of pulsing circuit

$= V_{DD} \times I_{(1)}$

$= 14 \times 1.05mW = 14.7mW$

Power dissipation in output stage of pulsing circuit

$= V_{SS} \times I_{(2)}$

$= 28 \times 0.16mW = 4.5mW$

Total power dissipated in pulsing circuit

$= 19.2mW$

2. V_{GG} rail pulsed on for 200ns in every 100μs (S1 in position 1)

$I_{(28)} = +180\mu A$ $I_{(14)} = -1.013\ mA$

$I_{GG} = +3\mu A$ $I_{(2)} = +160\mu A$ $I_{(1)} = +1.03mA$

Total power dissipated in pulsing circuit = 19.2mW (from (1) above).

Power dissipated in device due to V_{DD} rail

$P_{(V_{DD})} = (V_{SS} - V_{DD}) \times I_{DD}$

$I_{DD} = I_{(14)} + I_{(1)} = 1.03 - 1.013mA = +17\mu A$

$\therefore P_{(V_{DD})} = 14 \times 17 \times 10^{-6}$ W $= 0.238mW$

Power dissipated in device due to V_{GG} rail

$= (V_{SS} - V_{GG}) \times I_{GG}$

$= 28 \times 3 \times 10^{-6}$ W

$= 84\mu W$

Total shift register power dissipation = 0.238 + 0.084 mW

$= 0.332mW$

Therefore typical power dissipation of a system comprising one pulsing circuit and 12 x Dual 50 bit static shift registers, operating statically with both clock phases held at constant voltages:–

= Power input to pulsing circuit + 12 x V_{DD} power input + 12 x V_{GG} power input

$= 19.2 + 12 \times 0.238 + 12 \times 0.084$ mW

$= 19.2 + 2.86 + 1.01$ mW

$= 23.1$ mW (typical)

From the above measurements it will be seen that the power dissipation if one device under static supply conditions is typically 150mW, and under pulsed conditions typically 0.332mW. An approximate 450 : 1 reduction in power dissipation under conditions of 500 : 1 MSR pulsed supply rail operation is thus achieved without loss of data. Of course, there is no guarantee of the repeatability of these measurements with all possible device parameter variations. However, it was found possible to reproduce the above results with a random sample of 6 TMS 3002 LR over the temperature range of 0 to 80°C. If a reduction in power consumption to only, say, 1/200th of the static value is tolerable, then it is possible to design for a power supply 'on' time of 500ns in every 100μs. This should ensure completely reliable operation with all device parameter variations and over the complete operating temperature range of the device.

It will, of course, be necessary to disable the pulsing circuit during the time that the register is to be clocked. However, it may be possible to pulse the V_{GG} supply in synchronism with the $\phi 1$ and $\phi 2$ clock pulses, although such circuitry as will be necessary is complex and requires considerable additional evaluation work. Furthermore, it appears likely that the reduction in power dissipation within the register would be considerably less than that possible under long term data storage conditions.

In a system where low power is an important criterion, a clock driver circuit having low power dissipation is necessary. Provided that the time during which $\phi 1$ and $\phi 2$ are running is small compared to the time when $\phi 1$ and $\phi 2$ are static, then the power consumption of the clock circuit is relatively unimportant. This is true because the majority of power dissipated in the driver circuit occurs during the switching transients, when the register clock capacity is charged and discharged. As the clock inputs are almost purely capacitive, virtually no power is required to hold them at a constant voltage during static data storage. Hence under the above conditions, the mean power dissipation of the clock circuit is very small.

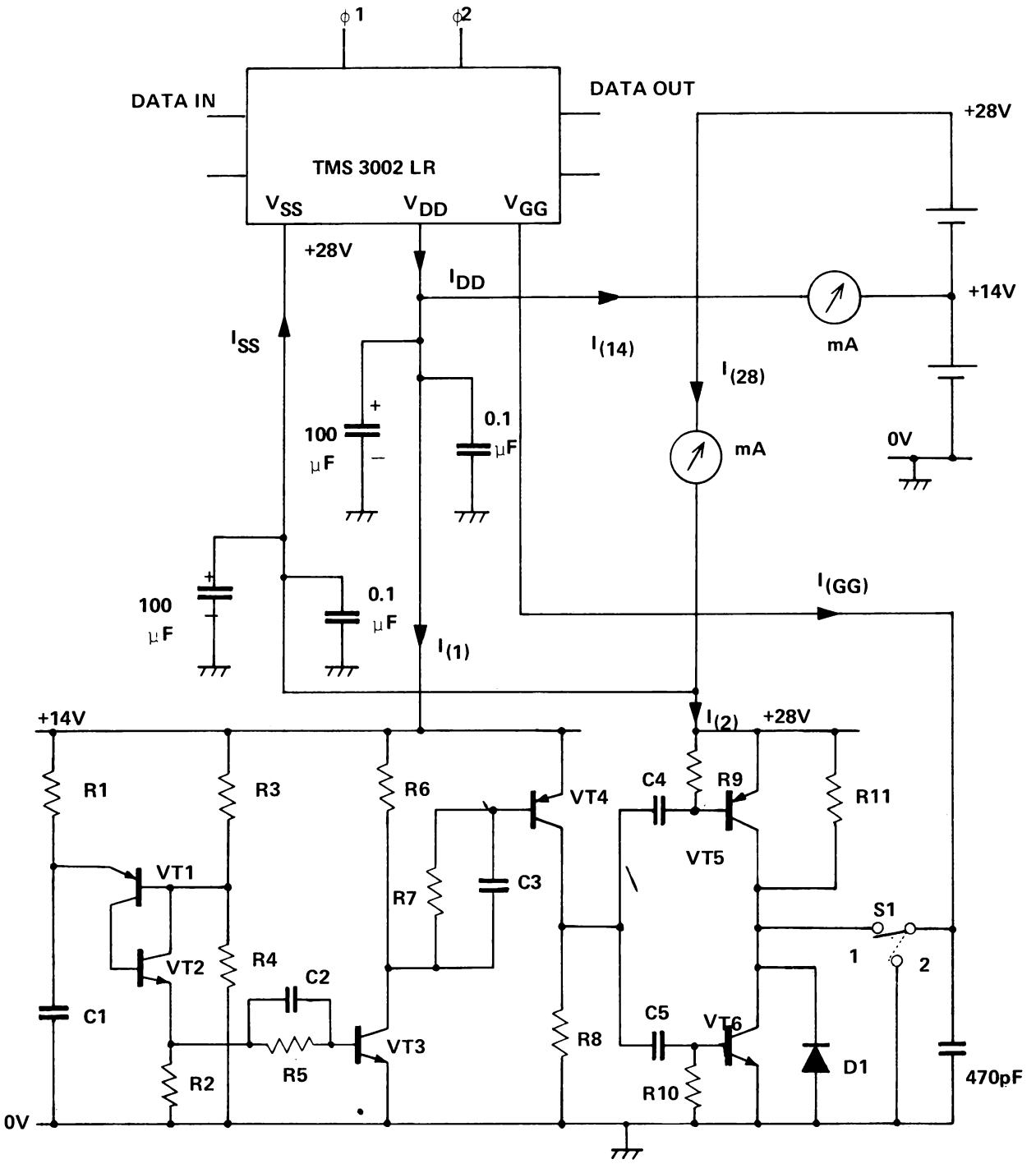


FIGURE 7.

R1	=	680kΩ	R6	=	1k	C1	=	400pF	VT1	=	TIS50
R2	=	100Ω	R7	=	10k	C2	=	330pF	VT2	=	TIS49
R3	=	10k	R8	=	470	C3	=	22pF	VT3	=	BC182L
R4	=	4k7	R9	=	47k	C4	=	47pF	VT4	=	BC212L
R5	=	2k2	R10	=	47k	C5	=	47pF	VT5	=	BC212L
			R11	=	33k	D1	=	1S44	VT6	=	BC182L

In all the above tests the only load on the data output of the shift register was a scope probe presenting a loading of 10MΩ and approximately 7pF capacity. In practice the output stage of the register will probably be loaded rather more heavily. This may cause the register output voltage to change during the time that the V_{GG} rail is pulsed 'off'. A buffer stage on the register output therefore may be necessary. This could be achieved by driving the register output into the gate of a discrete field effect transistor presenting very little loading to the register and, therefore, not significantly discharging the storage capacitors within the last cell. Another alternative is the use of a type of latch as an output buffer. This could be set to give the correct output each time that the register is clocked and can be arranged to hold the information during the time that the V_{GG} supply is pulsed.

CONCLUSIONS

It is shown that it is feasible to reduce the power dissipation of static shift registers, while clocks $\phi 1$ and $\phi 2$ are in the state for long term data storage, by turning 'off' the load resistor MOS FETs in each cell of the shift register. This is achieved by pulsing the V_{GG} rail of the shift registers 'on' with a mark space ratio of 1 : 500 every 100μs approximately. A reduction in power dissipation of each register to approximately 1/500 of the normal static power dissipation is therefore possible. The above circuitry was found to work for every device in a random sample of shift registers at room temperature and +80°C. However, sufficiently

ature and +80°C. However, it was not possible to test the above circuit with a sufficiently large number of devices to ensure reliable operation over the possible device parameter spread, but the feasibility of the mode of operation is shown

NEW SHIFT REGISTERS FROM TEXAS INSTRUMENTS

Device Number	Function	TTL Compatibility		Recirculate Logic
		Data	Clock	
TMS310/LC/NC	Dual 100 Static	*		
TMS3102LC/NC	Dual 80 Static	*		
TMS3103LC/NC	Dual 64 Static	*		
TMS3112JC/NC	Hex 32 Static	*	*	*
TMS3113JC/NC	Dual 133 Static	*	*	*
TMS3114JC/NC	Dual 128 Static	*	*	*
TMS3401LC/NC	Single 512	*		
TMS3402LC/NC	Single 500			
TMS3404JC/NC	Dual 512 Dynamic	*		
TMS3409JC/NC	Quad 80 Dynamic	*	*	*
TMS3412JC/NC	Quad 256 Dynamic	*		
TMS3413LC/NC	Quad 512 Dynamic	*		
TMS3414LC/NC	Single 1024 Dynamic	*		
TMS3417JC/NC	Quad 64 Dynamic	*	*	*

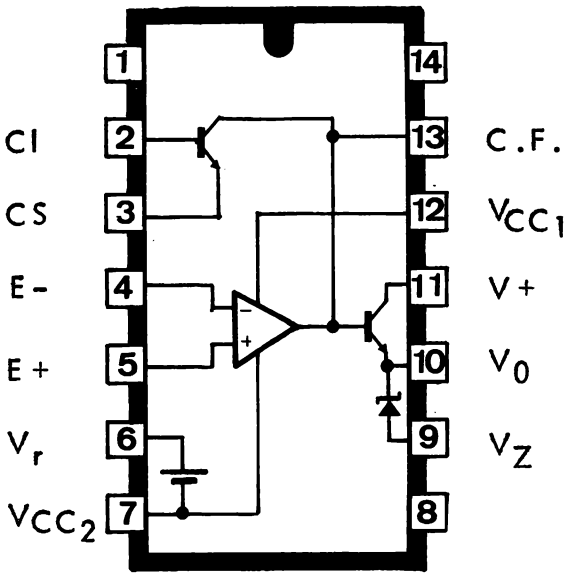
Regulateur 72723 (NA 62)

REGULATEUR SN 52/72 723

1. DESCRIPTION

Le régulateur SN 52/72 723 se compose de deux parties distinctes :

- Une source de tension de référence (tension nominale 7,15V)
- Le régulateur proprement dit.



SN 52/72 723 N

1.1. Source de tension de référence (Fig. 1)

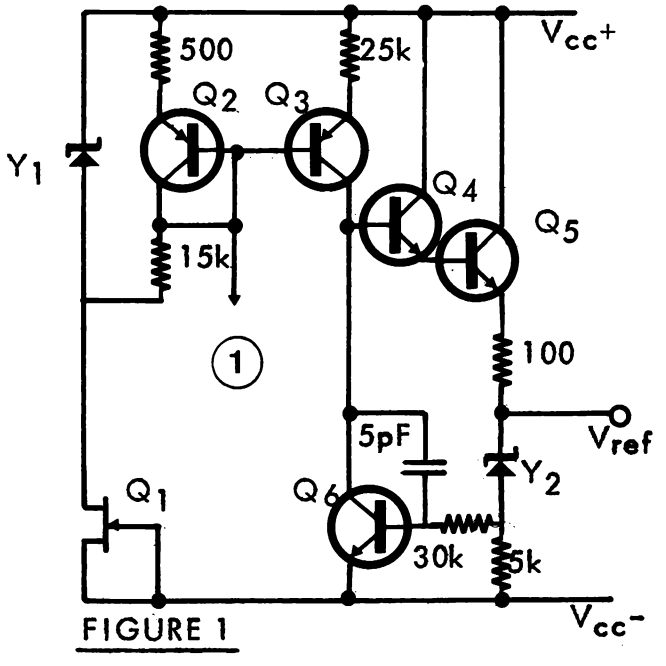
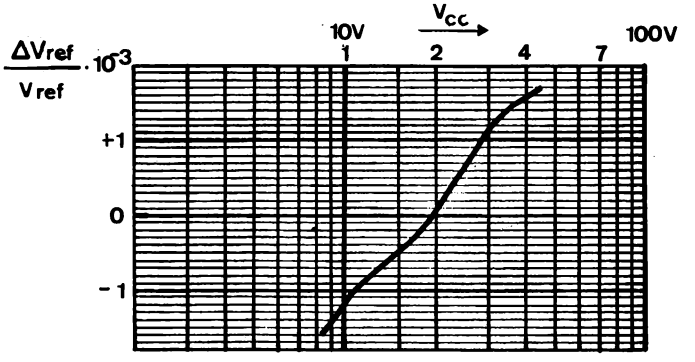
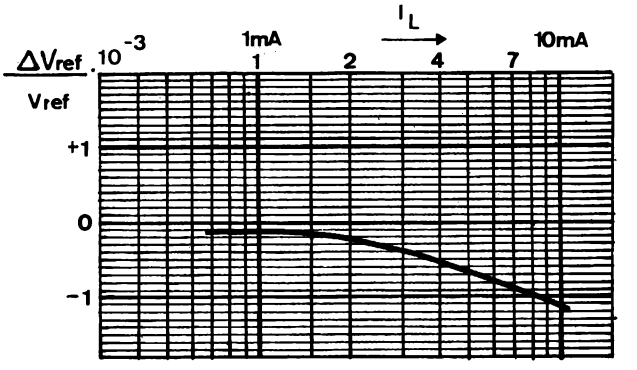


FIGURE 1

La source de tension de référence est essentiellement composée de la diode zener Y_2, de l'amplificateur d'erreur Q_6 et de l'amplificateur de puissance Q_4, Q_5. Ce montage a deux buts : compenser le coefficient de température de la diode z ener mais surtout, permettre qu'elle soit alimentée par un courant constant quels que soient le courant de charge et la tension d'alimentation comme le montrent les deux courbes ci-dessous : la première représente la variation relative de la tension de référence en fonction de la tension de référence en fonction de la tension d'alimentation et la seconde la même variation relative en fonction du courant de charge.





La source de tension de référence peut être alors représentée par le schéma simplifié de la figure 2.

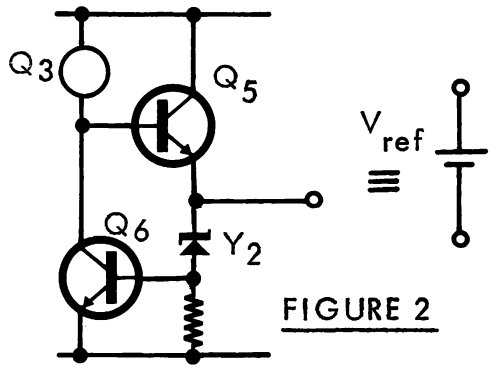


FIGURE 2

Toutes les résistances de charge des éléments actifs étant constituées par des générateurs de courant ceux-ci ont besoin d'une source de référence. Elle est constituée par la diode zener Y1 et le pont 500Ω, Q_2, 15kΩ. La diode zener Y_1 est alimentée à courant quasi-constant par le FET Q_1.

1.2. Régulateur (Fig. 3).

Le régulateur proprement dit comporte un amplificateur différentiel d'erreur (Q_{11} et Q_{12}) et un amplificateur de puissance Q14 suivi du ballast Q15. Les émetteurs de l'étage différentiel sont alimentés par la source de courant Q_{13} dont la tension de référence est fournie par Q_9 et Q_{10}.

Les deux électrodes (émetteur et collecteur) du ballast sont sorties, ce qui permet d'utiliser toute combinaison possible de ballasts extérieurs.

Le schéma simplifié du régulateur est représenté sur la figure 4.

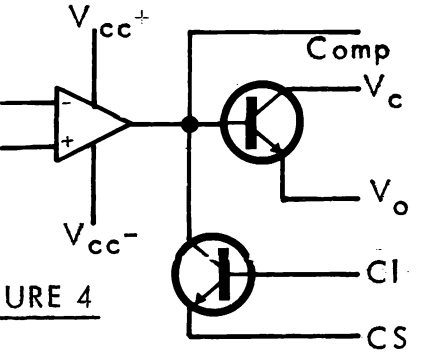


FIGURE 4

2. UTILISATION

Le régulateur SN 52/72 723 peut être utilisé seul à condition que la puissance dissipée ne dépasse pas les limites tolérées (Fig. 5) ou associé à des ballasts extérieurs, il peut être utilisé en régulateur positif ou négatif, haute ou basse tension, générateur de courant etc... comme le montrent les différentes applications ci-dessous.

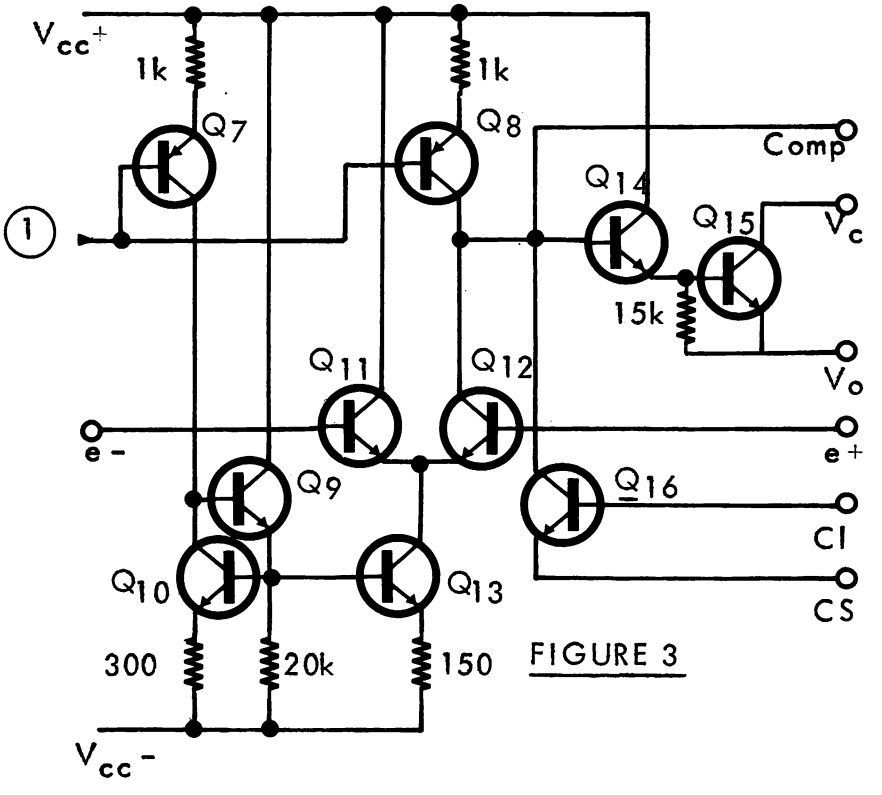


FIGURE 3

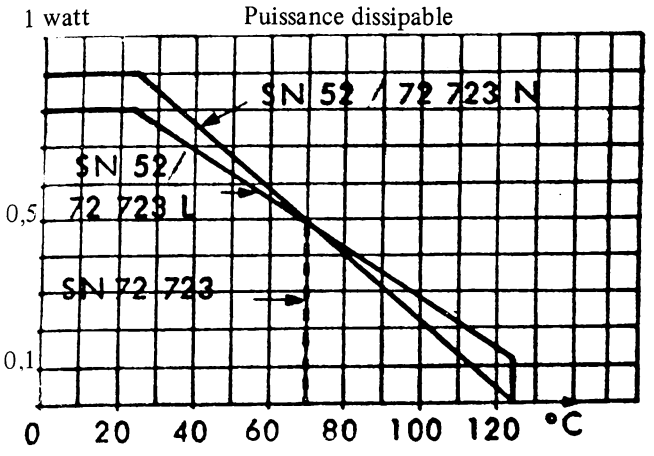


Figure 5

2.1. Tension de sortie inférieure à la tension de référence (Fig. 6)

L'amplificateur d'erreur est monté en suiveur, au gain unité et la tension de référence est ramenée à la valeur voulue (5V dans ce cas) par un pont diviseur qui alimente l'entrée non inverseuse. La tension minimale de l'entrée est de 2V. Il est préférable, pour un régulateur de ce type,

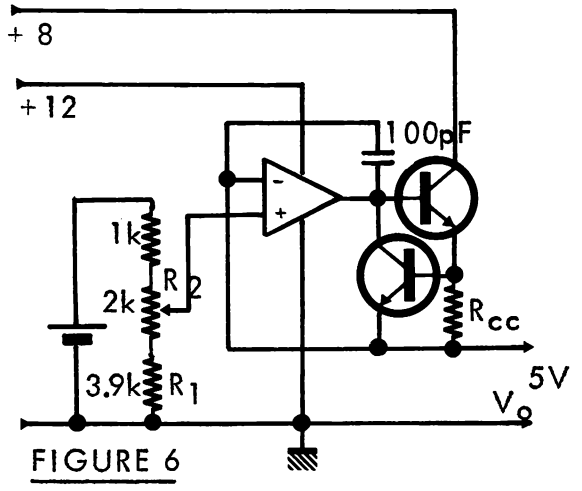


FIGURE 6

qui est destiné en général à alimenter des circuits logiques, d'alimenter le régulateur par une tension de 12V plus ou moins stabilisée et le ballast par une tension inférieure (8V par exemple) pour diminuer la puissance dissipée dans le régulateur. Par exemple, d'après la courbe de la figure 5 et, pour une utilisation avec une température ambiante de 40°C Max. le régulateur SN 72 723 N peut dissiper 760 mW m W; la dissipation interne normale est de 40 m Wenviron, il reste donc 720 m W disponible pour le ballast. Sachant que la tension d'alimentation, qui est, nominalement, de 8V peut atteindre 9V et, qu'en court-circuit, il reste 0.6V env. aux bornes de R_{cc}; la chute de tension dans le ballast peut être de 8.4V ce qui, pour une puissance dissipée de 720 m W donne un courant maximal de sortie de 85 mA par contre, si l'on est certain qu'il n'y aura ni court-circuit, ni surcharge, on peut disposer de 150 mA qui est le courant maximal que peut débiter le régulateur.

$$V_o = V_Z \frac{R_1}{R_1 + R_2}$$

2.2. Tension de sortie supérieure à la tension de référence

Dans ce cas, la tension de référence est branchée directement sur l'entrée + et la tension de sortie est ajustée par le pont de résistances. Les mêmes considérations de puissance et de courant de sortie que celles du montage précédent doivent être appliquées.

$$V_o = V_Z \left(1 + \frac{R_2}{R_1}\right)$$

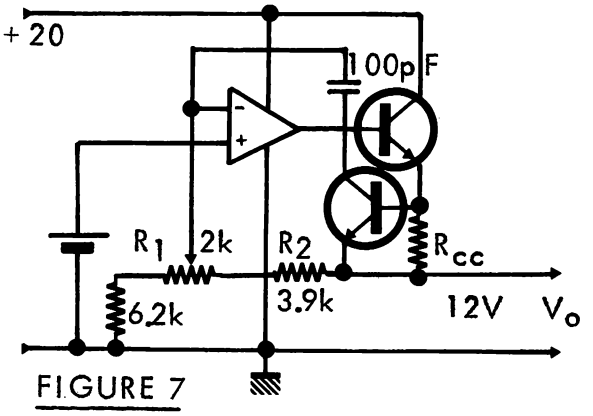


FIGURE 7

2.3. Adjonction de ballasts extérieurs

Quand le courant de sortie ou la puissance dissipée dépassent les limites admissibles, on peut adjoindre des transistors extérieurs, quitte à les monter sur radiateur, pour obtenir une puissance de sortie plus élevée.

a) Ballast PNP

Quand on utilise un ballast PNP, celui-ci doit être monté en amplificateur à contre-réaction totale (quelquefois appelé "Super Darlington") comme le montre le schéma de la figure 8.

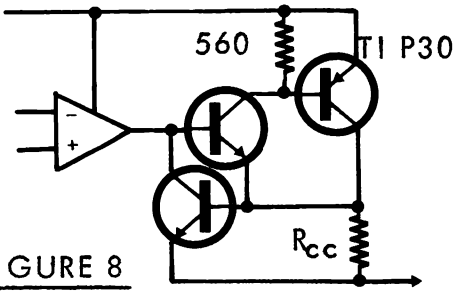


FIGURE 8

b) Ballast NPN

Si on utilise un ballast NPN, celui-ci doit être monté en Darlington avec le ballast intérieur. Mais la régulation risque d'être moins bonne qu'avec le montage précédent puisque l'amplificateur d'erreur doit rattraper les deux V_{be} des transistors de sortie, dont celui du dernier transistor, qui peut varier de près de 400 mV dans les cas extrêmes.

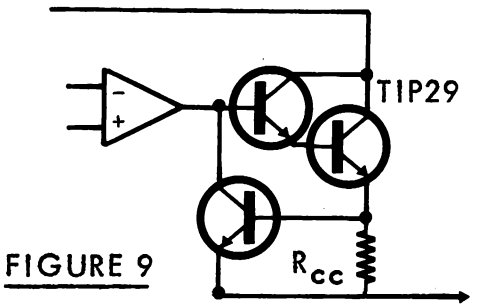


FIGURE 9

c) Ballast combiné PNP-NPN

Dans les cas des figures 8 et 9 ont peut atteindre des courants de sortie de l'ordre de l'ampère; si on veut des courants plus importants, on peut combiner les deux montages et arriver à celui de la figure 10 qui, lui, peut fournir un courant de 10A.

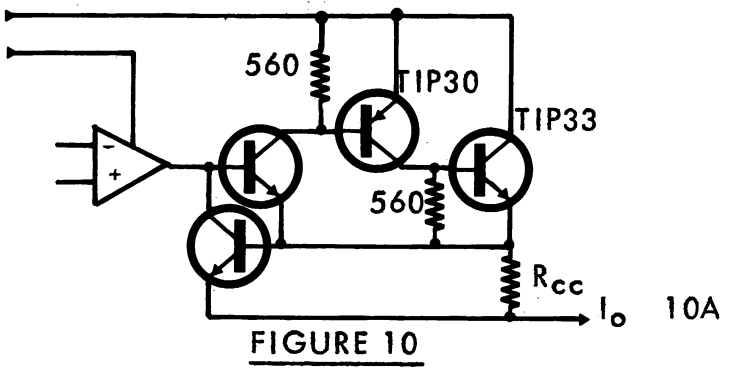


FIGURE 10

2.4. Régulateur de tension négative (Régulateur série)

On peut utiliser le régulateur SN 52/72 723 pour réguler des tensions négatives par rapport à la masse à condition de lui adjoindre un ballast extérieur. La tension de référence étant alors accrochée à la tension régulée et non à la masse, les entrées de l'amplificateur d'erreur doivent être inversées.

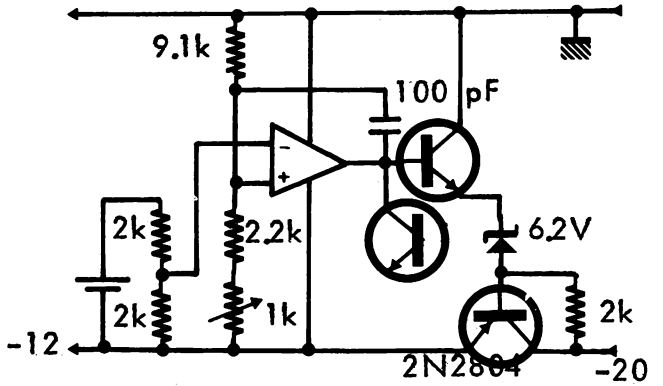


FIGURE 11

L'entrée - est réunie à la tension de référence, divisée par deux de façon à assurer un fonctionnement correct de l'amplificateur d'erreur, alors que la tension de sortie (qui est l'alimentation du régulateur) est mesurée par le pont 9.1k - 2.2k - 1k et injectée sur l'entrée +. Le démarrage du régulateur est assuré normalement par la résistance de 2kΩ entre base et collecteur du ballast. Dès que la tension de sortie est atteinte, le courant de base est modulé par le régulateur à travers une diode zener de 6.2V (cette diode est incorporée dans le SN 52/72 723 N mais non dans le L qui ne dispose pas d'assez de broches) de façon à maintenir la tension de sortie constante.

2.5. Régulateur de tension négative (Régulateur Shunt)

Bien souvent, les régulateurs négatifs sont des régulateurs de faible puissance; ils ne servent qu'à fournir la tension V_{cc} - à des amplificateurs opérationnels et on peut alors utiliser le montage shunt de la figure 12. Ici, le ballast est constitué d'une résistance RB et le régulateur ne fait qu'absorber le surcroît de courant qui est nécessaire pour maintenir la tension de sortie à la valeur voulue. Avec la diode interne du SN 52/72 723 N on peut atteindre un courant de régulation de 25 mA; ce courant correspondant aux fluctuations dues aux variations de charge ou de tension d'entrée.

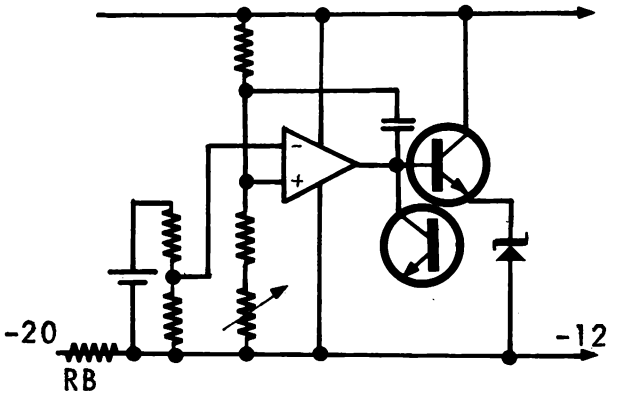
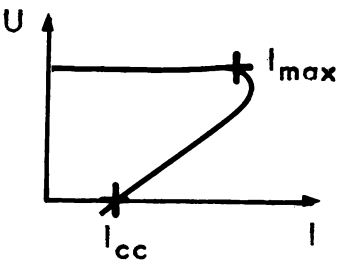


FIGURE 12

2.6. Protection par limitation de puissance (Fig. 13)

Ce type de protection contre les court-circuits dit Fold Back en anglais à l'avantage de limiter la puissance dissipée dans le régulateur en cas de court-circuit; le courant de sortie diminuant au fur et à mesure que la tension de sortie descend suivant une courbe identique à celle ci-contre. Les deux points clés qui sont I_{max} et I_{cc}



sont données par les formules ci-dessous. Elles ne sont pas rigoureuses du fait que la tension V_{be} du transistor de limitation peut varier de 0.55 à 0.65V; une valeur moyenne de 0.6V a été choisie :

$$I_{max} = \left(\frac{V_o}{R_{cc}} \cdot \frac{R_1}{R_2}\right) + I_{cc}$$

$$I_{cc} = \frac{0.6}{R_{cc}} \quad (1 + \frac{R_1}{R_2})$$

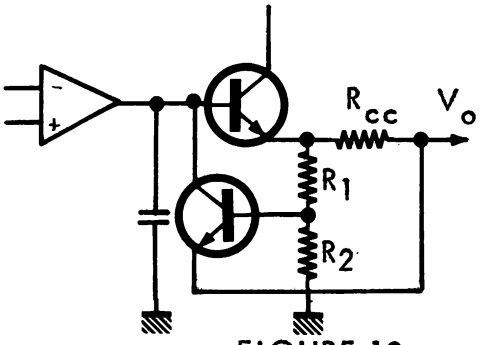


FIGURE 13

2.7. Masse synthétique (Fig. 14)

Pour diverses raisons d'ordre pratique (puissance dissipée, coefficient de température, limitation de courant etc...) on a avantage à utiliser une seule alimentation et à la couper ensuite en deux, plutôt que deux alimentations distinctes quand il s'agit d'un ensemble analogique avec amplificateurs opérationnels; si par exemple ceux-ci doivent être alimentés par + et - 12V on peut faire une seule alimentation 24V, la division en deux par un pont à faible résistance interne et utiliser ce pont milieu comme masse; malheureusement, deux résistances ne constituent pas une source d'assez faible impédance pour réaliser une bonne masse. On peut alors utiliser l'amplificateur d'erreur d'un SN 52/72 723 de façon à rendre presque nulle l'impédance présentée par le pont diviseur. Si le courant dans le point milieu est faible, on peut utiliser, comme masse la sortie du régulateur avec une résistance ballast vers le V_{cc}- si non, il vaut mieux utiliser deux transistors comme sur la figure 14.

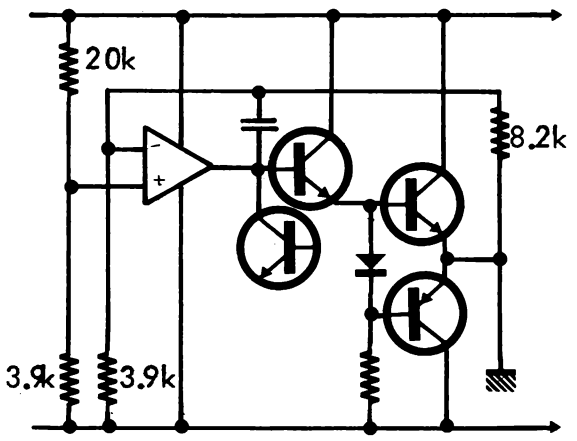


FIGURE 14

2.8. Régulateur positif haute tension (Fig. 15)

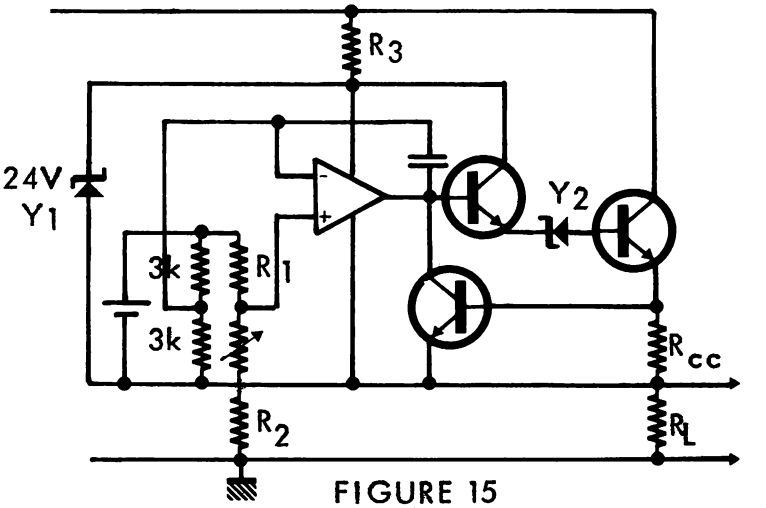


FIGURE 15

Ce régulateur est prévu pour fournir des tensions de sortie supérieures à la valeur maximale admissible de la tension d'alimentation du régulateur SN 52/72 723. Le circuit intégré est monté flottant entre la tension d'entrée et la tension de sortie, il est alimenté sous 24V par R_3 et Y_1 ce qui fait qu'il demande d'être utilisé avec une résistance maximale ou bleeder (R_L) de façon à ce que, même à vide, le courant d'alimentation du régulateur et celui de la zener puissent s'évacuer vers la masse. On doit donc avoir

$$R_{L(k\Omega)} \quad \frac{e_o}{I_{Z(mA)} + 3.5}$$

Le ballast doit, obligatoirement, être extérieur puisqu'il doit pouvoir supporter la totalité de la tension d'alimentation en cas de court-circuit.

La valeur de la tension de sortie est donnée par

$$3.6\,(1 + \frac{R_2}{R_1}) \quad \text{à } \pm 3\%$$

2.9. Régulateur négatif haute tension (Fig. 16)

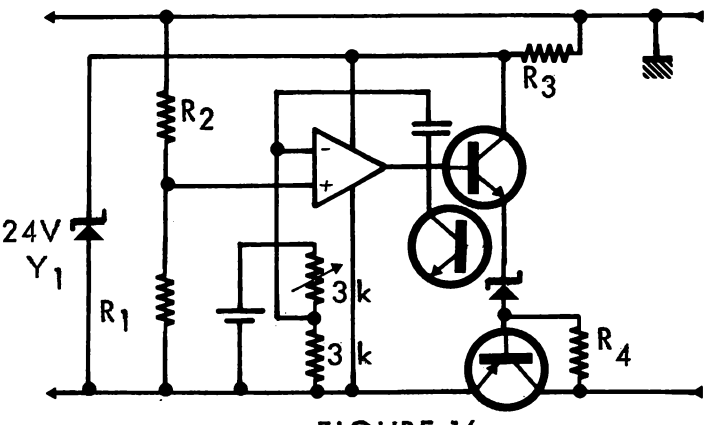


FIGURE 16

Ce régulateur est la transposition, en version haute-tension de celui du paragraphe 2.4. Le circuit est alimenté, sous 24 V, par R_3 et Y_1 et le ballast est un transistor PNP et son fonctionnement est exactement semblable à celui de la figure 11.

2.10. Régulateur de courant (Fig. 17)

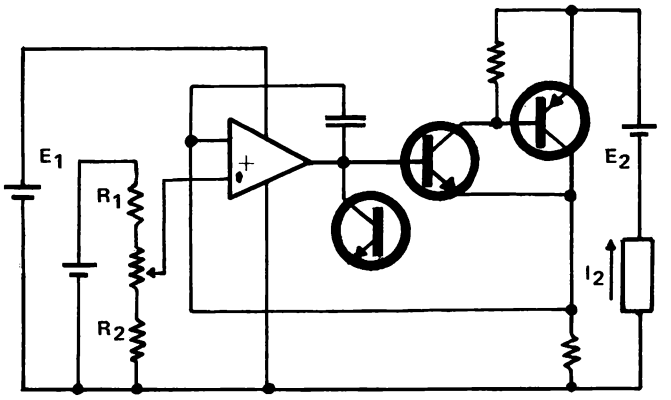


Figure 17.

Ce régulateur de courant demande deux sources d'alimentation : E_1 qui doit fournir de 10 à 30 V pour l'alimentation du régulateur et e_2 qui alimente le circuit de puissance. Ces deux sources peuvent être communes si le courant d'alimentation du régulateur est négligeable devant le courant d'utilisation.

Le courant dans la charge I_L est maintenu constant par le simple fait que la tension aux bornes de la résistance de mesure R_m est maintenue égale à celle qui est présente sur le pont diviseur R_1 R_2.

Suivant la nature du ballast extérieur utilisé, des courants de quelques milliampères, à quelques milliers d'ampères peuvent être aisément contrôlé.

2.11. Régulateur à commutation :

L'utilisation du SN 72723 permet de réaliser, avec un petit nombre de composants additionnels, des alimentations à commutation offrant l'avantage sur les alimentations séries d'avoir un excellent rendement, donc un encombrement réduit par suppression des dissipateurs.

Le principe d'une alimentation à commutation est simple (fig. 18) : lorsque l'interrupteur, constitué par le transistor Q, se forme, le courant croît linéairement dans la self L suivant la relation : $V_E - V_S = \frac{di}{dt}$; un courant traverse la charge et charge la capacité C. Quand le transistor Q est bloqué, le courant décroît dans la self L, le circuit se refermant alors par la diode D. Quand le courant dans la self devient inférieur au courant dans la charge, la capacité commence à se décharger, puis Q se ferme et le cycle recommence.

En négligeant les chutes de tension aux bornes du transistor Q et de la diode D, on aura $V_S = V_E \frac{\text{temps de conduction}}{\text{}}$ et ce, quelque soit le courant traversant la charge.

Une modification de la tension d'entrée ou du courant dans la charge se traduira, soit par une modification du rapport cyclique, soit par une modification de la fréquence de fonctionnement.

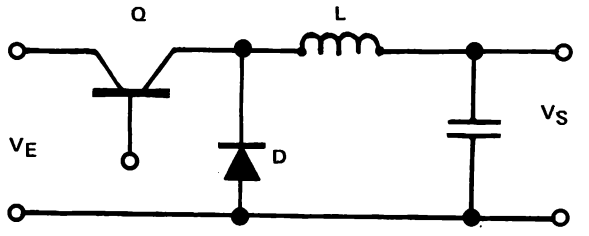


Fig. 18. Alimentation en Commutation Principe

Une telle alimentation est réalisée facilement en utilisant le circuit SN 72723.

A l'entrée non inverseuse de l'amplificateur commandant le transistor ballast interne est appliquée la tension de référence V Ref interne du SN 72723 à laquelle est ajoutée une faible réaction positive, déterminée par le rapport des résistances R_1 et R_2 et la tension d'entrée VE.

Une fraction de la tension de sortie est ramenée sur l'entrée inverseuse, cette fraction étant déterminée par le rapport des résistances R_4 et $R_5 + PR_6$.

Si nous supposons que $R_1 \gg R_2$, la tension à l'entrée non inverseuse l'amplificateur d'erreur est donnée approximativement par : $V_{Ref} + \frac{R2}{R1} \times V_E$.

Nous appellerons $V_H = \frac{R2}{R1} \times V_E$ la tension égale à l'hystérésis apportée à l'amplificateur d'erreur par la réaction positive.

A la mise en route, la tension de sortie est inférieure à la tension $V_{Ref} + V_H$, le transistor ballast interne conduit et le transistor externe est saturé; le courant circule à travers la self et dans la charge; lorsque la tension de sortie dépasse $V_{Ref} + V_H$, l'amplificateur d'erreur bloque le transistor ballast interne et le courant commence à décroître dans la self L, la diode D est polarisée en direct.

Lorsque le courant dans la self L descend en dessous du courant dans la charge, la capacité C commence à se décharger et la tension de sortie diminue jusqu'à ce que la fraction de cette tension ramenée à l'entrée inverseuse soit inférieure à la tension de référence V_{Ref}; alors l'amplificateur d'erreur bascule et vient faire conduire le ballast interne qui sature Q et le cycle recommence.

La tension de sortie V_S oscille donc autour de la valeur choisie d'une amplitude voisine de $V_H = \frac{R1}{R2} \times V_E$, à la fréquence de commutation du transistor Q.

L'ondulation résiduelle sera de l'ordre de grandeur de V_H; la capacité C en parallèle sur $R_4 + PR_6$ réduit cette ondulation en la réinjectant à l'entrée de l'amplificateur.

La valeur de la self déterminera le courant crête qui traversera le transistor ballast externe et la diode D en fonction du courant consommé en sortie; des équations de courants, on tire :

$$L = \frac{V_S - V_E}{2\,(I_{max} - I_s)} \times \frac{V_S}{V_E} \times \frac{1}{f}$$

La valeur du condensateur de sortie est fonction de l'ondulation résiduelle tolérée en sortie, de la fréquence de fonctionnement et des tensions d'entrée et de sortie :

$$C = \frac{V_S}{V_E} \times \frac{(V_E - V_S)}{8L\ f^2\ (\Delta V_S - V_H)}$$

Ces équations ne se veulent pas rigoureuses; elles peuvent cependant être un outil de calcul utile pour dégrossir le problème dans le cas où on voudrait réaliser une alimentation à commutation utilisant un amplificateur d'erreur en autooscillateur.

Les valeurs réelles utilisées après expérimentation sont :

$L = 2$ mH; $V_H = 25$ mV; $C = 50\ \mu$F.

L'alimentation réalisée à titre d'exemple (fig. 19) avec le SN 72723 ayant les caractéristiques suivantes :

16 volts / 1,2 A
ΔV_S < 50 mV
f > 20 kHz
V_E > 25 volts
protégée contre les court-circuits

a donné les calculs suivants :

$L_{min} = 1{,}5$ mH; $V_H = 25$ mV; $C = 100\ \mu$F.

La limitation en courant utilise le transistor interne du SN 72723; la tension nécessaire pour le débloquer est donnée d'une part par la chute de tension aux bornes de R & C, d'autre part par la tension ramenée sur l'émetteur par l'intermédiaire du pont R7, R8, ce qui permet de ne protéger le transistor extérieur que lorsqu'il vient en saturation, donc de permettre à l'oscillation de se poursuivre même sous conditions de court-circuit et de diminuer alors probablement la puissance dissipée, tout en fournissant un signal sonore, la fréquence d'oscillation descendant à des fréquences audibles.

$$I_{Lim} = \frac{V_{BE}}{R_{SC}} + \frac{R_8}{R_7 + R_8} \quad \frac{(V_E - V_S)}{R_{SC}}$$

Le rendement de l'alimentation donné sur le schéma dépasse 80%.

Les pertes par commutation sont faibles, le temps de commutation du ballast de sortie environ 1 μs restant court devant le temps de saturation.

L'utilisation de diodes à recouvrement rapide 1 N 3880 diminue les pertes lors de la mise en conduction du transistor; le courant produit par les charges stockées restant faible.

Les pertes par conduction du transistor approximativement :

$$P_{ST} = V_{CESAT} \cdot I_S \cdot \frac{V_S}{V_E}$$

et, par conduction de la diode, approximativement :

$$P_{SD} = V_{FD} \cdot I_S \cdot \frac{V_E - V_S}{V_E}$$

représentant une part importante de la puissance perdue, tout en étant faibles devant la puissance de sortie.

Les alimentations à commutation à très bon rendement sont réalisées avec un petit nombre de composants, grâce à l'utilisation du SN 72723. Les principes de fonctionnement, assez simples, ont été exposés ici et les équations données permettront de réaliser rapidement de telles alimentations.

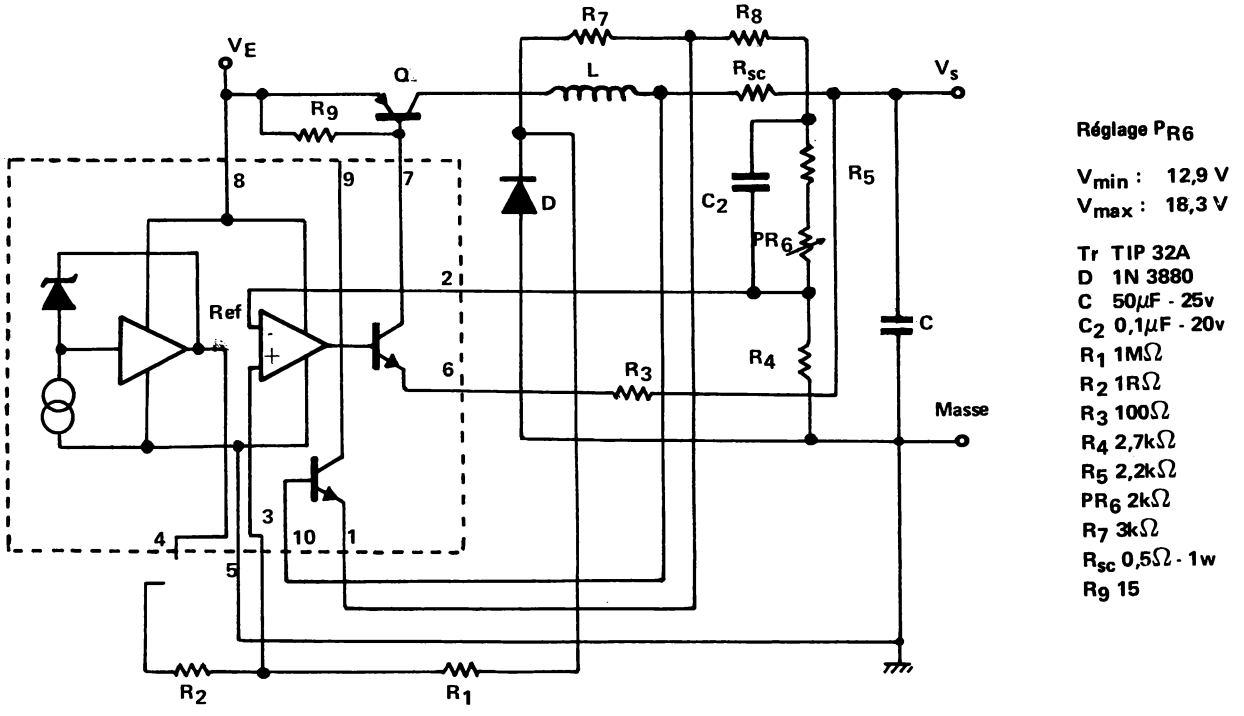


Figure 19. Alimentation 13 - 18 V; 1,2 A

Monochrome TV switching regulator and line driver

(B 114)

MONOCHROME TV SWITCHING REGULATOR AND LINE DRIVER

By Kuldip Rupra

INTRODUCTION

The 135V – 150V regulated supply required for a BU105 line output stage can be obtained by a number of methods. The concept described here offers considerable advantages over other available regulators, especially where low TV set power dissipation is a prime consideration.

The regulated voltage is achieved by using the series switching technique where the mark space ratio of the switching transistor is varied in sympathy with the output voltage change caused by either mains voltage fluctuation (± 10%) or load variations. The principle of such a regulator is explained in greater detail in Application Report B76. For a regulator output of 145V, say, and a period (τ) of 64μs (i.e. frequency of operation 15kHz), the conduction period (t_{on}) of the series switch under normal mains condition is 32μs. The absolute limits of t_{on} are 28μs with low mains (–10%) and 38μs with maximum mains (+ 10%). Both these figures are within the permissible drive pulse width tolerance for a BU105 line output stage, and therefore this design uses the low pass filter coil also as the voltage step-down transformer (e.g. 30 : 1) which provides the base current for the BU105. The fact that there is a 50Hz width modulation (1 – 3μs) on the BU105 drive pulses should not worry the line synchronisation section. This will be explained later.

A further advantage of this concept is that any number of auxiliaries low tension supplies may be obtained by additional windings on the filter choke.

The circuit is protected against the 145V rail being shorted to earth and also the series switch failing, i.e. collector-emitter short circuit.

CIRCUIT DESCRIPTION

General

Figure 1 shows, in block diagram form, the principle of a switching mode power supply. The series transistor switch is operated at the fixed oscillator frequency. Its mark space ratio is determined by the variable mark space generator which is in turn controlled by a D.C. level fed to it. This level is the amplifier error signal obtained by comparting the output from the supply with a D.C. reference voltage.

The complete switching regulator and line driver circuit is shown in Figure 2.

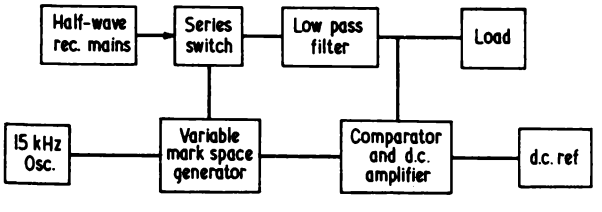


FIGURE 1 SWITCHING MODE POWER SUPPLY

Series Switch (a BD410 transistor) operation

Half wave rectified mains is fed to the collector of the switching transistor VT4. An important point about this regulator design is the use of a BD410 in this position. As the device is in a SOT32 package it provides a considerable price saving over any device in a TO3 package. Its main parameter requirements are :–

1. BV_{CER} > 400V
2. Reasonably fast switching
3. Good saturation characteristics at I_C = 600mA.

As can be seen from the device data sheet, the breakdown voltages required for this application are well within the device's capabilities.

The transistor must switch reasonably fast since the majority of the power dissipation occurs during the switching excursion. Photographs 1 and 2 show the switching speeds of a typical device. Both switch "on" and switch "off" are less than 1μs. (Typically t_{on}=400ns t_{off}=500ns). This means that dissipation in the device during these transient conditions is less than 3W.

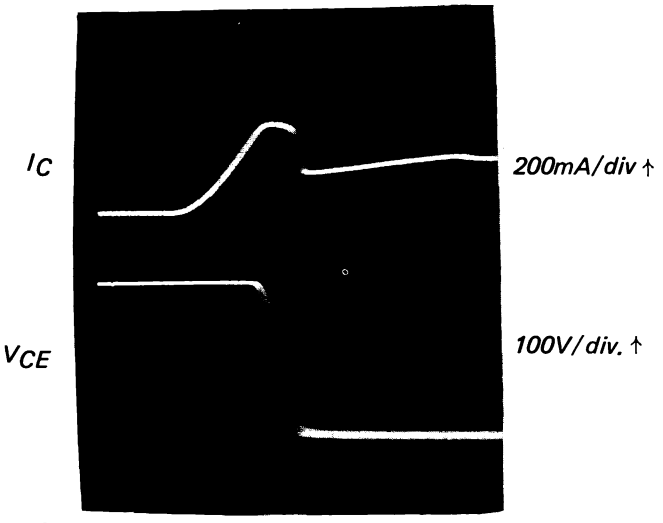


PHOTO. 1 SWITCH ON 500ns/div. →

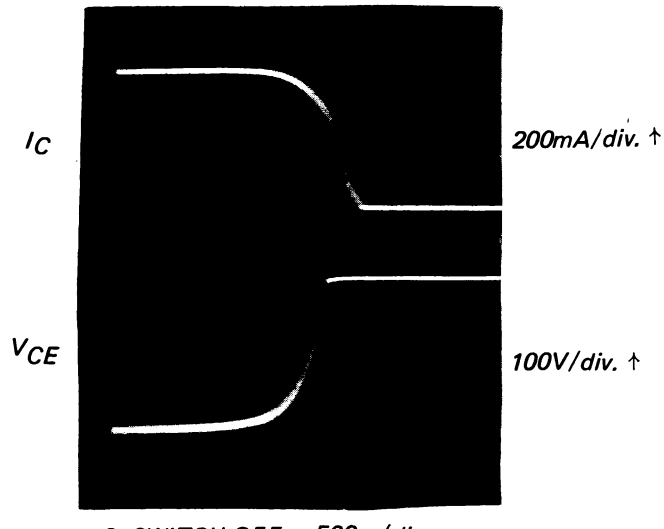


PHOTO. 2 SWITCH OFF 500ns/div. →

MONOCHROME TV SWITCHING REGULATOR AND LINE DRIVER

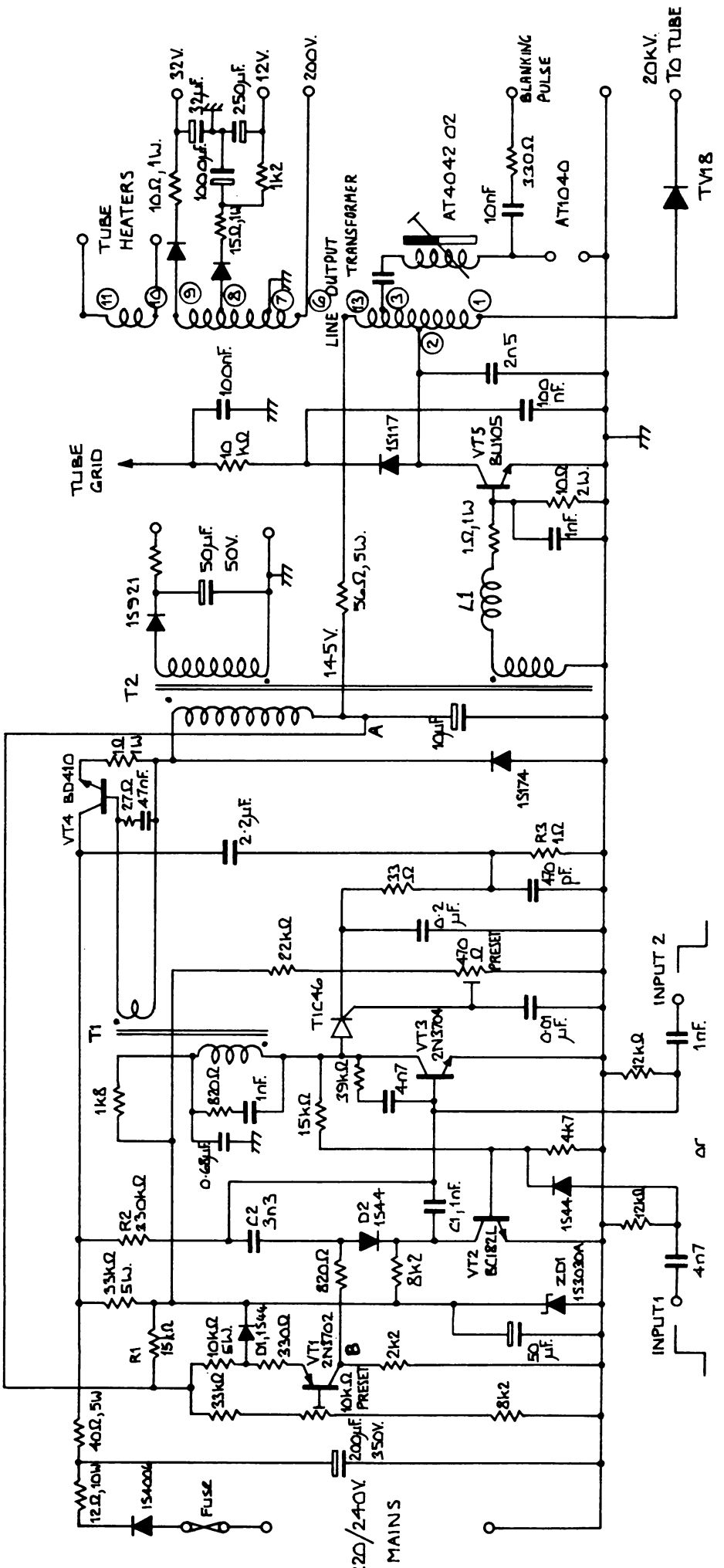


FIGURE 2

The saturation characteristic of the device needs to be sufficiently good to avoid excessive dissipation, i.e. $V_{CE(sat)}$ must not be more than 10V with collector current of 600mA. From photograph 3 it can be deduced that the base drive required to maintain this condition is 125mA. Extensive measurements show, however, that for such applications this value of base current required may be reduced by 30% to 75mA to maintain $V_{CE(sat)}$ of 10V at 600mA under the dynamic condition.

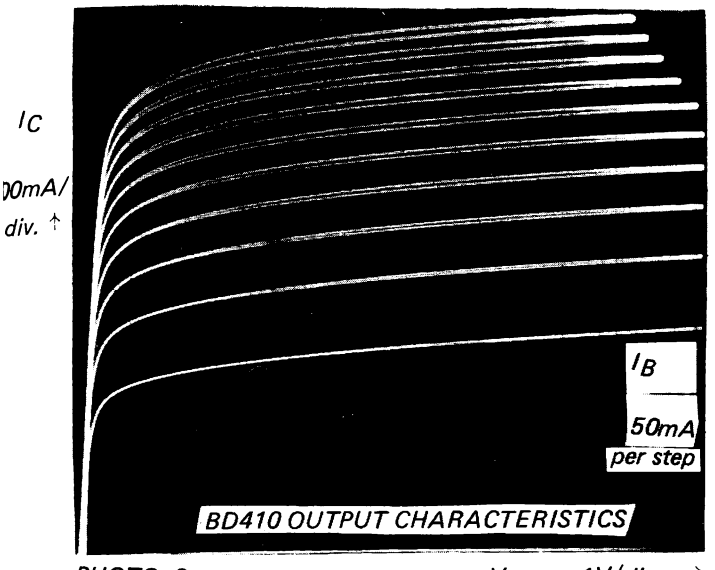


PHOTO. 3 V_{CE} 1V/div. →

Line Oscillator

The oscillator is provided externally to the regulator circuit shown in Figure 2, and provides a pulse to be fed to the input point. The trigger pulse required by the variable mark space generator from the line oscillator must have a fast triggering edge. A positive trigger pulse, which would be fed to Input 1, must have a width greater than 4μs. If a negative going trigger, fed to Input 2, is used, its pulse width should not be less than 4μs or greater than 10μs. This helps to limit the maximum pulse width out of the monostable to 54μs which, under low mains and overload condition, avoids monostable operation at half the required frequency. The trigger pulse amplitude can be between 4V and 10V, and may be of fairly high source impedance.

In the worst case, low mains and maximum loading, the base drive pulse width to the BU105 would be changing by about 4μs. In a normal, flywheel synchronising system, the flyback voltage pulse is referred to the line oscillator. If the response time of the system is faster than 50Hz, which it normally is, the slight 50Hz modulation occuring on the leading edge of the BU105 base drive pulse is allowed for, so that picture displacement does not occur.

Since the control circuitry for this switching regulator needs line oscillator pulses to drive it, it is essential that the oscillator starts up rapidly and that it is frequency stable from low voltages to the ultimate regulated rail voltage. Also too much current must not be consumed since its supply has to be dropped from the 300V line.

There are various ways in which the line oscillator function can be performed. One of them is to use a SN 76533 "Jungle" Integrated Circuit to act as the line oscillator and phase comparator. The circuit arrangement for this is given in the Appendix.

The "Jungle" has an internal zener diode supply for the line oscillator, which is frequency stable to within 10% during switch on and switch off.

With this system, the synchronisation pulses are at always a predetermined separation from the leading edge of the output pulse of the SN76533, determined largely by the storage time of the BU105 and, to some extent, the delay caused by the driver switching "on".

The waveforms shown in photographs 4, to 8 are taken with a fifth harmonic tuned line output stage and the oscilloscope triggered by the leading edge of output pulse from the SN76533. The relationship of the sync. pulse to the collector current turn "off" (or initiation of flyback voltage) is shown by comparing photographs 4 (top trace) and 8 (bottom trace).

Monostable and Driver

A cheap, effective, simple monostable circuit is employed to perform the pulse width modulation for regulation purposes. The stable element (transistor VT3) of the monostable is also used as the driver stage. This driver has a current step-up transformer (T1) as its load, providing sufficient base drive for the BD410 series switching device. Transistor VT2 is normally "off" except when a positive going signal is applied to its base. Alternatively, applying a negative going signal to the base of transistor VT3 to switch it "off" will in turn switch transistor VT2 "on" through the resistor network from transistor VT3's collector. Monostable action starts from this point.

The transformer in the collector of transistor VT3 is so arranged that the BD410 is "on" during the period the driver VT3 is "off", i.e. the "on" time of VT2. In practice, however,

the BD410–t_{on} = VT2–t_{on} + a delay due to transformer leakage inductance.

It is important that, during supply switch on, the t_{on} of the BD410 is very small so that large currents through this device (even though occurring for only a few cycles) are avoided. This will also ensure a gradual build up of the output voltage which gives added stability to the system.

This narrow pulse width during "start up" is achieved by ensuring that the timing network consists of only resistor R2 and capacitor C1. This in fact is so, since as the output voltage (point A) is zero, the collector of the comparator is also zero and thus the diode D2 is reverse biassed during the timing period, effectively isolating capacitor C2 from the timing network. Waveforms applicable to this section of the circuit are shown in photographs 4 and 5.

PHOTO. 4

Video input — 2V/div.↑

Line Oscillator Voltage (Input to Monostable) — 2V/div.↑

PHOTO.5

V_{CE} VT3 — 5V/div.↑

I_B BD410 VT4 — 100mA/div.↑

PHOTO. 6

I_C BD410 VT4 — 200mA/div.↑

V_{R3} — 200mV/div.↑

PHOTO. 7

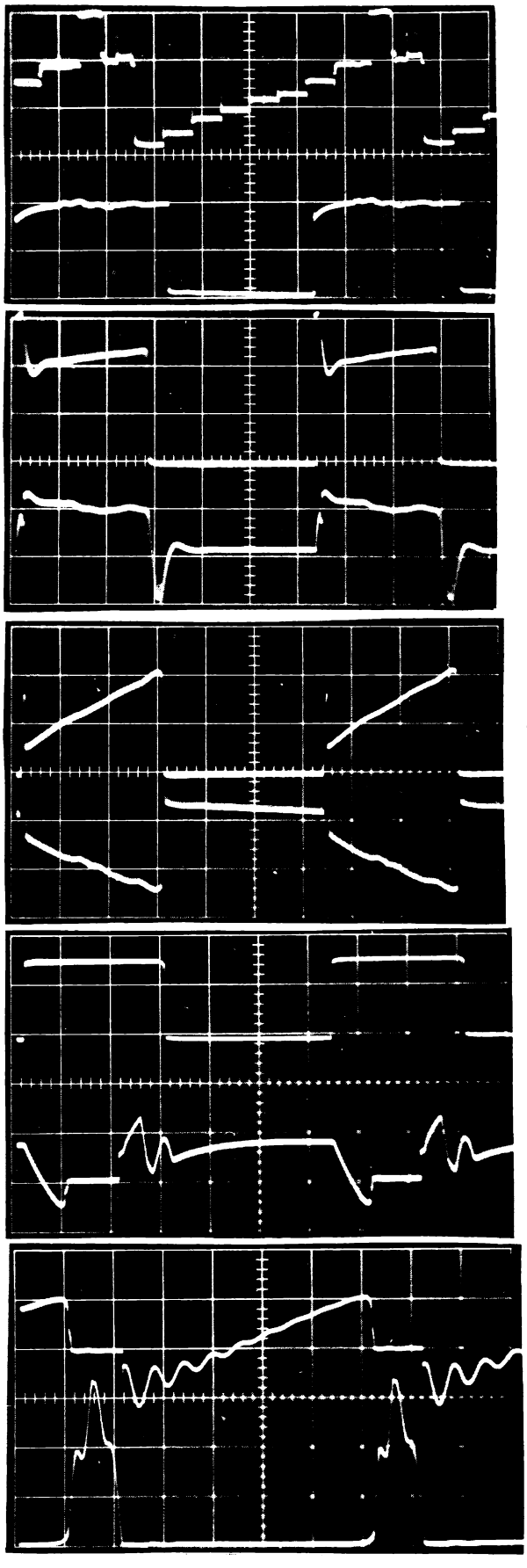
V_{CE} BD410 VT4 — 200V/div.↑

I_B VT5 (BU105) — 1A/div.↑

PHOTO. 8

I_C BU105 VT5 — 2A/div.↑

V_{CE} BU105 VT5 — 400V/div.↑



10μs/div.→

PHOTOGRAPHS OF WAVEFORMS DURING NORMAL OPERATION

Comparator

The minimum pulse width from the monostable results in the voltage developed at point A

$$V_{out(A)} = V_S . t_{on}/\tau$$
$$= 320.4/64$$
$$= 20V$$

where V_S= voltage at the collector of BD410

t_{on} ⇔ 4μs

τ = 64μs

Increasing the voltage at point A increases the voltage at the collector of the comparator transistor VT1, which in turn adds to the t_{on}. The resulting output voltage rise causing a further increase in voltage at point B, and so on. This progressive increase of pulse width t_{on}, and V_{out}, continues until the required V_{out} is reached. Here the comparator transistor changes its mode of operation into a high gain error amplifier as explained in Report B76. The zener diode ZD1, which during the "start up" condition is starved of current, experiences a progressive increase in current through it from the resistor R1 (15k) and the 10kΩ resistor and diode D1, ensuring a stable reference voltage across it. The V_{out} can be varied by a variable resistor feeding the base of transistor VT1.

Dynamic Trip

In a power supply of this nature, it is essential that there is adequate protection against any current overload, i.e. if the BU105 went short circuit or in the event of a tube "flash-over".

The collector current through the BD410 is sensed by monitoring the voltage across the resistor R3, this being proportional to it. The waveforms are shown in Photograph 6.

A plastic S.C.R. (TIC46) is used as the dynamic trip. The voltage developed across resistor R3. is fed to the cathode of the TIC46 after the necessary integration of sharp edges. The gate of this device is pre-biassed so that at the desired overload condition value the S.C.R. gate trigger voltage is reached at the end of the BD410 conduction period, as shown in Figure 3. If, therefore, an overload occurs, the TIC46 is triggered before the end of BD410's normal conduction period, shortening the drive pulse to it during subsequent cycles. Since the BD410 collector current waveform has a triangular component, this trip technique is effective. While the S.C.R. is latched "on" transistor VT3, due to normal monostable action, will switch "on". This helps to reset the TIC46 by draining current from it to below the holding current level – thus switching it "off". The S.C.R. is then ready for the next cycle of the dynamic trip action. Waveforms illustrating the circuit operation during a BU105 short circuit are shown in Photographs 9, 10 and 11.

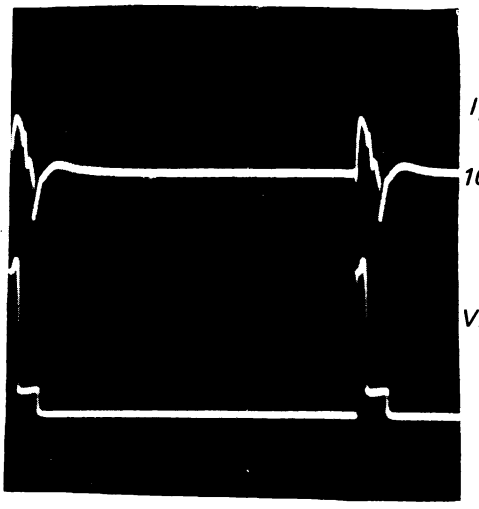


PHOTO. 9 *10μs/div.*

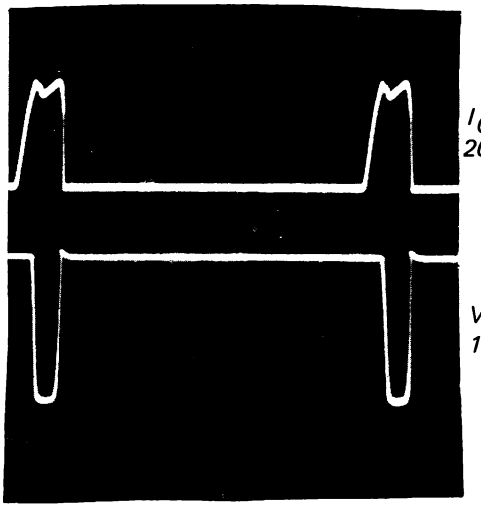
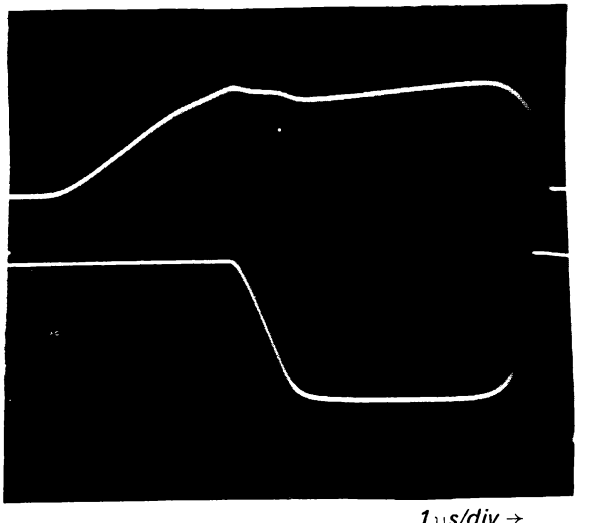


PHOTO. 10. *10μs/div*



1μs/div.

PHOTO.11 (10 EXPANDED)

WAVEFORMS OCCURING WHEN V_{out} IS SHORT CIRCUITED THROUGH 56 OHM

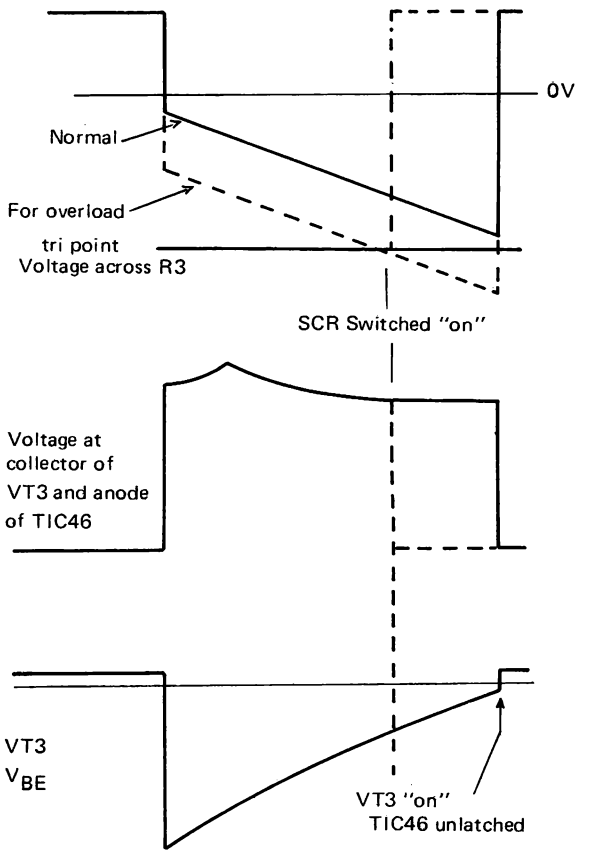


Figure 3.

An alternative trip circuit approach is to use two silect transistors rather than the SCR as shown in Figure 4. Costs are again kept low by using an NPN–PNP configuration.

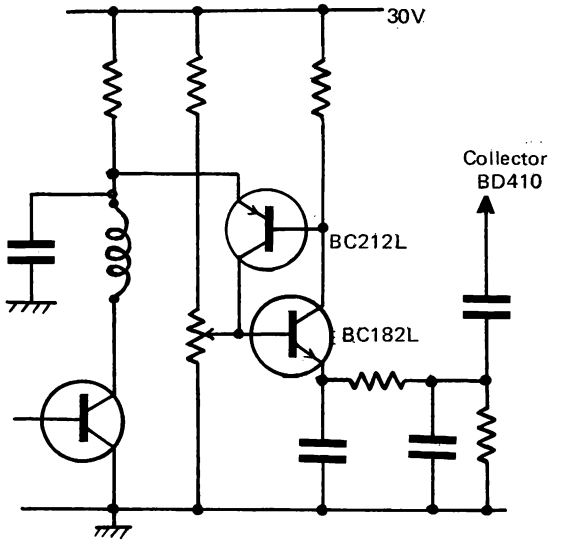


Figure 4

Line Output Stage

A turn-off delay of about 10μs has been introduced into the system, as illustrated in photograph 7, by putting a choke of 40μH (L1) in series with the base of the BU105. This ensures uniform extraction of excess stored charge from the device towards the end of its conduction period. To produce fast switch off times in very high voltage transistors, e.g. the BU105, the base current waveform must have the turn off delay referred to above and shown in photograph 7. If this is not present the clean and low dissipation BU105 collector current switch off, shown in photograph 8, would not occur.

RESULTS

Regulation achieved

ΔV_{out}	Full load to No load	= 2V
ΔV_{out}	Mains ± 20%	= 5V
15kHz ripple		= 1,5V
50Hz ripple		= 0.3V

TRANSFORMER DATA

BD410 Driver Transformer T1	Filter Choke and Transformer T2
Core = FX2238	Core = FX2241
N_p = 300 turns of 38 SWG	N_p = 400 turns of 34 SWG
N_s = 60 turns of 34 SWG	N_s = 80 turns of 28 SWG
Air Gap = 0.01 in.	N_{s2} = 8 turns of 26 SWG
	Air Gap = 0.1 in.

CONSTRUCTION

A printed circuit board layout is shown in Figure 6 and the component positions on this board illustrated in Figure 5.

CONCLUSIONS

The circuit concept described should be particularly useful for television manufacturers where maximum efficiency is of prime consideration. Simpler circuits available for deriving 135 – 150V supply rails have the disadvantage of approximately 80W power losses. Such losses cannot be tolerated in T.V.s which have a plastic cabinet and/or polythene back covers. This system with its low losses (≅ 20W) and hence low temperature rise is useful generally and ideal for sets employing thermoplastic cases, especially where they are intended for use in hot countries.

The circuit described could also be used to produce a regulated 150V 800mA supply. This would be suitable for 90° colour televisions using a single BU108 line output device. The series switch (VT4) in this case would have to have an appreciable gain at 1A collector current. This is beyond the capabilities of the BD410 and a R2010 would have to be used. Increases in loop gain and choke size would also be necessary for the higher power required.

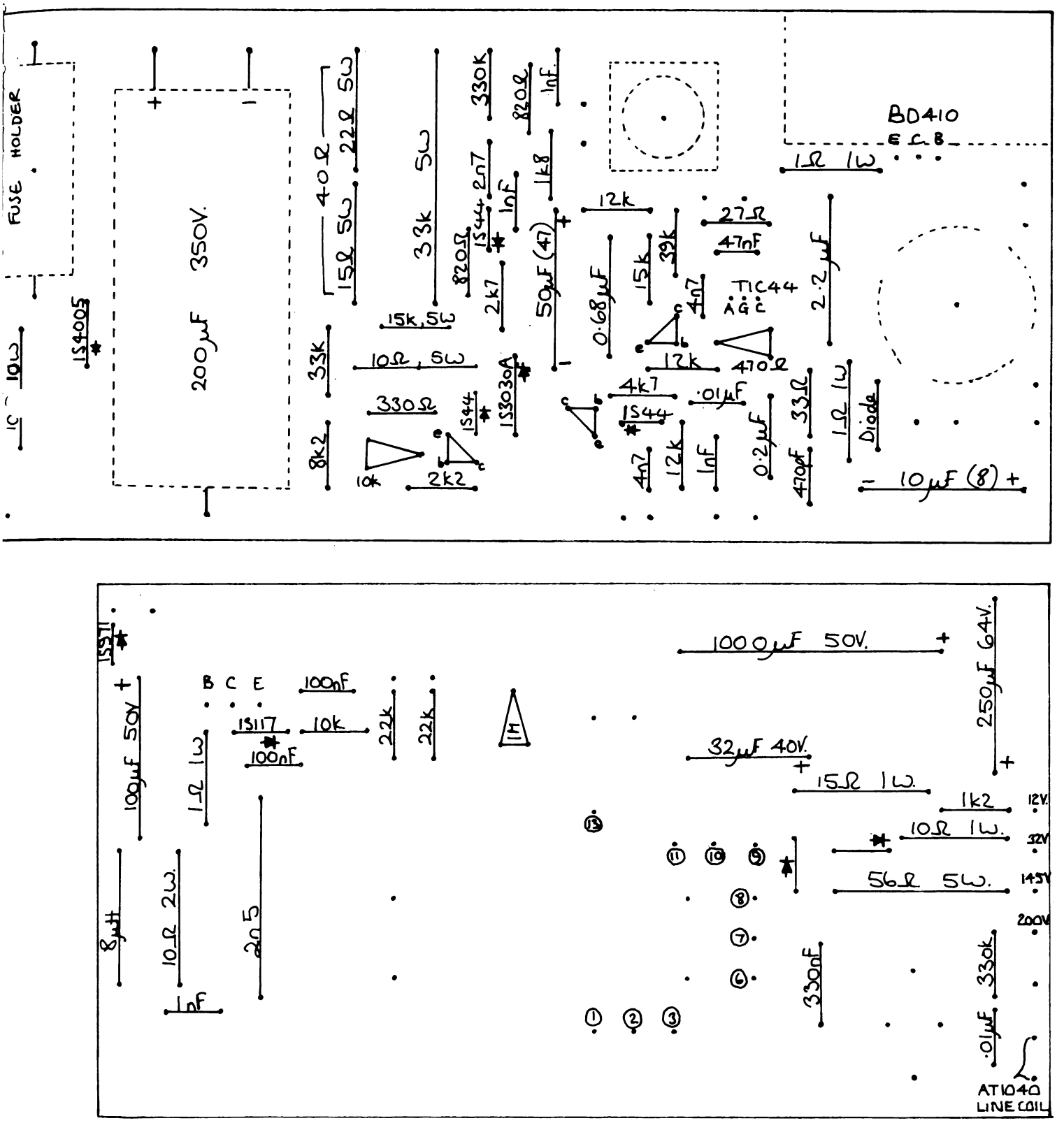
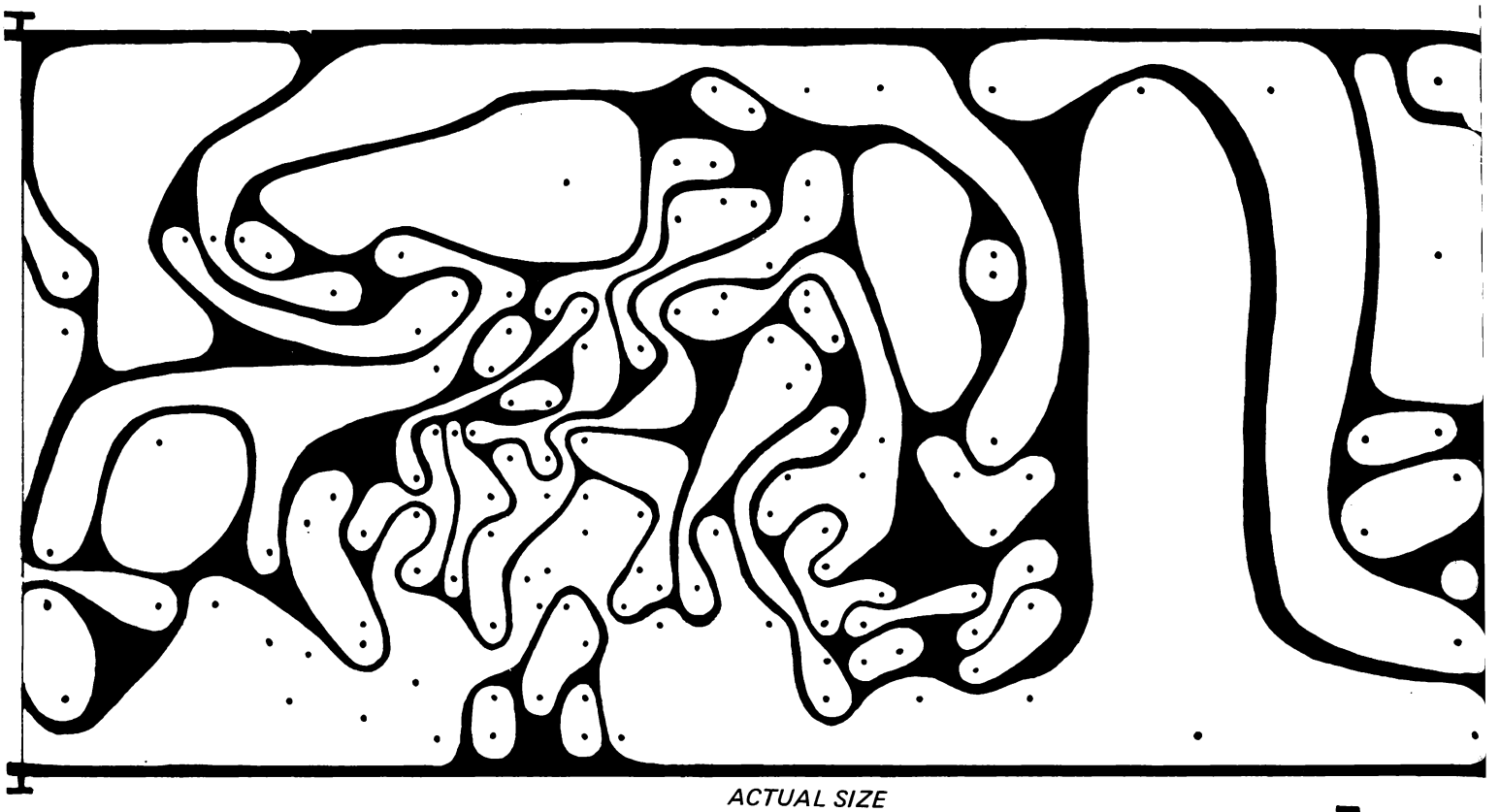


FIGURE 5 PRINTED CIRCUIT BOARD COMPONENT LAYOUT



ACTUAL SIZE

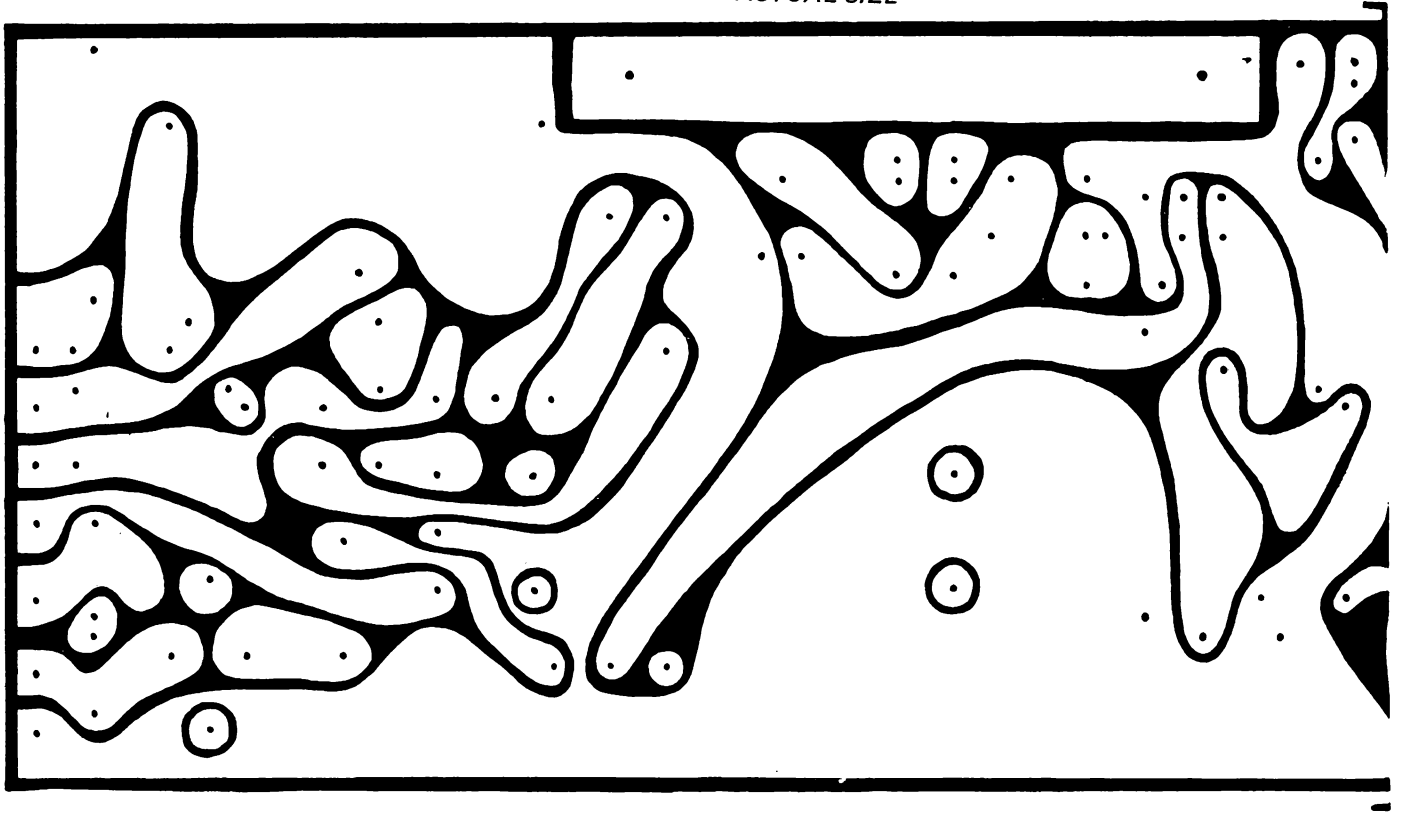
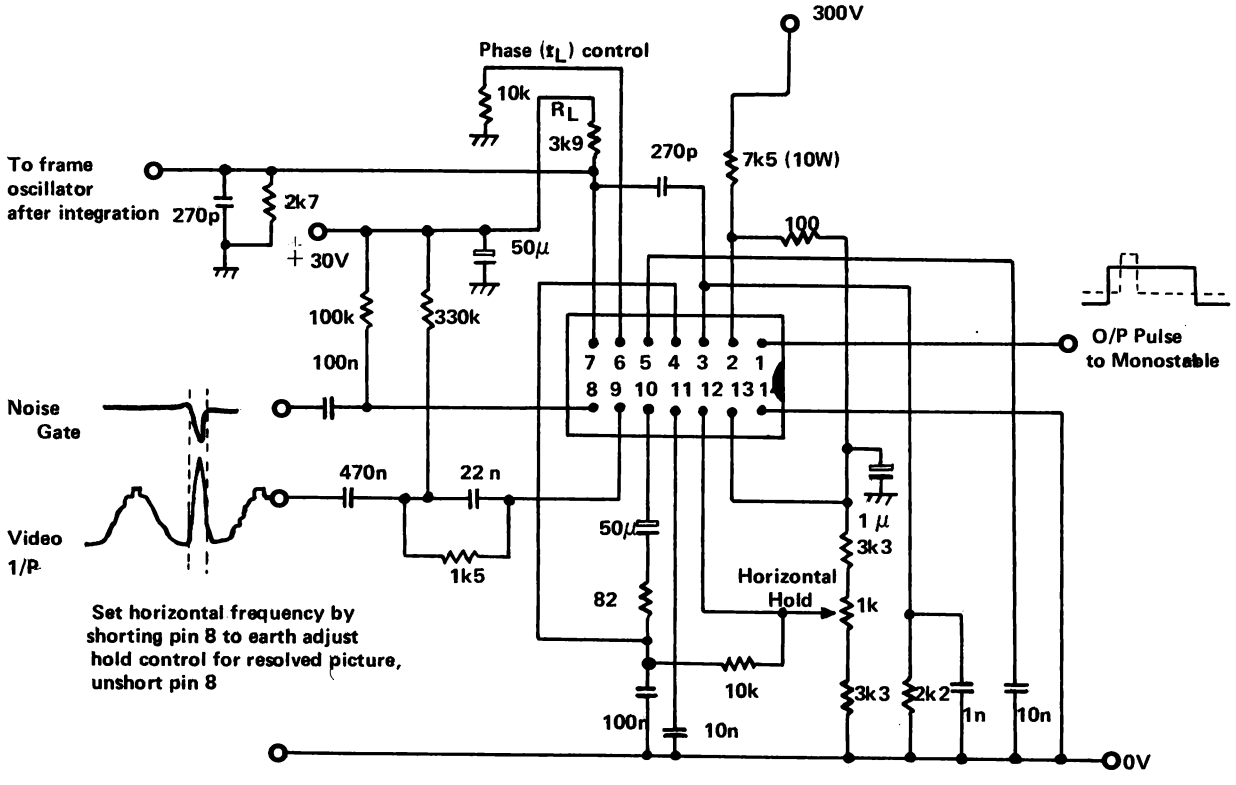
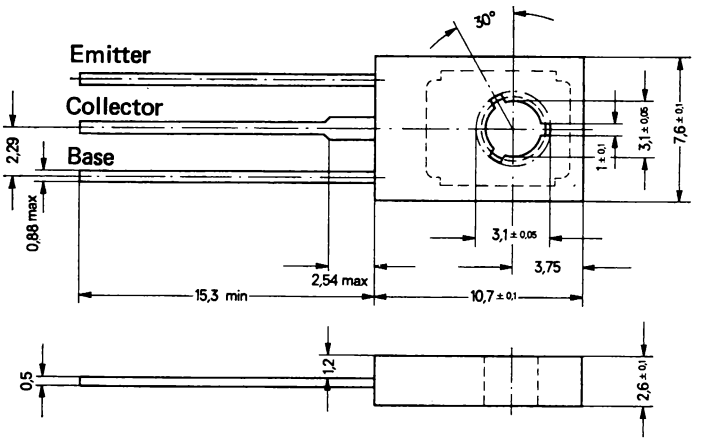


FIGURE 6 PRINTED CIRCUIT BOARD COPPER SIDE



APPLICATION OF A SN76533 AS A LINE OSCILLATOR AND PHASE COMPARATOR

Mechanical Outline



SOT-32

All dimensions are in mm.

Absolute Maximum Ratings at 25°C Free Air Temperature (unless otherwise stated)

Collector-Base Voltage	500V
Collector-Emitter Voltage (Note)	325V
Emitter-Base Voltage	6V
Continuous Collector Current	1A
Continuous Device Dissipation at (or below) T_C = 25°C (Note 2)	8.5W
Storage Temperature Range	150°C
Lead Temperature 1/16 inch from Case for 10 seconds	260°C

Electrical Characteristics at 25°C free-air temperature (unless otherwise stated)

	Parameter	Test Conditions	Min.	Typ .	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 500μA, I_E = 0	500			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10mA, I_B = 0 (Note 3)	325			
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 50μA, I_C =,0	6			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 10V, I_C = 5mA V_{CE} = 10V, I_C = 50mA V_{CE} = 10V, I_C = 100mA	30 30 20		240	
V_{BE}	Base-Emitter Voltage	I_B = 10mA, I_C = 100mA			1.5	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 15mA, I_C = 100mA			0.5	V
$I_{C\ (pk)}$	Peak Collector Current				3	A
C_{obo}	Common-Base Open-Circuit Output Capacitance	V_{CB} = 10V, I_E = 0 V_{CB} = 20V, I_E = 0 V_{CB} = 30V, I_E = 0		5.4 4.3 4.0	5	pF pF pF
I_{CES}	Collector Cut-off Current	V_{CE} = 300V, I_B = 0			100	μA

Notes
1. This value applies when the base-emitter diode is open circuited
2. Derate linearly to 150°C free-air temperature at the rate of 68mW/°C
3. These parameters must be measured using pulse techniques, t_p = 300μs. Duty Cycle 2%

Monochrome TV Circuit Design Using the BUY 71 2. 2KV Transistor
(B126)

MONOCHROME TV CIRCUIT DESIGN USING THE BUY71 2.2kV TRANSISTOR

by
Mick Maytum

ENVIRONMENT

Competitive pressures in the monochrome television market have forced circuit designers to become very cost conscious. Also, because price/cabinet combinations are the basic factors motivating the sale of television sets, further pressures exist to reduce the cost of the components.

The availability of low cost, high performance, small signal transistors caused a rapid change from vacuum tubes to transistors in the tuner and IF amplifier areas of the television (Figure 1). Continued transistor development resulted in high voltage devices such as the BF259 [$BV_{CBO} > 300$ V, $I_{C(max)} = 100$ mA, $P_{C(max)} = 5$ W] which ousted vacuum tubes from the video output stage. In the power supply unit, silicon rectifiers, typified by the 1N4000 series, quickly replaced the vacuum tube rectifiers used for half wave mains rectification.

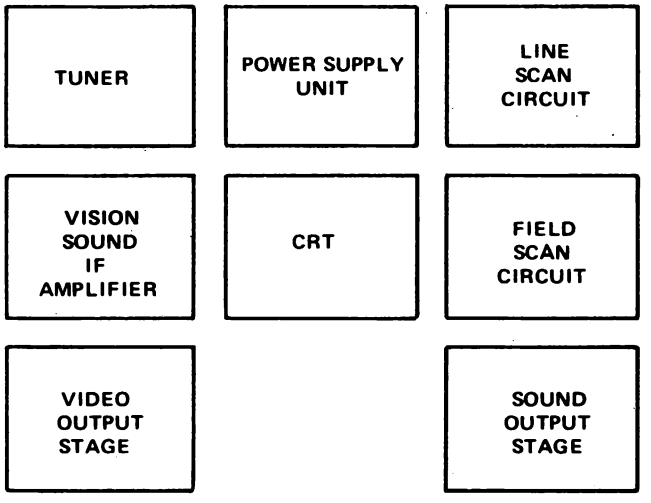


FIGURE 1. Typical Subsystems of a Monochrome Television Receiver

Most of the television receivers produced in 1972 are hybrids, with semiconductors in the positions described in the previous paragraph, and with valves performing the line, field, and audio output power functions. The choice of vacuum tubes for these three functions was really decided by the line output stage, which, when employing a vacuum tube, can be directly driven from rectified ac mains and could be made to stabilize against load and mains variations. Early linescan transistors, such as the BU107, had only a 300 V rating and thus required expensive mains transformers and series stabilizers for the linescan supply voltage. The supply rail voltage required for a linescan transistor is approximately one tenth of its BV_{CEX} rating. Advances in technology have increased linescan transistor ratings above 600 V (60 V supply rail) into the 1.2 kV – 1.5 kV region (120 – 150 V supply rail). Development was then almost static for the next few years due to relatively low volume device usage in Europe, resulting in high prices, and little development incentive in the U.S.A., where 1.2 kV transistors matched the rectified 120 V ac mains voltage. Even if European device prices had been low, set designers still had to solve the problem of how to 'lose' about 100 V from the rectified 220 – 240 V European ac mains.

This situation resulted in many ingenious circuit solutions. One popular method of increasing the supply voltage requirement was to stack the HT and LT rails, giving voltages in the 170 V to 200 V region. Component failure in the HT rail could feed high voltages into the LT system, necessitating protection circuitry for the LT rail.

Thyristor stabilized power supplies, providing 150 V output, have been proposed, but suppression problems and large capacitor values have, in general, ruled them out.

As the final voltage required is half of the rectified mains voltage, an ideal situation is formed for shunt stabilization.[1] The shunt stabilizer is usually placed on the scan rectified LT supply making Class B audio stages possible. This is the most cost effective solution for 1500 V linescan transistors, though careful cabinet design and circuit board layout are necessary because very large amounts of power have to be wastefully dissipated. The dangerous fault condition for this configuration would be an open circuit LT stabilizer, leading to an over voltage of the line output transistor and cathode ray tube.

The introduction of the BUY71, a 2200 V, 1.5 A monochrome linescan transistor, frees designers from the

design problems of 1500 V transistors by operating from a higher supply voltage and hence, taking less current. These factors enable the realization of greater set efficiency, better reliability and ultimately lowered costs.

BUY71 CIRCUIT DESIGN

Collector Circuit

The peak collector-emitter voltage rating of the BUY71 is 2200 V. This voltage should only be approached with all worse case conditions, i.e., line oscillator frequency low, supply line high and shortest flyback time. To arrive at the nominal peak working voltage, a derating factor is used. Usually this factor is about 0.75, yielding a nominal peak V_{CE} of 1650 V. For third harmonic tuning of the collector voltage waveform and an 11 μs flyback time, a supply of 200 – 210 V will be required.

A flashover protection resistor value of 100 Ω is recommended for the BUY71. Hence, if the linescan stage power consumption is about 40 W, then the input supply voltage will be in the region of 225 – 235 V. The permissible 50 Hz ripple content of the input supply is of the order of 1 V.

Figure 2 shows the collector circuit essentials of an early BUY71 design. The line output transformer was obtained by modifying a unit designed for a 1500 V transistor.

Forward scan rectification for the LT supply was performed by a fast recovery diode D5 (1SX174) and smoothing given by capacitor C4. Diodes D1 to D3 (1N4006), capacitor C3 and bleed resistor R2 provided a clipper ('snubber') circuit to limit the peak flyback voltage on the transistor after a flashover. Diode D4 was the EHT rectifier stick. Capacitor C2 was for flyback tuning and capacitor C1 for yoke current 'S' correction.

The yoke, L1, was tapped into half way up the line output transformer primary. This produced extra dissipation in the flashover protection resistor, together with severe scan modulation. Tapped thus, half the yoke sawtooth current flowed into the BUY71 collector and the other half in the flashover protection resistor. Partial decoupling of the protection resistor improved the circuit operation, but reduced the effectiveness of the protection resistor under flashover conditions. Thus, a yoke which matched directly into the BUY71 collector was shown to be necessary.

To reduce the peak voltage (relative to the chassis) across the directly driven yoke, a split primary of the line output transformer was used. The yoke ends were then at +900 V and −700 V during flyback. An additional advantage of this system was the cost reduction due to capacitor C3 now needing only a 1 kV rating, rather than 2 kV as previously. The final circuit configuration for the line output stage is shown in Figure 3.

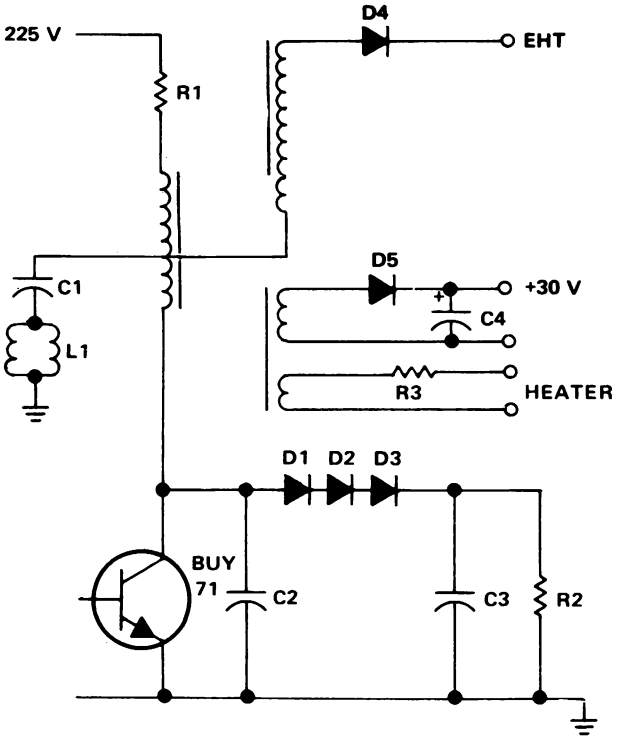


FIGURE 2. Early BUY71 Line Output Stage Design

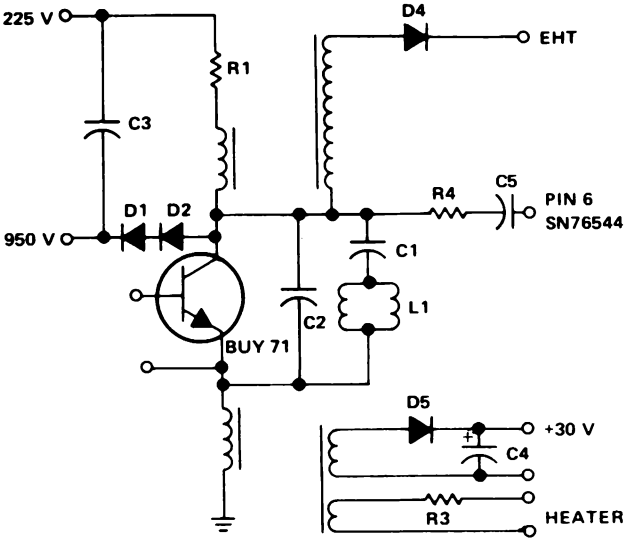


FIGURE 3. Balanced BUY71 Line Output Stage

Power Losses

To achieve the low operating losses possible with the BUY71, the base drive waveform must comply with the recommended drive conditions detailed later in the base circuit section. Using these drive conditions will ensure the device loss is below the values given in Figure 4.

The power losses are shown for a transistor case temperature of 80°C measured at the transistor's mounting flange. This provides a convenient reference point, easily accessible for measurement by the design engineer. Allowance is made in the power curve for a ±20% variation in the nominal peak working collector current value and a corresponding change in the base drive waveform. Hence, the 6.2 W maximum power loss quoted for a nominal

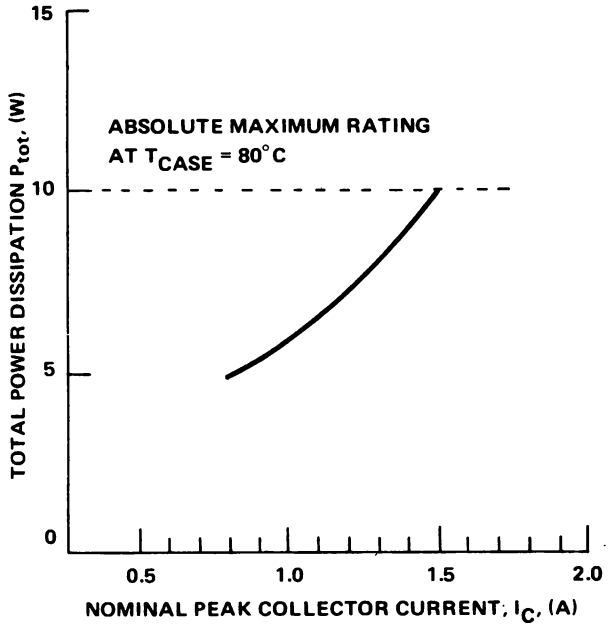


FIGURE 4. Maximum BUY71 Dissipation (P_{tot}) versus Nominal Peak Collector Current When Operating in a Line Output Stage With $T_{CASE} \leq 80°C$

collector current of 1 A is the maximum loss occurring in the collector current range 0.8 A to 1.2 A for $T_{CASE} \leq 80°C$.

If the BUY71 is mounted on a heatsink near the bottom of the television, the local ambient temperature might only reach 55°C. The maximum permissible thermal resistance from case to (local) ambient would be (80 – 55)/6.2 ≈ 4°C/W. Allowing 1°C/W for device mounting, a 3°C/W heatsink is required. This could be achieved with a piece of aluminum 10 cm X 30 cm, i.e., the screening shield for the line output transformer and rectifier.

At a nominal collector current of 1.5 A, the maximum device loss is equal to the transistor's maximum rating at 80°C. In order to work the device at 1.5 A, the expected tolerances must be carefully evaluated.

A mean power of about 40 W is supplied to the top end of the primary. The distribution of this power around the line output stage is shown in Figure 5. This power is relatively constant, due to the use of the SN76025 Class A audio IC, and thus the power supply design, discussed later, is simplified.

Base Circuit

The operating efficiency and overall reliability of linescan transistors are very much functions of the transient

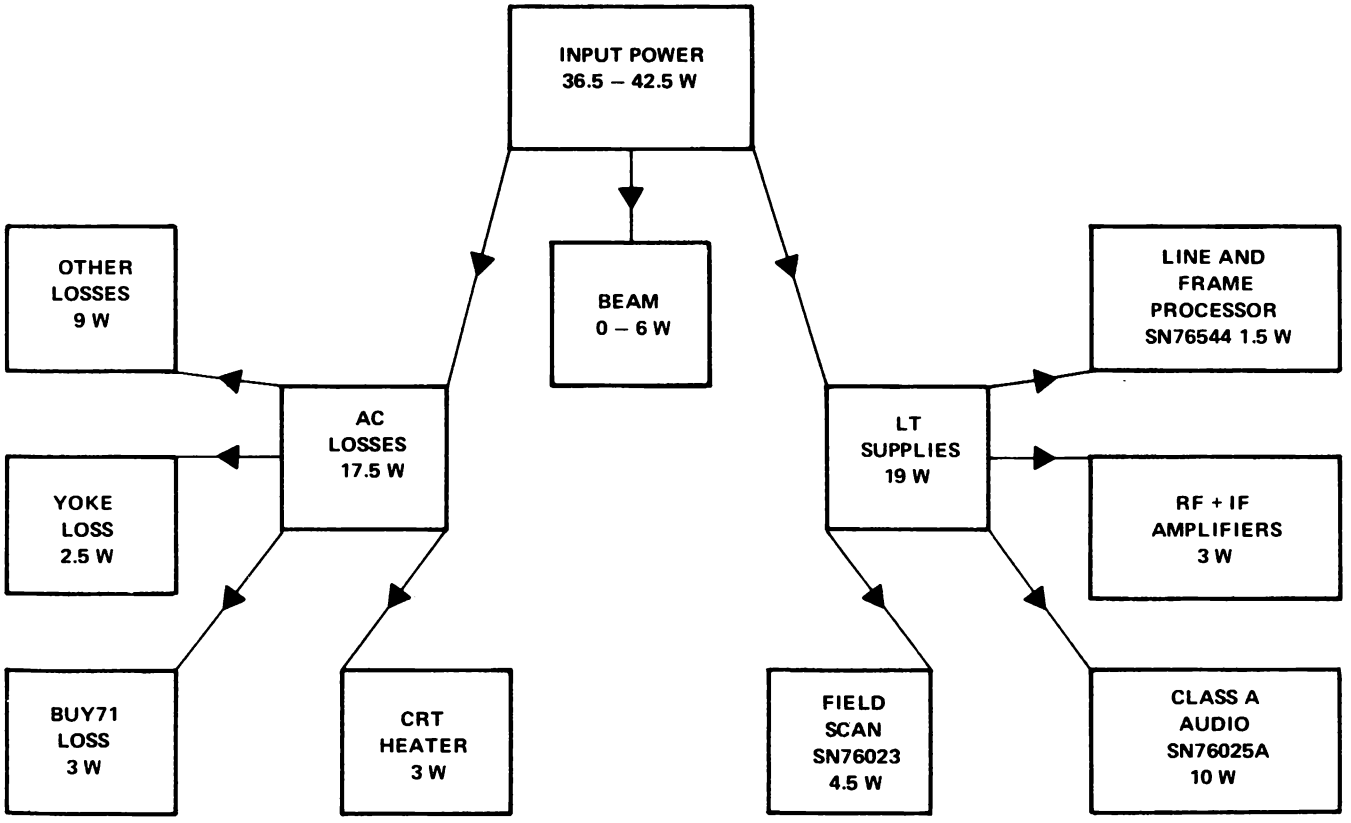


FIGURE 5. Line Output Stage Power Distribution

dissipation during device "turn-off", which is controlled largely by the applied base drive.[4]

The critical factors in the drive waveform for high voltage transistors have been determined, and it is recognized that optimization of these must comprehend device distributions, the total conditions of operation and the circuit tolerances experienced during equipment manufacture.

The values given in Figure 6 are for the drive parameters as defined in Figure 7 for a BUY71, operating in a line output stage, without an efficiency diode, and comprehend operation at case temperatures up to 80°C and variations of ±20% on nominal values due to supply and frequency variations and circuit component tolerances.

At a collector current of 1 A, Figure 6 recommends $I_{B(end)}$ = 0.35 A, dI_B/dt = 0.17 A/μs and resistor R_{BE} = 47 Ω. The purpose of resistor R_{BE} is to prevent ringing during the off period of the transistor. Its value is not critical and can be subjected to the normal preferred value tolerances. The values of R_{BE} in Figure 6 are chosen so that the resistor's current is not comparable with $I_{B(end)}$ at the end of scan, otherwise the tolerance on $I_{B(end)}$ is increased.

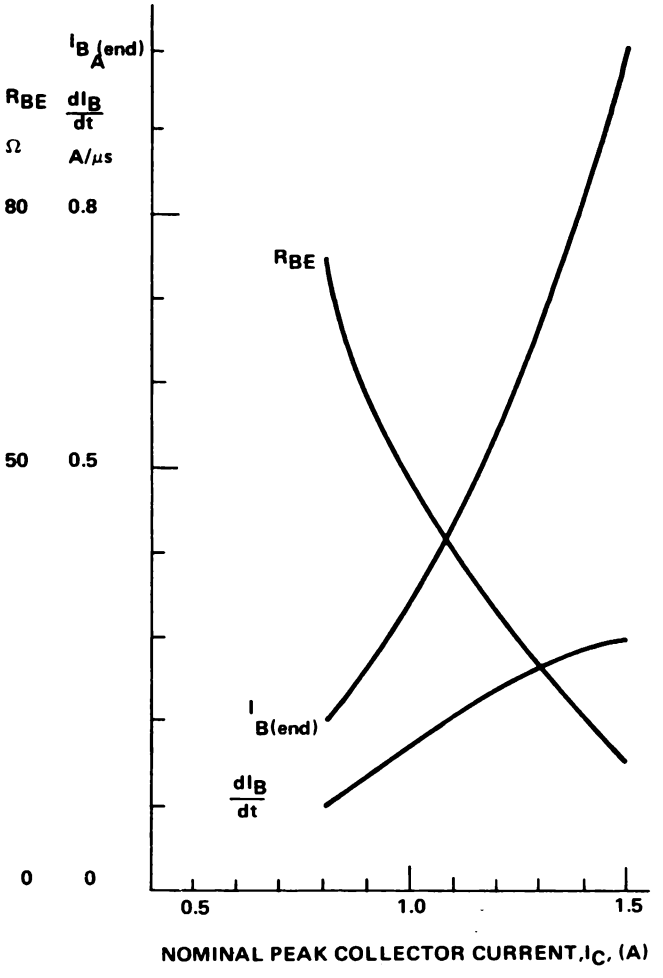


FIGURE 6. BUY71 Recommended Drive Conditions versus Nominal Peak Collector Current for Minimum Dissipation

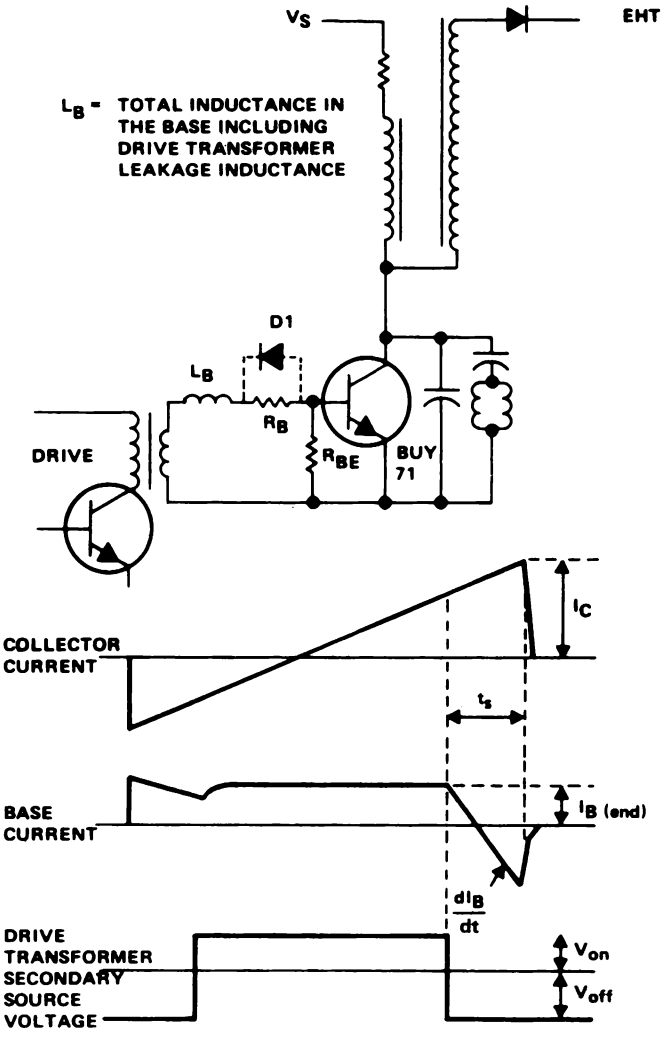


FIGURE 7. Line Output Stage Drive Parameters

The starting point in the base circuit design is the transformer negative source voltage, V_{off}, where a range of −3 to −5 V is recommended. Choosing V_{off} = −4 V and assuming the line driver is driven by the SN76544 line and frame processor integrated circuit, which has a mark space ratio of 28:36, the positive source voltage, V_{on}, will be 4 X 28/36 = 3.1 V. Allowing 1 V for V_{BE}, the value of resistor R_B is:

$$R_B = (V_{on} - V_{BE})/(I_{B(end)} + V_{BE}/R_{BE}) \quad (1)$$
$$= (3.1 - 1)/(0.35 + 1/47)$$
$$= 2.1/0.37$$
$$= 5.6\ \Omega$$

This resistor value then defines $I_{B(end)}$ and it is now necessary to find the value of inductance L_B to produce the required dI_B/dt.

Figure 8 indicates approximate values of L_B to produce certain dI_B/dt values. For dI_B/dt = 0.17 A/μs and

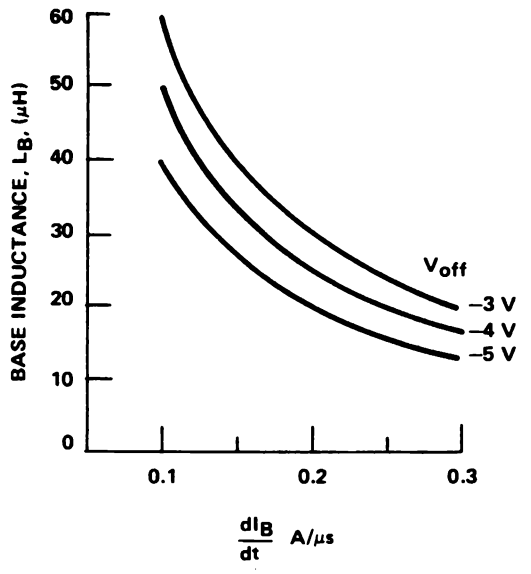


FIGURE 8. Determination of L_B to Obtain Correct dI_B/dt for Various Values of V_{off}

V_{off} = −4 V, a value of 30 μH is suggested. Once the circuit is constructed, a fine trim is made on inductor L_B to produce the required dI_B/dt *measured* on the actual base current waveform. The absolute value of L_B is unimportant, it is the value of dI_B/dt resulting from it which is critical.

To determine whether diode D1 (Figure 7) is needed to shunt resistor R_B during the storage time, t_S, Figure 9 is used. The maximum value of t_{off}, at 1 A collector current

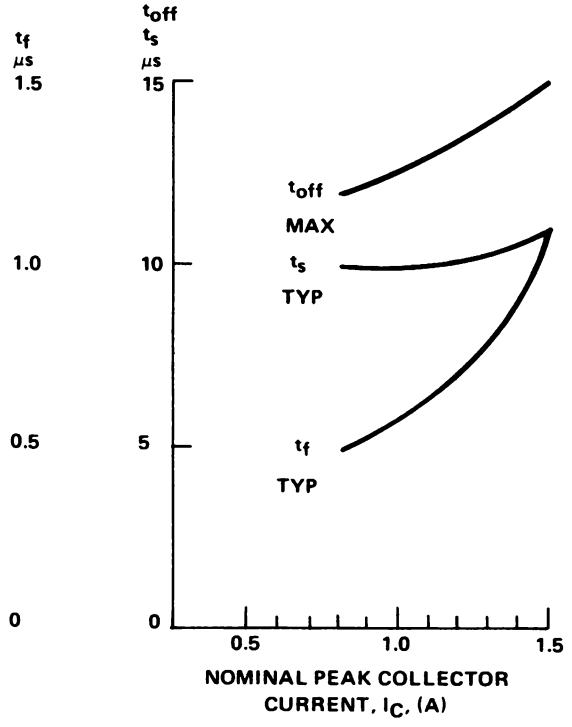


FIGURE 9. BUY71 Switching Times When Operating in a Line Output Stage With T_{CASE} = 80°C

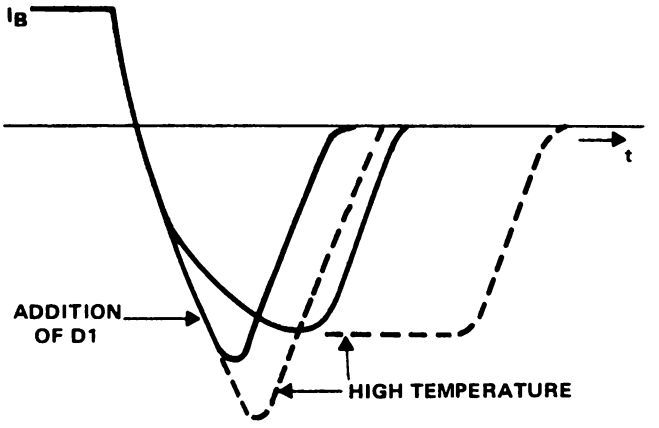


FIGURE 10. Temperature and Device Variations on dI_B/dt

and 80°C case temperature, is 12.5 μs. To maintain the dI_B/dt slope over this time period, $L_B/R_B \geqslant 12.5$ μs. As this condition is not met, L_B/R_B = 30/5.6 = 5.4 μs, diode D1 is required. Figure 10 shows the effect of the diode on the dI_B/dt.

The diode, D1, shunts the base drive resistor R_B and therefore maintains dI_B/dt and reduces storage time variability with temperature and between devices.

Temperature has an influence on the storage time, t_S. Figure 9 shows that the latter is typically 10 μs at 80°C whereas, at more normal case temperatures, it would be in the 6 to 8 μs region and would mask any resistive limiting in the negative base current. At higher temperatures, t_S would lengthen very rapidly due to a constant negative off drive. The transistor could then fail, either if the fall time, t_f, became too long or because the start of the forward base drive entered flyback. Thus, the need of diode D1 should always be assessed from $L_B/R_B > t_{off}$ rather than from low case temperature observations made on the base current waveform.

Line Driver Stage and SN76544 Feed (Figure 11)

The secondary of the driver transformer, T1, was designed in the previous section. Choosing a turns ratio, n, of 25 means that the average primary voltage will be nV_{off} = 25 X 4 = 100 V above the emitter of line driver transistor VT1. Transistor VT1 will have a peak collector emitter voltage of $n(V_{off} + V_{on})$ = 25 (4 + 3.1) = 180 V. The driver transistor's collector current will consist of three parts:

a) That required to maintain constant ampere-turns, i.e., $I_{B(end)}/n$ = 15 mA
b) The current due to discharging the 'damping' capacitor C2 through resistor R2
c) That due to the charge extracted from the base of the BUY71 transistor.

Factors in b) and c) cause the peak collector current to be about three times the referred base current, i.e., 45 mA.

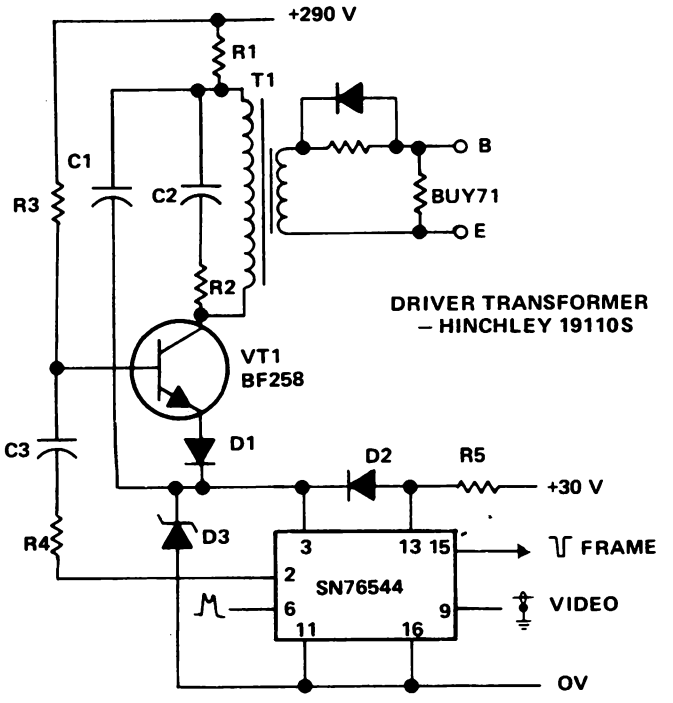


FIGURE 11. Line Driver Stage

Using a BF258 transistor for the line driver would mean the base current supplied by feed resistor R3 should be greater than $45/h_{FE(min)} \approx 45/25 \approx 1.8$ mA to hold the driver in saturation.

The overall efficiency of the driver stage is unlikely to be greater than 50%, and therefore primary feed resistor R1 will be supplying a mean current in the 15 – 20 mA region. The supply for resistors R1 and R3 should be taken from as near to the mains reservoir capacitor as possible. This will reduce the drop in base drive when the line output stage is overloaded, e.g., after a flashover. In an extreme case, e.g., an LT short, a strong drive to the line output will reduce its dissipation until the supply fuse blows.

One problem that faces the set designer is how to start the line oscillator. This drives the line driver which, in turn, switches the line output transistor from which the LT supply for the line oscillator is derived. Figure 11 shows one way of breaking this vicious circle. This circuit has previously been used successfully in industrial switching mode power supplies. When the input supply to resistors R1 and R3 is rising, transistor VT1 is biased hard "on", passing current into the line oscillator supply of the SN76544 line and frame processor. At about 50 V input, the line oscillator starts and drives the pulses, via capacitor C3 and resistor R4, into the base of transistor VT1, which, in turn, drives the base of the BUY71 transistor. Once this transistor starts to operate, the LT supply is produced, the field section of the SN76544 starts to function, and additional current is also fed into the line section. In normal operation, regulator diode D3 clamps the SN76544 line section supply to 12 V. Diode D2 prevents extra loading of the line section during "start-up" and clamps the field section supply to 13 V during normal operation. Resistor R4 limits the negative base current of VT1 and also gives flashover protection of the IC output. Diode D1 prevents the 11 V output swing of the SN76544 from breaking down the base emitter junction of transistor VT1. Decoupling capacitor C1 should adequately decouple the top end of the line driver transformer primary from high frequency ripple – a value of 220 nF usually suffices. Some 50 Hz component will probably be present on the supply to feed resistors R1 and R3, but, provided this does not cause more than 10% variation in the base current of the BUY71 transistor, the value of capacitor C1 need not be increased in value to decouple it.

Power Supply

All the power supply systems described in the introduction could be used with the BUY71 transistor. The design of such systems to provide BUY71 compatible rails would follow the same design techniques evolved for the lower voltage 1.5 kV device.

With the BUY71 transistor, the necessity of supply rail stacking does not arise because its supply requirement is in the 170 – 200 V region. This means the LT circuits are completely safe in the event of line output stage failure.

Two power supply options are described in this section, one unstabilized for low cost applications and the other stabilized for situations where frequent ac mains variations occur. Both solutions consume 50% less power than the shunt stabilized technique.

Unstabilized PSU

This system, shown in Figure 12, is the classical half wave rectified power supply followed by CR smoothing. Fuse F1 protects the system and components, capacitors C1 and C2 and resistor R2 protect the rectifier diode D1 against excessive voltages and currents. Resistor R1 serves to discharge any static voltage left on capacitors C1 and C2. Capacitor C3 is the reservoir capacitor. Resistors R3 to R6 and capacitor C4 reduce the 50 Hz ripple voltage to an acceptable level. A fine trim on the supply output voltage for adjusting scan width is obtained by shorting resistors R5 or R5 and R6. Resistor R3 is shorted for 220 V ac mains operation.

As described in the previous section, the supply for the line driver stage is taken as close to the reservoir capacitor as possible. A feed to the video output stage is also taken from this point to reduce the effect of line output stage variations.

Picture "breathing", due to brightness (beam current) variations, is about 2%. Hence, the use of an unstabilized supply reduces "breathing" by a factor of two times when compared with a shunt stabilized or a hybrid television. However, "breathing" caused by ac mains variations is several times worse for the unstabilized system, i.e., about half the percentage change of the mains.

Stabilized Supply

The output regulation of the stabilized supply must match the unstabilized supply's regulation to produce

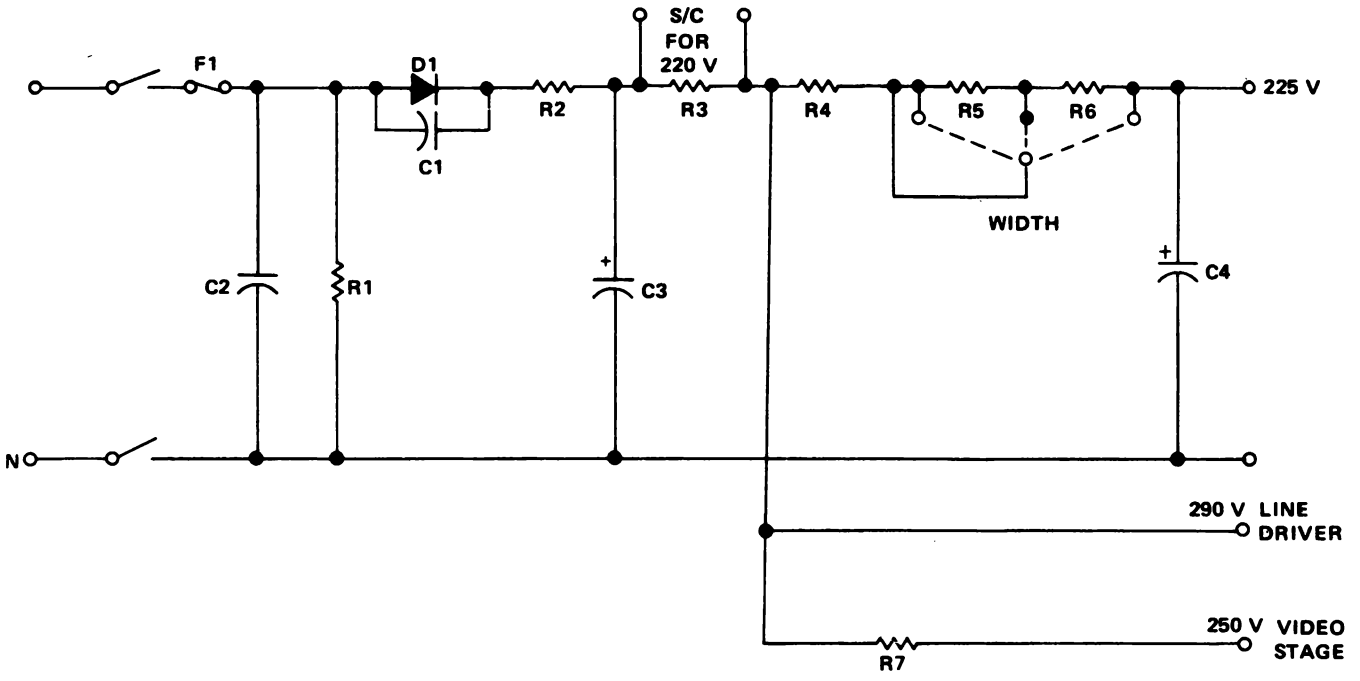


FIGURE 12. Simple Unstabilized Power Supply Unit

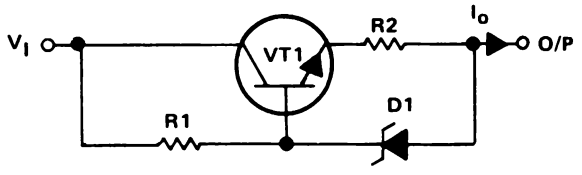


FIGURE 13. Current Source Stabilizer

compatible "breathing" with beam current. However, the stabilized supply must stabilize against ac mains variations. The requirement of high output impedance, coupled with insensitivity of voltage across the stabilizing element, can be satisifed by a current source (Figure 13). Here zener diode D1, fed by resistor R1, stabilizes the base voltage of transistor VT1. If current and temperature variations in the zener and base emitter voltages are small, then the voltage across emitter resistor R2 is constant. Hence, this circuit acts as a constant current source of $I_O = (V_Z - V_{BE})/R2$ (neglecting the zener current which is assumed to be small).

In the event of an output short circuit, transistor VT1 would dissipate a very large amount of power. The addition of resistor R3 (Figure 14) reduces the collector current to zero when the voltage across the stabilizer exceeds I_O (R2 + R3).

Under short circuit output conditions, the base emitter junction will be heavily reversed biased by $[V_Z - V_I] / [R2/(R3 + R2)]$. To protect the junction against breakdown, an additional diode, D2, is used. Resistor R4 is used to reduce the transistor's dissipation by setting its value such that it is just saturated at the lowest input voltage. Capacitor C2 serves to reduce 50 Hz modulation of the current source.

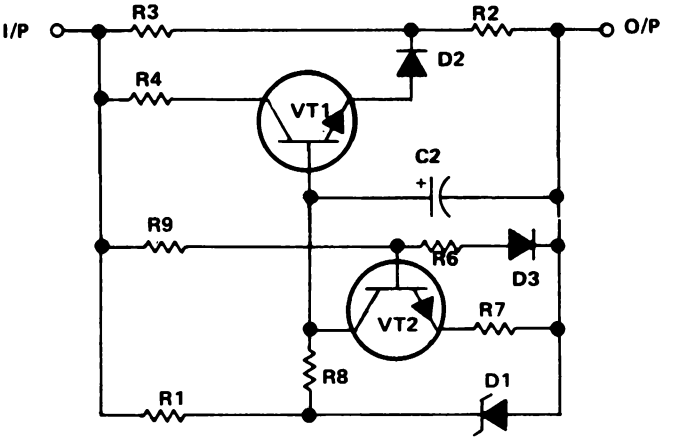


FIGURE 14. Improved Current Source Stabilizer

The fact that this stabilizer solution operates as a constant current source has several advantages. First, the smoothing capacitor at the output can be very much smaller than usual because it is being driven by a constant current source. Second, under flashover conditions, the supply current to the line output stage is limited. The heatsink required for transistor VT1 is relatively small because its maximum dissipation is in the region of 5 W. Tapping resistor R2 would permit adjustment of current I_O to set the scan width.

The output impedance of the stabilizer was improved from 800 Ω to 2,600 Ω by the addition of transistor VT2, diode D3 and resistors R6, R7, R8, and R9. Changes in the voltage across the stabilizer are fed, by resistor R9, to the base of transistor VT2 and the resulting change in its

collector current, flowing through resistor R8, modifies the base voltage and thus the current of the power transistor VT1. Thus, if the voltage across the stabilizer increases, the base voltage of transistor VT1 will fall, reducing the stabilizer's current (and hence increasing its output impedance) by an amount depending on the relative values of resistors R6, R7, R8, and R9. Diode D3 compensates for the base emitter voltage of transistor VT2.

CONCLUSIONS

An almost complete circuit diagram for a monochrome television using the BUY71 transistor is shown in Figure 15. Because of limited space, the tuner and video IF amplifier (SN76654 integrated circuit) are not shown. Power feeds to this section are, however, indicated.

The vertical deflection circuit uses an SN76023N power integrated circuit, running from the scan rectified 30 V rail.[2] Full external component details are shown for the SN76544 line and frame processor integrated circuit. The operation and tolerancing of this device are described in Reference 3.

The 6 MHz sound limiting and demodulation integrated circuit is an SN76660SS. This device is an improved SN76660 with regard to sensitivity, AM rejection and dc volume control range. The 13 V supply for the frame section of the SN76544 can also be used to drive the SN76660SS.

An SN76025A Class A audio integrated circuit easily provides 1.5 W into the 80 Ω loud speaker. As the supply current change from zero signal to limiting is very good, being less than 2%, audio picture modulation is negligible. The line output transformer screening provides an ideal heatsink on which to mount the 5 pin audio.

The remainder of the circuits are described in the text. The economics of this system can best be realized by noting the few number of active devices, i.e., only four integrated circuits, a BUY71 linescan transistor, one plastic power transistor and three low level transistors.

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2. Jonathan A. Dell, "The Application of Audio Integrated Circuits to Vertical Defection Systems," Texas Instruments Application Report B128.

3. Kuldip Rupra, "Applications of the SN76544 Line and Frame Processing Integrated Circuit," Texas Instruments Application Report B125.

4. Kenneth Salmon, "High Voltage Switching Transistors", Texas Instruments Application Report B131.

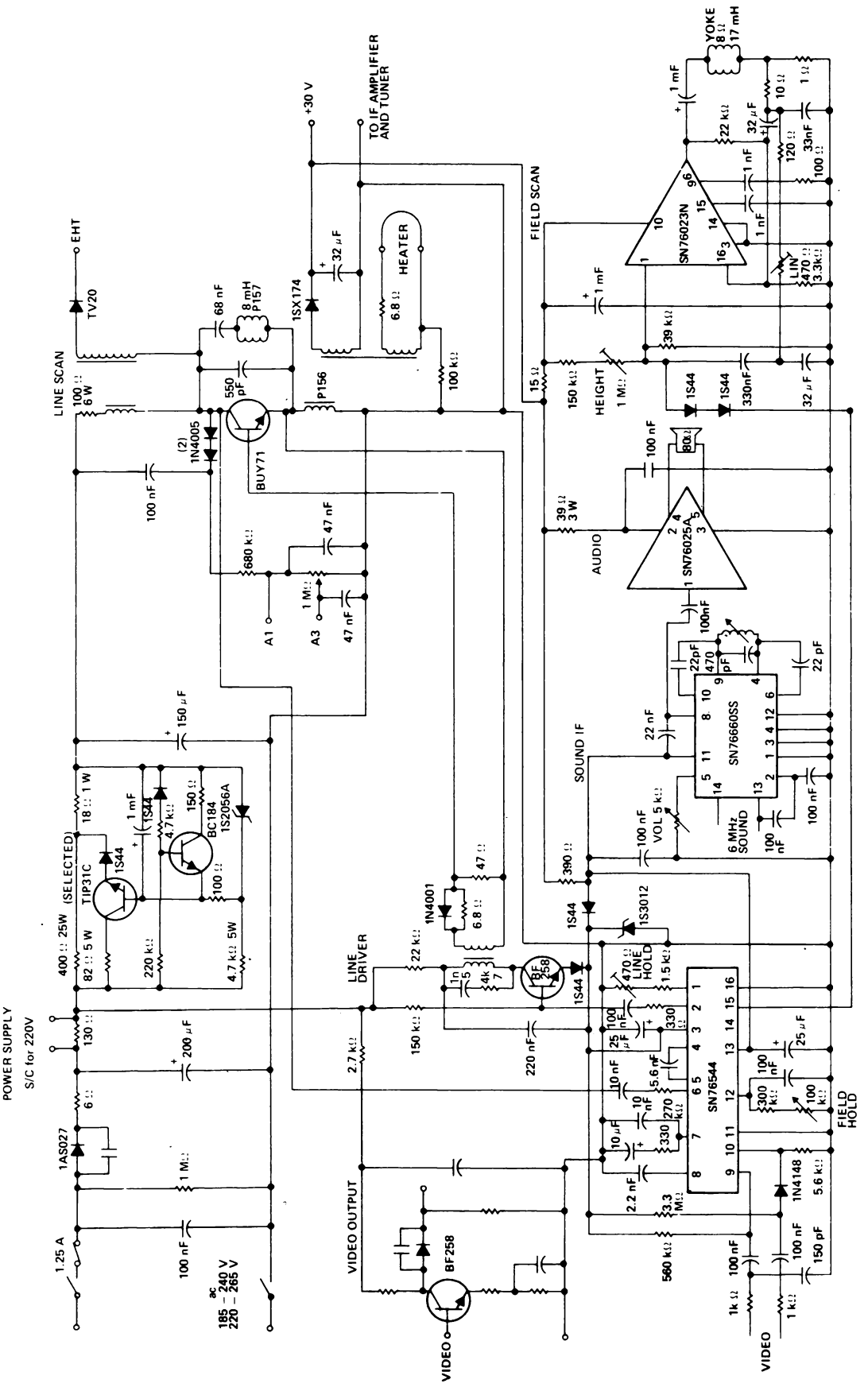


FIGURE 15. Power Functions of a Monochrome Television Receiver

APPENDIX

COMPARISON OF BUY71 (2.2 kV) AND BU105 (1.5 kV) TRANSISTOR SYSTEMS

A BUY71 system provides the following advantages compared to a BU105 system:

1) The supply rail requirement for the BUY71 system is 220 V compared with 150 V for the BU105 system. Thus, the BUY71 power supply current is smaller which, coupled with the lower voltage loss occurring in the power supply series element, gives reduced power losses in the supply. Alternatively stacked LT and HT systems may be replaced with a BUY71 system which provides complete isolation of the LT system from HT feedthrough.
2) The BUY71 transistor has a lower maximum power loss than the BU105 transistor and, therefore, the overall set efficiency is improved (see Figure 16).
3) The lower base drive requirement of the BUY71 transistor simplifies the line driver design (Figure 17). When designing the high voltage driver stage needed for the BU105 transistor, a decision must be made as to whether to use a medium power TO5 cased transistor (e.g., the BF259), working near its maximum collector current rating where the h_{FE} is low, or a larger and more expensive SOT32 power device (e.g., BD410) to improve efficiency. The BUY71 base current, being 50% lower, allows the driver transistor to be either a TO5 case transistor or a super silect (e.g., BFR88), both running at a collector current where their gain is high. Size reductions can also be made in the line driver transformer.
4) This report has discussed currently known and used circuit techniques employing BUY71 transistors. Future circuit developments employing the BUY71 characteristics should be a self-oscillating line output stage, which would eliminate the line driver transformer. Also, the voltage capability of the BUY71 transistor makes it extremely suitable for self-regulating line output stages.

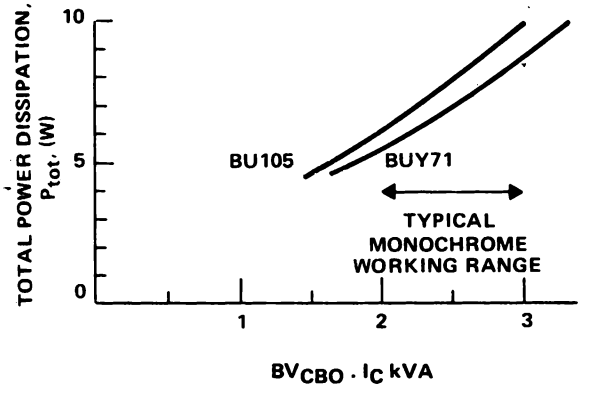


FIGURE 16. Maximum Transistor Dissipation (P_{tot}) versus kVA When Operating in a Line Output Stage

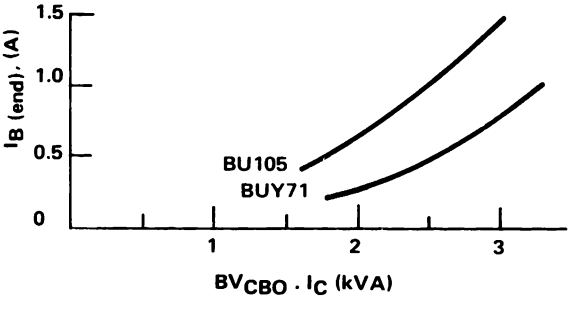


FIGURE 17. Linescan Transistor $I_{B(end)}$ versus kVA

Chopper Power Supplies Using BUY 69/70 High Voltage Power Transistors
(B116)

CHOPPER POWER SUPPLIES USING BUY69/70 HIGH VOLTAGE POWER TRANSISTORS

By Mick Maytum

INTRODUCTION

The BUY69 and BUY70 range of transistors have been designed for high voltage inductive switching applications. Their power switching losses are very small as their maximum switching fall time is 1μs. Hence using them, high power switching mode power supplies, operating at 20kHz and directly from the mains, can be made. Further details of this type of supply are given in Application Reports B76, B83 and B114.

GENERAL PRINCIPLES

All the designs described in this report are intended to run from rectified mains or D.C. supplies in the 100V to 500V region. Small sized high frequency transformers provide isolation and step-up or step down of the primary waveform as required. Variations of loading and mains voltage can be reduced by modulating the switching devices conduction period.

SINGLE DEVICE SHUNT CHOPPER POWER SUPPLY

Figure 1 illustrates a simple form of chopper power supply. It is directly equivalent to the usual mains transformer, rectifier and smoothing capacitor arrangement used as the d.c. source for power amplifiers, series stabilisers, etc. For powers above 50VA a switching mode power supply offers lower weight and volume compared with the conventional unit. Its basic output power and voltage characteristics versus output current are shown in Figure 2.

Circuit Operation

The mains supply is full-wave rectified by diodes D1 – 4 and smoothed by capacitor C1. Resistor, R1, "bleeds" a small current into the base of transistor VT1 to initiate the oscillation of the supply. Transformer, T1, consists of four windings on a ferrite core. Winding N1 provides the base drive for transistor VT1, winding N2 forms the primary and winding N4 forms the output secondary. The purpose of winding N3 is to maintain a constant output voltage of up to the maximum output power. (See Figure 2). This winding may be bifilar wound with winding N2, or preferably sectionalised.

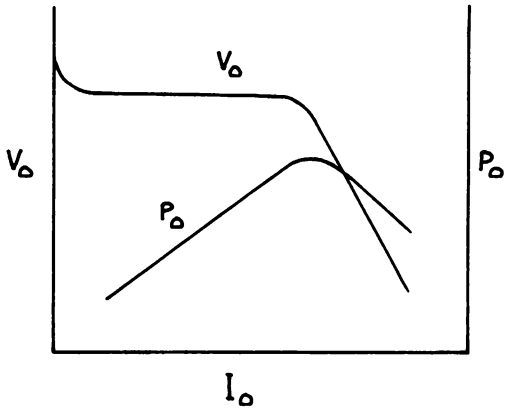


FIGURE 2

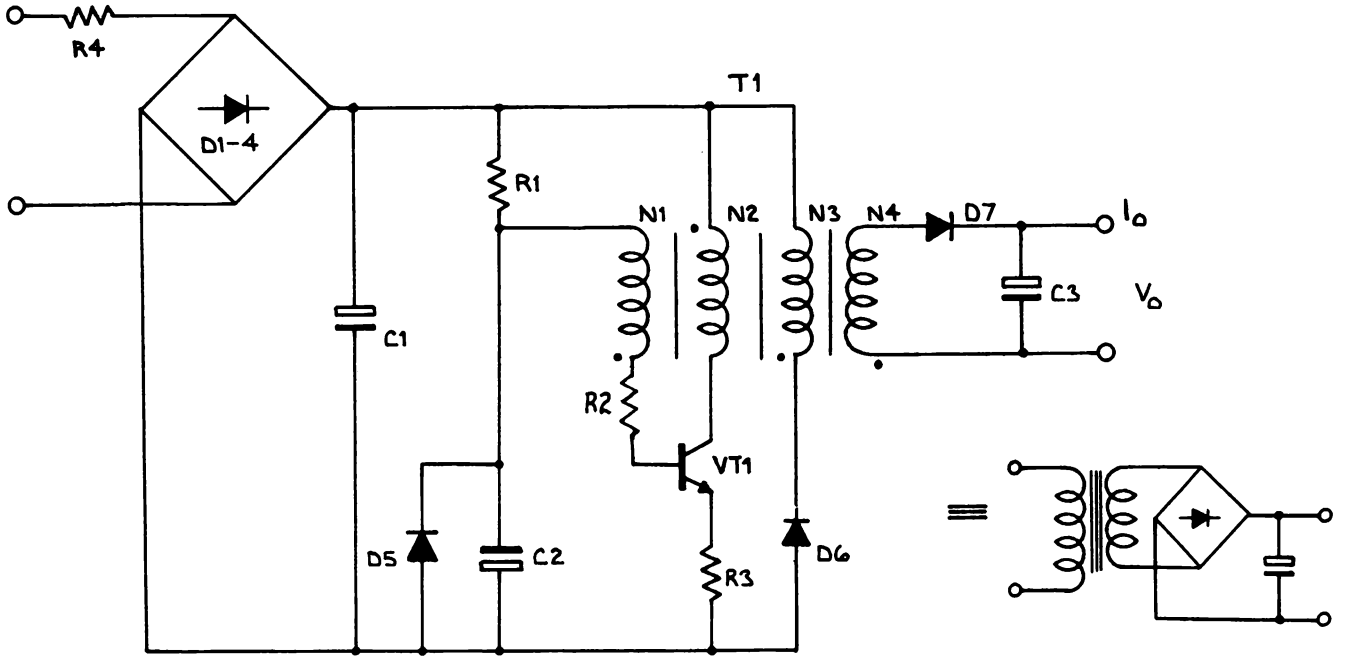


FIGURE 1

The collector current of transistor VT1 (Figure 3 (C)) will be a sawtooth whose slope ($\Delta I_C/\Delta t$) will be determined by the inductance L2 of winding N2 and the supply voltage V_S

$$\Delta I_C / \Delta t = V_S/L2 \qquad A/s$$

The peak value of collector current is limited to:–

$$I_{C(max)} \cong (V_S \cdot N1/N2 - V_{BE}) / R3$$

This is the condition for zero base current, i.e. the point in the operation where the device starts to switch off. The device in starting to switch off (i.e. V_{CE} rising) reduces the base drive voltage and regenerative action gives a fast device switch-off.

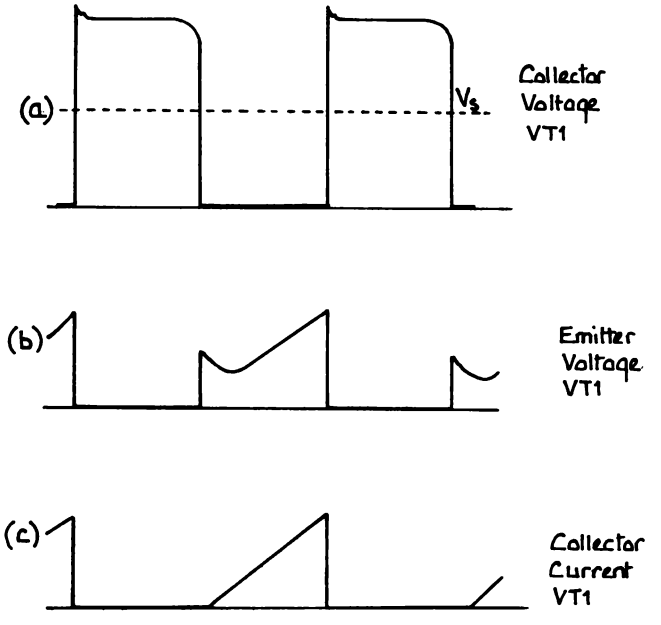


FIGURE 3 CIRCUIT WAVEFORMS

Energy, stored in the transformers core during the devices conduction period has two alternative "sinks". It can be returned to the supply V_S via winding N3 and diode D6 or transferred to the secondary load. In normal operation some energy is returned to the sypply and some to the load. The regulation of the secondary voltage starts to fall when all the energy is transferred to the load. This type of supply, if correctly designed, can tolerate open circuit and short circuit load conditions. If the winding N2 and N3 have equal turns the peak collector voltage will be $2V_S$ and the collector voltage waveform will be a square wave (Figure 3 (a)). As windings N2, N3 and N4 may handle equal powers, equal winding spaces must be allotted to these three windings. The power supply's output voltage will vary by the same percentage as the input mains but the frequency of operation will remain sensibly constant.

Design Considerations

The BUY70B device is specified at I_C = 4A and has a BV_{CER} > 400V and a BV_{CBO} > 800V. From a rectified supply of 300V an equal turns ratio for windings N2 and N3 will produce a peak collector voltage of 600. Working to a peak collector current of 4A, the maximum output power will be 300. 4. 0.5. 0.5 = 300W assuming a 50% duty cycle and neglecting transformer and rectification losses. Use of a BUY69B device working to a 8A peak collector current would give 600W.

Extensions to the basic circuit

The supply described will have the same percentage output voltage change as the input supply. It is possible to stabilise the output voltage against supply variations, and one form the additional circuits could take is shown in Figure 4.

Here a unijunction transistor oscillator defines the oscillation frequency. A fast thyristor turns transistor VT1 "off", the thyristors firing point being determined by an error amplifier and opto coupling link from the secondary.

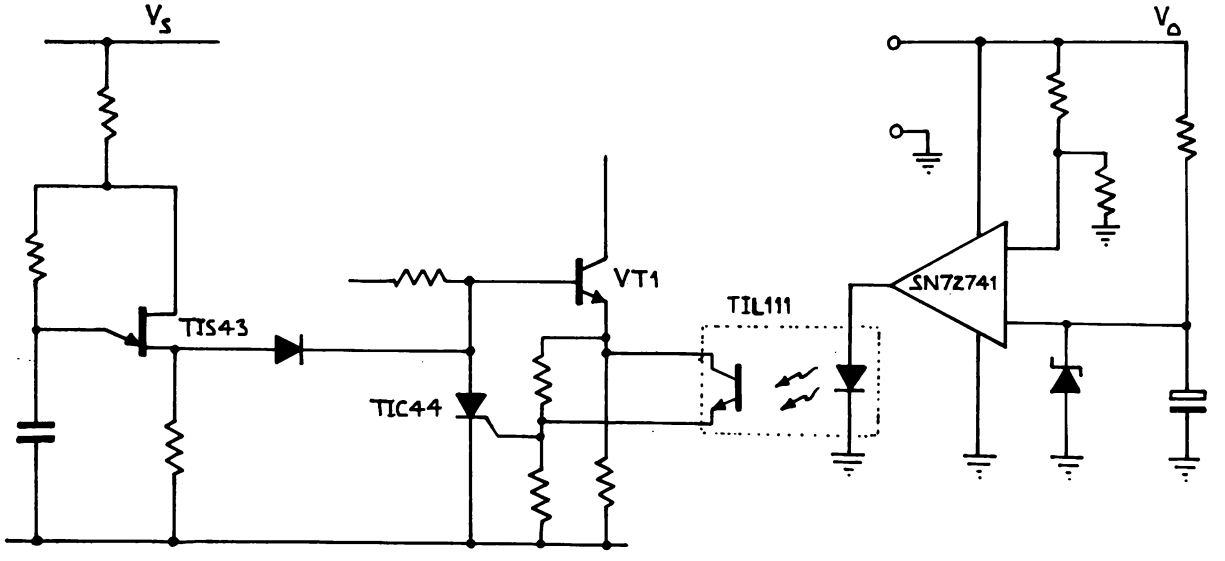


FIGURE 4

MODIFIED CIRCUIT TO INCREASE OUTPUT POWER

The power output of a single device shunt chopper may be increased by reducing the slope of the collector current of transistor VT1 and switching the device "on" before transformer T1 has delivered all its energy to the secondary load. Typical waveforms are shown in Figure 5.

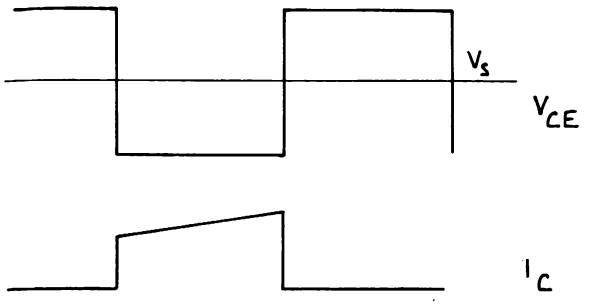


FIGURE 5

Taking the previous BUY70B example and specifying the collector current rising from 3A to 4A the power output becomes (3 + 4) x 0.5 x 0.5 x 300 = 525W. This output power for a BUY70B device operating at a collector current up to 4A is very nearly equal to the 600W obtained from a BUY69B device operating at 8A collector current when the initial collector current is zero. Thus increasing the transformer size, to produce a smaller ramp on the collector current pulse, makes better use of the devices peak current by giving more output power.

The circuitry to drive VT1 of necessity increases in complexity. A block diagram of this is shown in Figure 6.

Circuit Operation

Transformer T1 acts as an energy store, and when the transistor VT1 conducts the transformers stored energy is increased. This energy increase is transferred to the output load by diode D2 after transistor VT1 has switched "off" and the transformer's voltage reversed. Suitable selection of the output decoupling capacitor, C2, reduces ripple and noise to an acceptable level. The value of capacitor C2 will be relatively small due to the high "chopping" frequency.

An error amplifier, A1, which may be fabricated from any common integrated circuit differential amplifier (e.g. SN72741P) monitors the power supply's output voltage compared with a fixed voltage reference diode, D3 (e.g. a Y95AS). The signal from amplifier A1 controls the pulse width of the modulator, hence holding the power supply output voltage constant. Linking the control circuitry and the output transistor VT1 is a driver stage consisting of transistor VT2 and transformer T2. It is usual to arrange the windings of transformer T2 so that when transistor VT2 is conducting transistor VT1 is "off" and vica-versa. This form of operation gives a strong and defined turn-off drive for transistor VT1.

The current limit circuit, if activated, overrides the output of the amplifier A1 and reduces the output device's (VT1) conduction time to limit its peak current.

Waveforms for the circuit are shown in Figure 7.

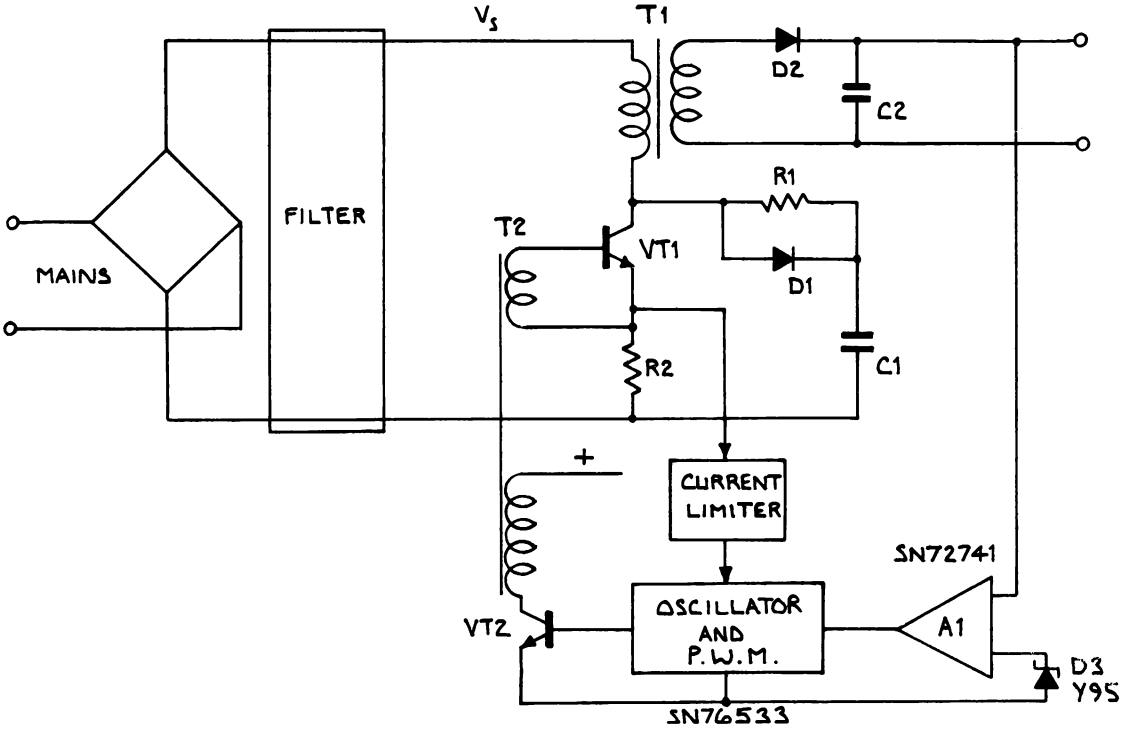


FIGURE 6

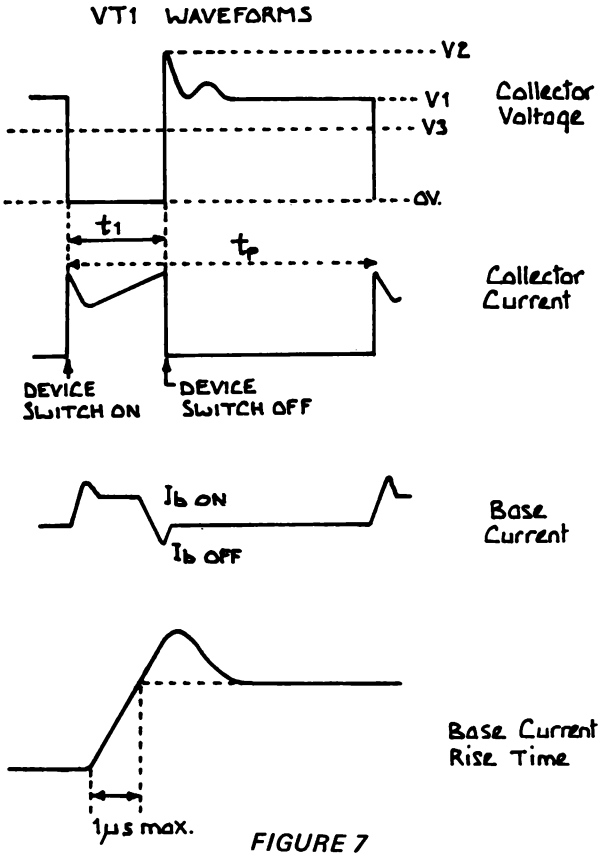


FIGURE 7

Switch-off Conditions of Transistor VT1

To ensure reliable operation of the transistor VT1 it is desirable that the device's collector current should have stopped flowing before its collector voltage exceeds the device's BV_{CER} rating. Capacitive damping applied to the primary of transformer T1 will slow the rate of rise of collector voltage at switch-off of transistor VT1. Resistor R1, capacitor C1, and diode D1 slow the voltage rise to enable the collector current to fall to zero before the collector voltage has risen above the supply voltage V_S (Figure 8). Typical values of capacitor C1 are 1.5nF per Amp. of collector current.

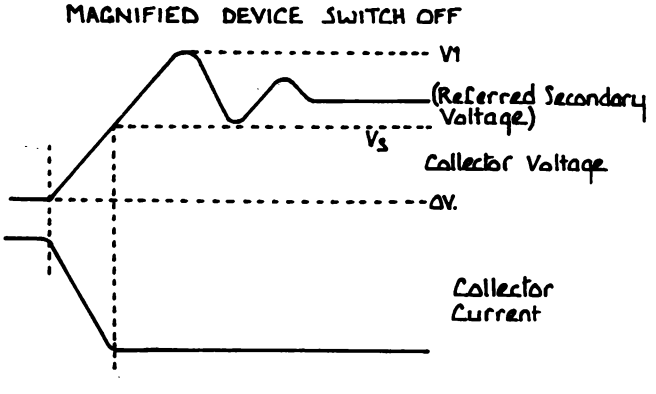
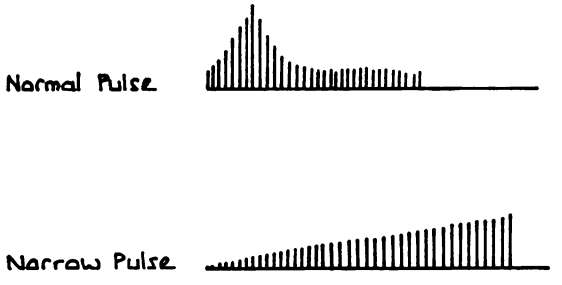


FIGURE 8

Supply Start Up

During the initial supply start-up the conduction time of transistor VT1 should be as short as possible. The reasons for this are as follows:–

(i) A small pulse width at the supply start-up gives a gentle rise of the output voltage with no over-shoot.



COLLECTOR CURRENT AT START UP
FIGURE 9

(ii) The peak current that transistor VT1 experiences is very much reduced (Figure 9).

(iii) Drive and voltage levels in the control circuits are given time to stabilise.

Large pulse width "start-ups" could cause the devide VT1 to come out of saturation and also possibly cause saturation of transformer T1.

An alternative is to rely on the current limit circuit. The voltage developed across resistor R2 provides collector current sensing. If this current exceeds a preset value the pulse width can be made to reduce itself and hence the peak collector current (dynamic current limiting). The maximum modulation capability of the pulse width modulator should be of the order of 50% of the total period. This again reduces possible stress on the transistor VT1.

Selection of Transistor VT1

(a) The device could be operating (i.e. conducting) when $V_{CE} = V_S$ and hence $BV_{CER} \geqslant V_S$ (maximum).

(b) The leakage inductance of transformer T1 causes a voltage overswing of V'. This voltage V' may be reduced by clamping, damping or improved transformer design. It is necessary that $BV_{CEX} > V'$. I_{CEX} is usually quoted in manufacturers published data, X being the reverse base-emitter voltage which is normally $-2V > X > -8V$.

(c) The forward base drive current should be in the order of $I_{B(on)} = I_{C(max)}/4$ and have a rise time $< 1\mu s$. The reverse base drive current is normally arranged to be $I_{B(off)} = 0.75\ I_{B(on)}$. Under these conditions the collector current fall time will be less than $1\mu s$.

PUSH–PULL SHUNT CHOPPER POWER SUPPLIES

In this type of inverter, width modulated pulses are averaged out in a filter to produce a mean D.C. Any variations in the required D.C. output voltage are compensated by increasing or decreasing the pulse widths. A block diagram of this type of power unit is shown in Figure 10 and waveforms are given in Figure 11.

To avoid large currents at device switch on, Filter 2 is usually a "choke-input" type. This is a useful configuration at the transformer's leakage inductance can be considered as part of the filtering system. Hence a very low leakage inductance output transformer is not required as in the case of the single transistor chopper transformer.

Design Considerations

Bridge rectifying the mains will produce an on-load voltage of about 300. Assuming a BUY69B device is to be used running at 8A peak collector current, the following procedure enables an estimate of the output power to be made. Due to the transformer magnetising current some slope on the collector current is inevitable (Figure 11). Assuming this slope to be 2A gives an effective collector current during the device conduction time of $8 - 2 \times 0.5 = 7$A. As the two power devices cannot be allowed to conduct simultaneously a guard space must be left between their conduction periods. If the guard space and width modulation occupy 20% of the available working time the mean effective primary power will be $300 \times 5.6 \cong 1.7$kW. Transformer and secondary rectifier losses will reduce the power output to about1.5kW.

Hence two BUY69B transistors are capable of generating power outputs of 1.5kW and similarly two BUY70B devices could produce 800W.

The major problem with this type of inverter is its load variations. If the load current drops to a very low value the storage time of the switching transistors becomes very long. In the case of the BUY69 2.5A of base drive is necessary to ensure a low saturation voltage at the maximum expected collector current of 8A. When the collector current is low say 1A, the 2.5A base drive will heavily overdrive, the device and the storage time can increase to as much as 10μs. The effect of this pulse lengthening is to cause the secondary rectified output voltage to rise. Several methods are available to overcome this problem. Base current variation with loading, pre-loading the power supply, and emitter current switching are obvious solutions.

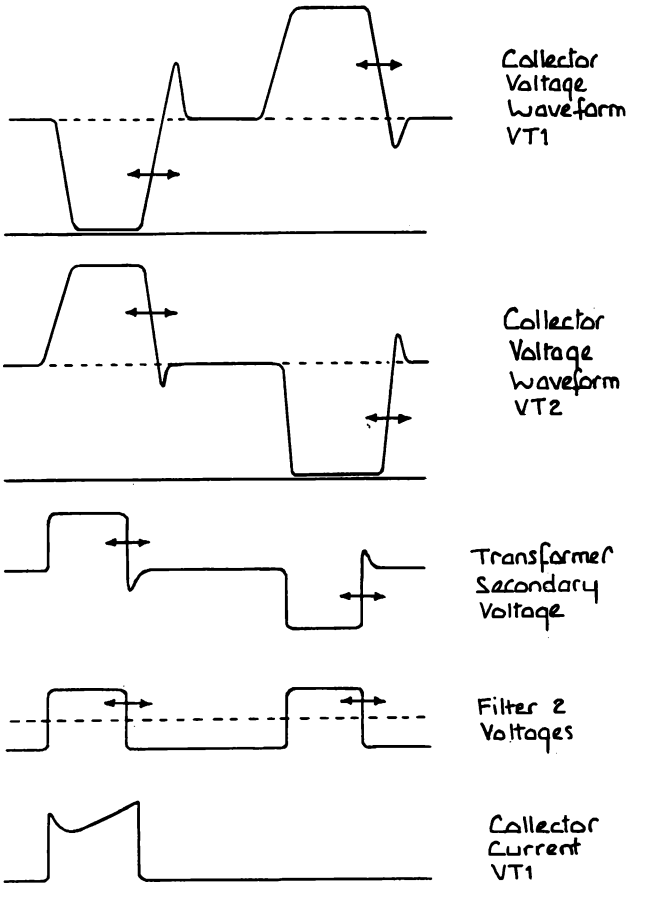


FIGURE 11 CIRCUIT WAVEFORMS

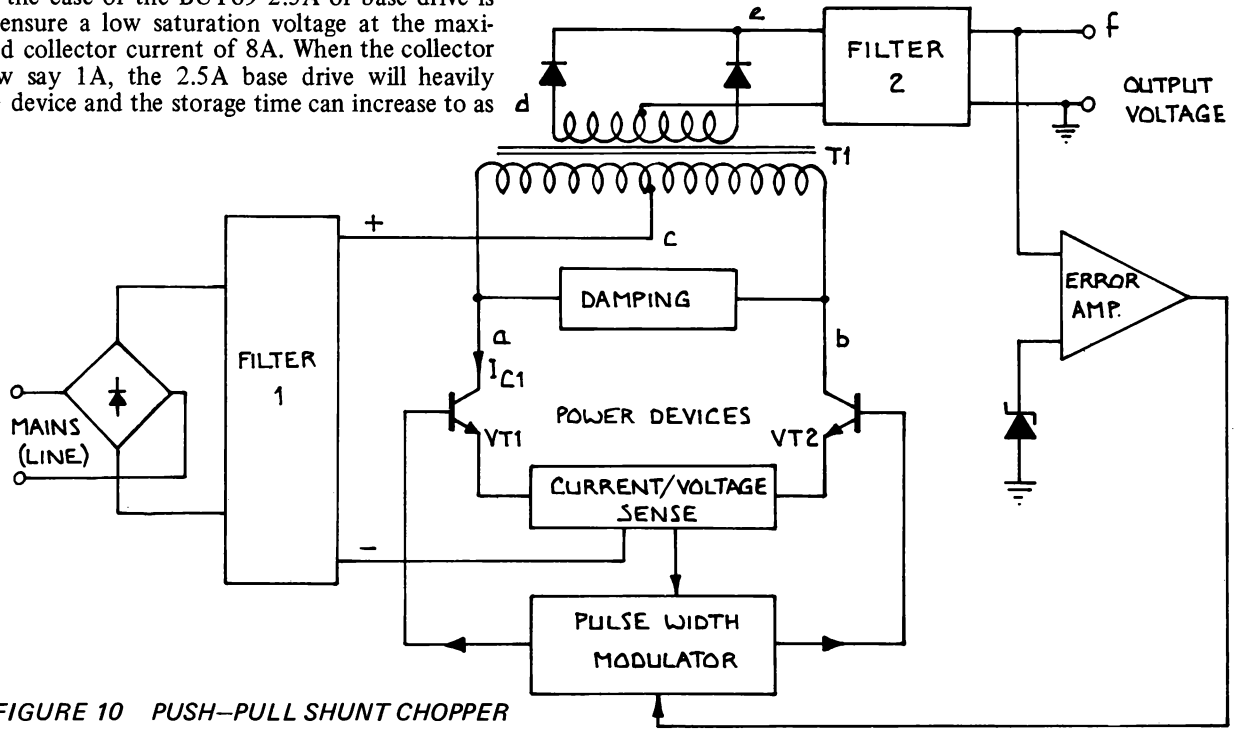


FIGURE 10 PUSH–PULL SHUNT CHOPPER

CONCLUSIONS

The following table summarises the possible output powers from BUY69 and BUY70 transistors operating in chopper power supplies driven directly from rectified mains.

	BUY69 (B) W	BUY70 (B) W
Simple regulated power supply unit	600	300
Regulated and stabilised power supply unit	1000	500
Push-Pull	1500	800

RATINGS OF BUY69 AND BUY70 TRANSISTORS

Absolute maximum ratings (at 25°C ambient temperature)

		BUY69A	BUY69B	BUY69C	BUY70A	BUY70B	BUY70C
Collector-Base Voltage ($I_E = 0$)	V	1000	800	500	1000	800	500
Collector-Emitter Voltage ($-2 > V_{BE} > -8V$)	V	1000	800	500	1000	800	500
Collector-Emitter Voltage $R_{BE} = 10\Omega$)	V	500	400	250	500	400	250
Emitter Base Voltage	V	8					
Collector-Current peak (see Note 1)	A	15					
continuous	A	10					
Base-Current continuous	A	3					
Total Dissipation D.C. ($V_{CE} < 17V$)	W	100			75		
Storage Temperature	°C	−65 to +200					
Operating Junction Temperature	°C	−65 to +200					

NOTE 1 Pulse Width <500 μs Duty cycle <25%

H.V. Stacks, Parallel Operation and System Design
(B118)

H.V. STACS, PARALLEL OPERATION AND SYSTEM DESIGN

By Jurek Budek

1. INTRODUCTION

The introduction of silicon rectifiers gave rise to new ideas in designing high voltage, H.V. power equipments. H.V. silicon rectifier stacks offer the advantages of long life, small size, reliability and low operating costs when compared with thermionic valves. Furthermore, there is no need for the warming up period and heating transformer associated with thermionic valves. The silicon devices used in H.V. assemblies incorporate their own inherent reverse voltage limiting protection. They are of a non-destructive avalanche breakdown type, so that additional protection against excessive voltage transients is not required in the majority of cases. The stacks may be encapsulated in epoxy resin thus giving a rigid construction suitable for mounting either on insulation or metal plates or brackets. For larger powers the stacks can be connected in parallel as discussed later in this report.

The most common application for the large H.V. power supplies are radar, radio transmitters, travelling wave tubes, microwave, inductive and dielectric heating. The circuit most frequently used for the above supplies is the three phase bridge. The design information given in this report, therefore, is for a three phase bridge, together with efficiency and power factor calculation.

2. SERIES OPERATION OF AVALANCHE RECTIFIERS

When connected in series controlled avalanche rectifiers require no shunting resistors to ensure an equal reverse voltage distribution across each element because of their ability to work satisfactorily in the avalanche region.

Figure 1 shows two rectifiers connected in series.

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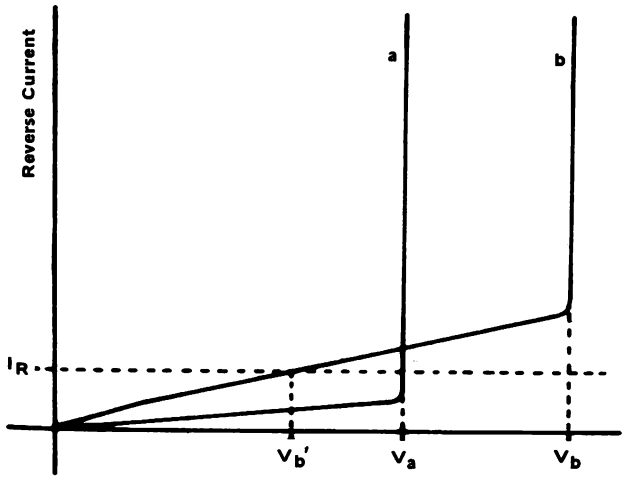


FIGURE 1

For a given reverse voltage supply equal to $V_a + V_b$/ the voltage swing across devices a and b will be as shown in Figure 1. Any increase in reverse voltage will cause an increase in the reverse current and V_b' will increase until the avalanche voltage V_b is reached. Providing that the total voltage applied to both diodes in series is less than the sum of the two avalanche voltages, i.e.$(V_a + V_b)$ the value of reverse current I_R will remain low well within the rating of the devices.

Conventional rectifiers need shunting resistors for steady state voltage sharing and also capacitors for transient voltage sharing. As avalanche rectifiers have an inherent capability of absorbing reverse power, there is no need for shunting capacitors. In a normal design there will be sufficient reverse power capability existing in diodes connected in series to cope with any transients generated by switching "on" and "off" of most of their equipment transformers.

Manufacturers' data sheets provide information on the reverse power rating. The voltage transient energy can be evaluated from the magnetic energy stored in the transformer core. A simple comparison of these quantities will allow the suitability of the devices to be checked.

3. PARALLEL OPERATION OF HIGH VOLTAGE STACKS

When running H.V. stacks in parallel two points must be considered : load sharing at the nominal load and load sharing during fault conditions.

Typical forward voltage characteristics are shown in Figure 2. The slopes of the minimum and maximum curves are approximate only. (In fact, they curve slightly so that an increase of current does increase the forward voltage drop.) If two diodes are connected in parallel, one having a maximum and the other a minimum forward voltage drop, V_f, Figure 2 shows that at 1.0V forward drop, one diode will take 10A and the other only 6.5A. This unbalance will increase at lower currents, i.e. at 0.8V across two diodes connected in parallel, one diode will take 5A, but the other only 2.5A. Paralleling up strings of diodes will lessen the unbalance; the greater the number of diodes in series, the less inequality.

Several tests were carried out on three strings of devices connected in series. Each string consisted of 20 avalanche diodes, type 1AS029. Table 1 gives a summary of the results. The current measured is the peak current of a 50Hz half sine wave. "Percentage above mean" figures were obtained from the formula:–

$$(B - M)100/M \ \%$$

where B is the highest current of a string.
and M is the total current divided by 3,
i.e. ideally shared current per string.

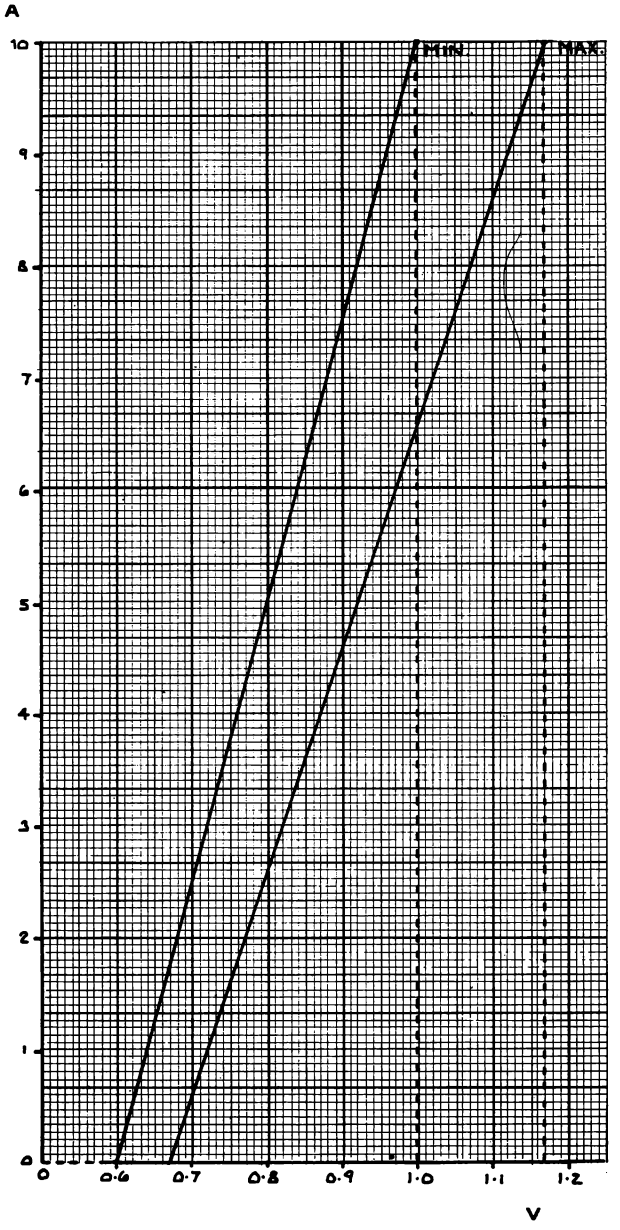


FIGURE 2

In practice, it can be expected that one or two diodes may become short circuit. This can arise as a result of the faulty manufacture of a diode. Alternatively, there might be a mismatched junction capacitance, a device with a soft characteristic or poor avalanche reverse power capability.

Total	'a'	'b'	'c'	Percentage above mean	Remarks
14.5	5	4.5	5	2.1	
36.5	12.5	11.5	12.5	2.9	
69.5	23.5	22.5	23.5	1.7	
83.9	28.7	27.6	27.6	3.1	
124.2	41.4	41.4	41.4	0	
142.5	47.5	47.5	47.5	0	
162	54	54	54	0	
21	8.5	6.0	6.5	21.5	One diode is short
59.5	22.5	18.0	19.0	12.5	circuited in string
89.7	32.5	28.6	28.6	8.3	'a'
123.7	43.7	40	40	6.1	
135.0	50	47.5	47.5	3.6	
18.5	6.5	6.0	6.0	4.8	One diode is short
39	13.5	12.5	13.0	3.8	circuited in string
63.5	21.5	21.0	21.0	2.4	'a' and 0.8Ω resis-
86	30	28.5	27.5	4.3	tors are added to
107	36	36	35	1.4	each string.
145	48.8	48.7	47.5	1.1	
22	10.5	5.5	6.0	44	Two diodes are
55	22.5	16.0	16.5	20.3	short circuited in
77	31.0	22.5	23.5	20.0	string 'a'
107	41.0	32.5	33.5	15.4	
141	52.4	43.6	45	11.6	
16	6.5	4.5	5	21.4	Two diodes are
39.5	14.0	12.5	13.0	6.6	short circuited in
62	21.5	20.5	20	4.1	string 'a' and 0.8Ω
74.5	26.0	25.0	23.5	5.3	resistors are added
119.5	41.0	40.0	38.5	3.1	to each string
147.5	50	50	47.5	1.8	

Table 1

Table 1 shows, therefore, load sharing between strings with one string having one or two diodes short circuited, i.e. 5% or 10% loss of diodes in one string. Some sort of external forced load sharing must be then introduced as the unbalance between strings in such a case becomes unacceptable. An 0.8Ω series resistor, connected with each string gives a satisfactory result for this particular example. As guidance, a series resistor, R_S, which will dissipate 10% of the diode losses, should be used with each string of diodes. For example, a 1AS029 diode is rated at 1.5A average with a typical forward voltage drop 0.87V. Total power dissipation in a 20 diode string will be 20 x 0.87 x 1.5 = 26W. The series resistor then will be $R_S = 2.6/1.5^2 = 1.15\Omega$; Resistor R_S compensates for the unbalance caused by the loss of 10% of diodes in one string. For less than 10 diodes in series, the value of the series resistor should be increased.

To illustrate an unbalance between various strings some current traces were recorded and are shown in Figure 3. The effect of an 0.8Ω series resistor is quite noticeable.

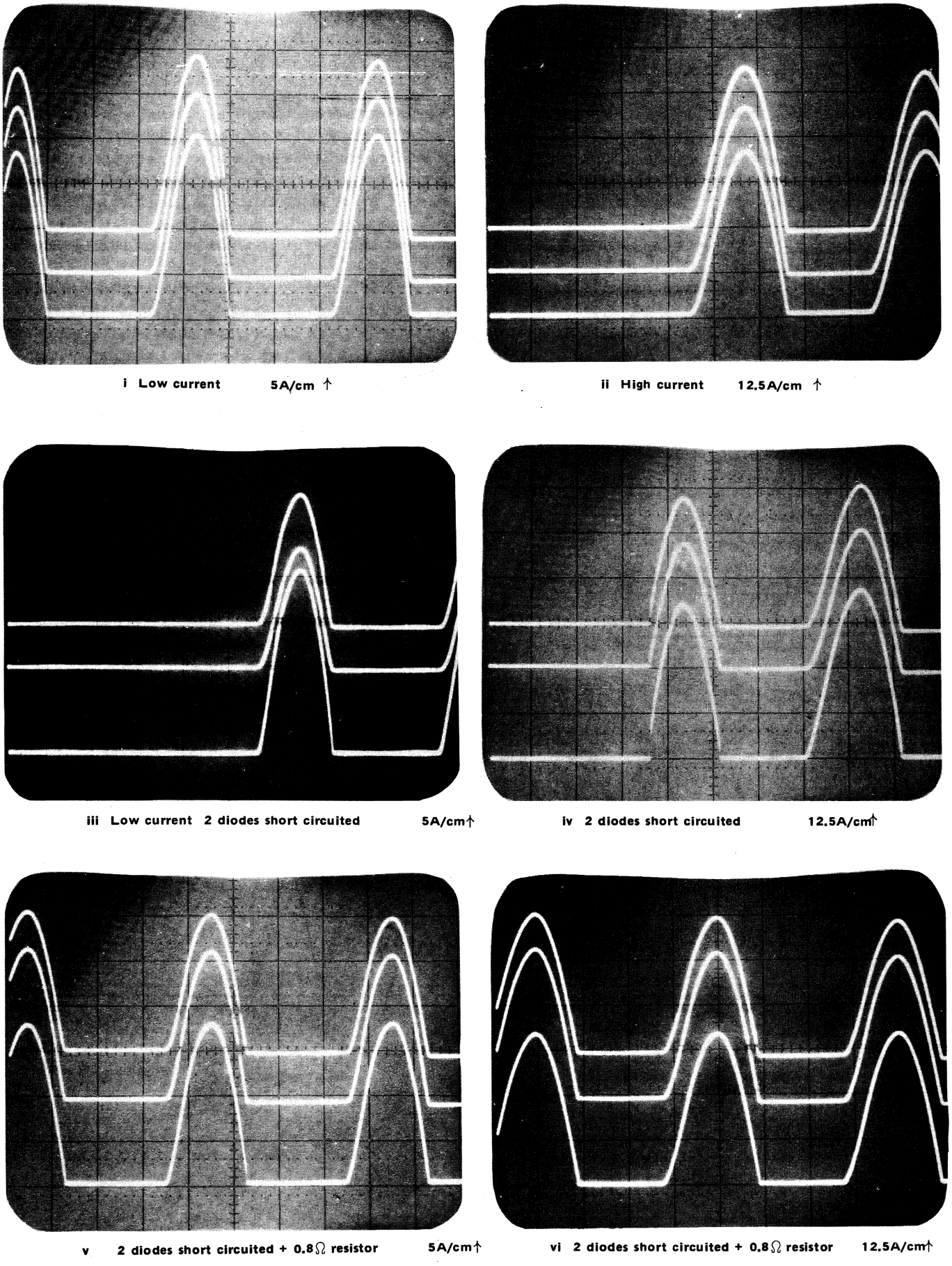

i Low current 5A/cm ↑
ii High current 12.5A/cm ↑
iii Low current 2 diodes short circuited 5A/cm↑
iv 2 diodes short circuited 12.5A/cm↑
v 2 diodes short circuited + 0.8Ω resistor 5A/cm↑
vi 2 diodes short circuited + 0.8Ω resistor 12.5A/cm↑

FIGURE 3 Waveforms of fault current through 20 diode H.V. stacks

4. THREE PHASE BRIDGE DESIGN

4.1 Theory *Ref. 1

One of the most common connection for H.V. power conversion is a three phase bridge (See Figure 4) where the transformer and silicon rectifiers capabilities are fully utilised.

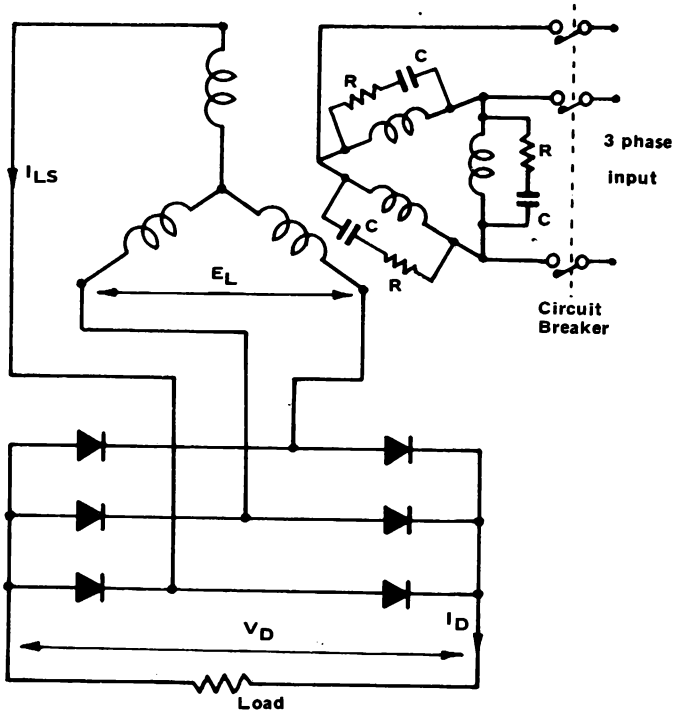


FIGURE 4

The following design information is based on what is known as the "Infinite Reactance Theory", It assumes that each pulse of current is rectangular in form as though a reactance of infinite value is in the D.C. output circuit. It shows good correlation with practical results in poly-phase rectifier circuits, but is less accurate in single phase circuits because of an increasing departure from the assumed idealised waveform.

High power circuits, employing semiconductors, invariably use a certain amount of reactance to provide fault current limitation. In most cases the reactance values vary between 5% and 10%. The voltage drop, caused by the reactance, cannot be ignored and must be taken into account for accurate circuit design. As the current waveforms in rectifier circuits are not therefore sinusoidal it would be rather difficult to establish the correct voltage loss due to the presence of reactance. "Infinite Reactance Theory" offers a solution to this problem. An overlap angle present in rectifier circuits and proportional to the a.c. reactance causes a reduction in D.C. voltage output which can be calculated, See Figure 5. The voltage drop occurs only during the period of overlap and it is this feature which is the main difference between this method and the orthodox design calculations. In the latter the a.c. reactance is neglected as it is considered to be too small to make any appreciable difference, or calculated as an a.c. input drop.

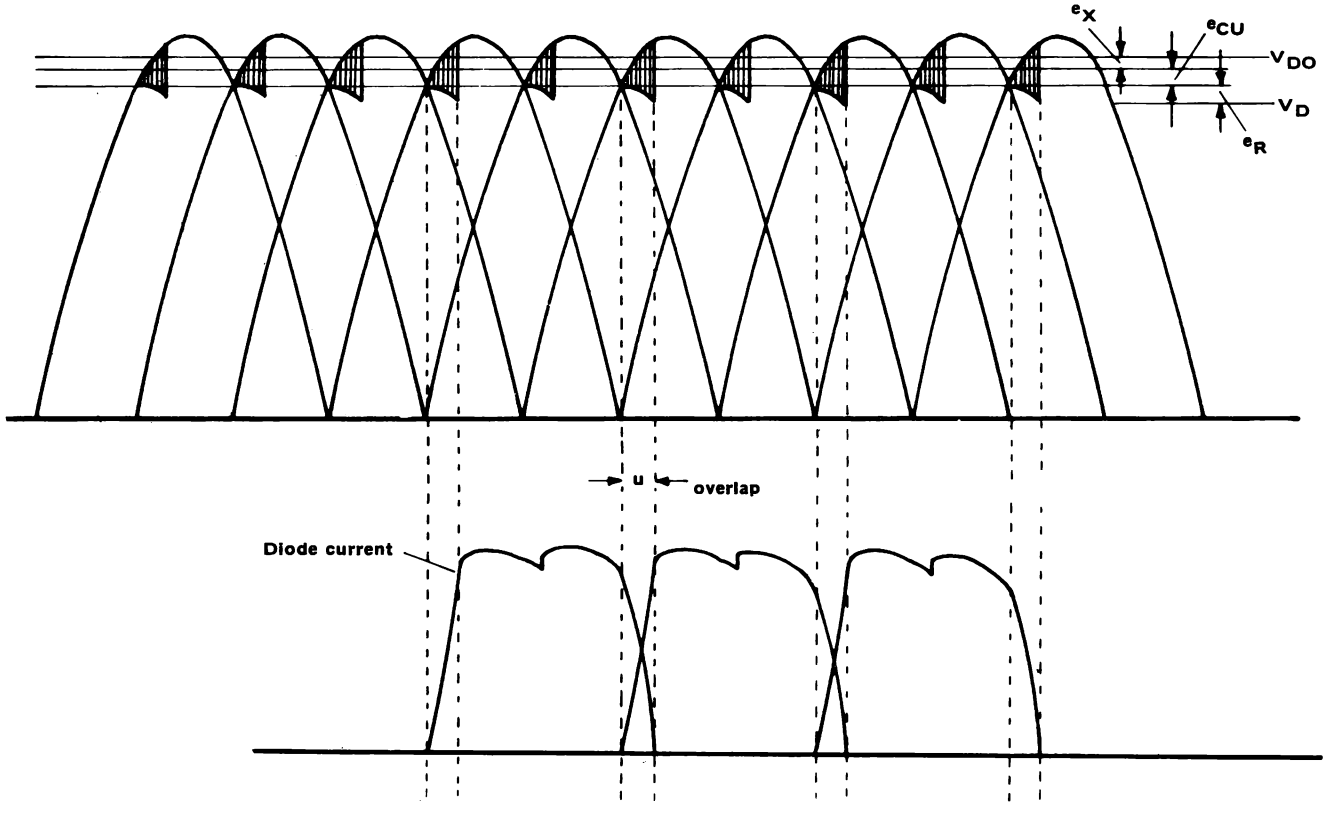


FIGURE 5

(a) Circuit Design

The following equation must be satisfied:–

$$V_{DO} = V_D + e_x + e_R + e_{CU} \quad \ldots\ldots (1)$$

where

V_{DO} = theoretical no load D.C. voltage

V_D = Full load D.C. voltage

e_X = D.C. reactive voltage drop (during commutation) due to the presence of transformer leakage reactance and supply reactance.

e_R = D.C. voltage drop (total) in the rectifiers.

e_{CU} = D.C. voltage drop due to the presence of resistance in the circuit, including copper loss

Now

$$e_X = (X_T + X_S).\ V_{DO}/200 \quad \ldots\ldots (2)$$

where X_T = percentage transformer reactance referred to the primary kVA

e_{CU} = total circuit power loss due to resistance/I_D ... (3)

where I_D = D.C. current in amps at full load.

From equation (1) and (2) V_{DO} can be determined.

$$V_{DO} = (V_D + e_R + e_{CU})/[1 - (X_T + X_S)/200] \quad \ldots\ldots (4)$$

$$E_{L0} = V_{DO}/1.35 \quad \ldots\ldots (5)$$

where E_{L0} = Secondary r.m.s. voltage between lines at no load.

$$I_{LS} = I_D \times 2^{1/2}/3^{1/2} \quad \ldots\ldots (6)$$

where I_{LS} = rectifier transformer secondary RMS line current

Primary transformer rating = secondary transformer rating = $1.05 \times I_D \times V_{DO}/1000$ kVA ..... (7)

4.2. Fault Current *Ref. 2

The fault current has been assumed to be limited only by the leakage reactance of the transformer and supply. When switching on to a fault condition, it can be observed that the first pulse of the current is larger than that of the steady state short circuit. This is due to the asymmetry (asymmetrical pulse) caused by the presence of a reactance. The amplitude of the asymmetrical pulse depends on the ratio R/X of the system and can be established from Figure 6.

It can also be seen from Figure 6 that the maximum asymmetrical pulse can be double the peak value of steady state short circuit current for an a.c. infinite reactance system. For practical purposes, account must be taken of an asymmetrical pulse when dealing with up to, for instance, only 3 or 4 pulses. In longer periods the steady state pulses will swamp the effect of the asymmetrical pulse.

$$I_{SC} = I_D \times 200/3^{1}/^{2}\ (X_T + X_S) \ldots\ldots\ldots\ldots\ldots (8)$$

where I_{SC} is short circuit peak current.

4.3 Efficiency

The accepted way of calculating efficiency in larger equipments is by a summation of losses.

$$\text{Efficiency} = \eta = (1 - \text{losses}/(\text{power output} + \text{losses})]\ 100\% \quad \ldots\ldots\ldots (9)$$

In calculating the efficiency the losses of the transformer, rectifier and auxiliaries should be included. The losses in the rectifier diodes will depend upon the overall load current and will be equal to:–

$$P_R = I_D \times 2 \times V_F \times n \ldots\ldots\ldots\ldots\ldots\ldots (10)$$

where

P_R = total rectifier losses in the three phase bridge

V_F = forward voltage drop across one diode at current, I_D

n = number of diodes connected in series

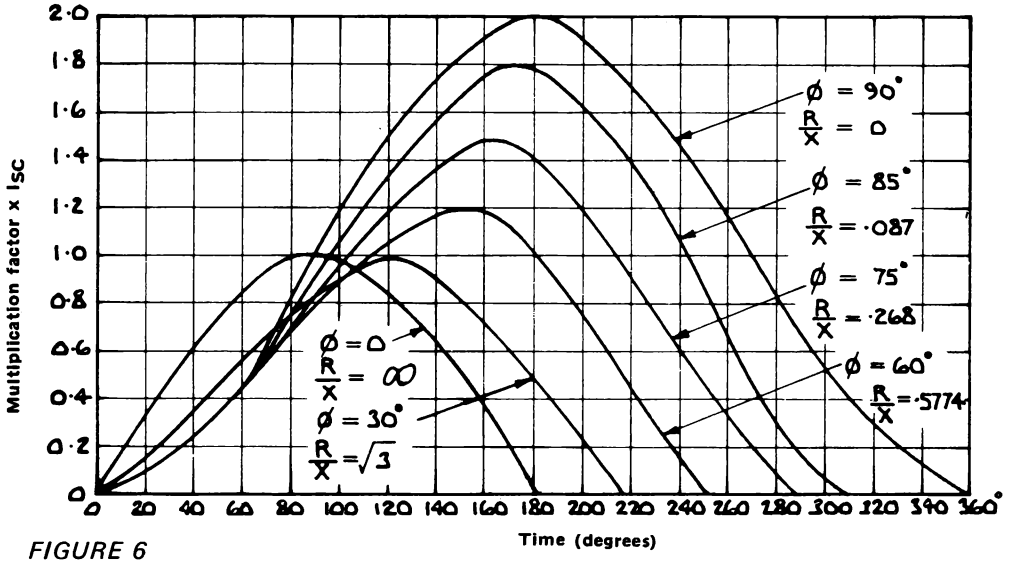


FIGURE 6

4.4 Power Factor

For practical purposes the only important value of the power factor of the current drawn from the supply is the power factor of the fundamental or cos ϕ, where ϕ is the angle by which the fundamental component of current lags the supply voltage. It is this value that will be measured by instruments. The total power factor is the product of the displacement factor (due to the fundamental) and of the distortion factor (due to the harmonics), the latter of theoretical interest only.

The evaluation of the power factor depends upon the following relationship :

$$\cos u = 1 - 2e_X/V_{DO} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (11)$$

$$\tan \phi_1 = (u - \sin u \cos u)/\sin^2 u \quad \ldots\ldots\ldots\ldots \quad (12)$$

where u is the angle of overlap (See Figure 5)

From the value of tan ϕ_1, cos ϕ_1 can be ontained and by applying this to the curves of Figure 7 for varying amounts of percentage magnetising current, the power factor of the fundamental cos ϕ can be established. The magnetising current taken represents a percentage of the full load primary current. If, therefore, the power factor is to be calculated for any other load current, it must be remembered that the magnetising current percentage must now be based on the new primary current. For example, if the full load magnetising current is taken as 5%, the magnetising current percentage at half the primary current would become 10%.

In the case of e_X, the D.C. reactive volt drop, this will be directly proportional to I_D, the output current.

4.5 Protection

To ensure the satisfactory operation of equipment using semiconductor devices the problem of protection against possible excessive voltage transients and excessive currents must be solved. In section 2, the capabilities of avalanche diodes to absorb large powers in the reverse direction was discussed. Therefore, for normal applications of H.V. stacks, there is no need for further steps to be taken. However, in some cases, when frequent switching is taking place, e.g. induction or dielectric heating, a simple CR network, connected across the primary windings of the transformer will help to suppress excessive voltage transients. Recommended values for voltage transients suppression are shown below and connections are given in Figure 4.

$$C = 350 I_M/E_p \ \mu F \ldots\ldots (13)$$

$$R = 100/C \ \Omega \ldots\ldots\ldots (14) \quad \text{assuming a 50Hz supply}$$

where I_M is the magnetising current in amps.
and E_p is the primary supply line voltage.

Surge currents are easier to evaluate than voltage transients and they can be controlled by a circuit design as described in section 4.2. By choosing the correct value of transformer leakage reactance, the peak fault current can be kept below a safe value for the devices. Circuit breakers, contactors and fuses are normally used to protect semiconductor equipments against overloads and short circuits. Contactors, not having fault breaking capabilities, are normally backed up by fuses. Circuit breakers, however, do not require fuses. In order to withstand an inrush current to a transormer, the fuses in the input side of the transformer are usually rated at twice or three times the nominal current. Therefore, protection against the D.C. faults becomes more difficult. On the other hand, the fuses on the secondary side of the transformer may be rated very near to the full load current. This is not always convenient, especially for H.V. equipments, as the fuses become rather expensive. When fuses or breakers are adapted for the protection of silicon devices, correct discrimination can be achieved by keeping below the rectifier overload curve at every point by either fuse or breaker characteristics. A knowledge of i^2t (let through energy) values is very useful in cases when a fault current is expected to be interrupted within ten milliseconds. In this time interval, the i^2t can be assumed to be approximately constant. A simple comparison of the rectifiers i^2t with total fuse i^2t will give the rating of the fuse needed. *2.

5. PRACTICAL EXAMPLE

5.1 Rectifier Transformer

Requirements : – Rectifier power equipments to deliver 10A at 12kV, i.e. 120kW for an induction heating load.

$I_D = 10A$
$V_D = 12kV.$

Let us assume $X_T = 7\%$ and $X_S = 1\%$

From equation (8) $I_{SC} = 10 \times 200/3^{1}/^{2} \times 8 = 145A.$

Assuming the copper loss =2%, i.e. 2 x 120/100=2.4kW

The ratio of the percentage of equivalent resistance due to the copper losses to the total percentage reactance (i.e. 2/8 = 0.25) gives the multification factor for obtaining peak asymmetrical current from Figure 6 which here is 1.5.

Therefore, the peak asymmetrical current is 145 x 1.5 218A.

Connecting 3 x 1.5A H.V. stacks in parallel will give, including a 10% unbalance, 218 x 1.1/3 = 80A per stack, which is well within the surge rating of a 1AS029 avalanche rectifier.

It is now necessary to find the theoretical no load D.C. voltage, V_{DO}.

Considering a stack consisting of 20 avalanche diodes connected in series with say, 1.0V drop per diode,

$e_R = 2 \times 20 \times 1 = 40V.$

$e_{CU} = 2400/10$ from equation (3)
$= 240V$

$\therefore V_{DO} = (12,000 + 40 + 240)/[1 - (7+1)/200]$ from equation (4)
$= 12800V$

Check:

$e_X = (7 + 1) \times 12800/200$ from equation (2)
$= 512V$

$\therefore V_{DO} = 12000 + 512 + 40 + 240$ from equation (1)
$= 12792$, i.e. 12800

Note that the D.C. reactive voltage drop $e_X = 512V$ which cannot be ignored when designing rectifier equipments.

Now then other transformer details can be found.

$E_{L0} = 12,800/1.35 = 9,500V$ From equation (5)

$I_{LS} = 10 \times 2^{1/2}/3^{1/2} = 8.2A$ From equation (6)

Rating of the transformer $= 1.05 \times 10 \times 12,800/1000$
$= 134.4kVA$ From equation (7)

Check

Rating of the transformer is also $= 3^{1/2} \times E_{L0} \times I_{LS}/1000kVA$
$= 3^{1/2} \times 9,500 \times 8.2/1000$
$= 135kVA$

The specification for the transformer can now be written

Connections:–	delta/star
Primary supply	440V, 3 phase, 50Hz
Secondary open circuit line voltage	9500V
Secondary full load current	8.2A rms
Leakage reactance	7%
Assumed copper losses	2.4kW
Ambient temperature	30°C

Figure 8 shows the D.C. voltage regulation of the equipment.

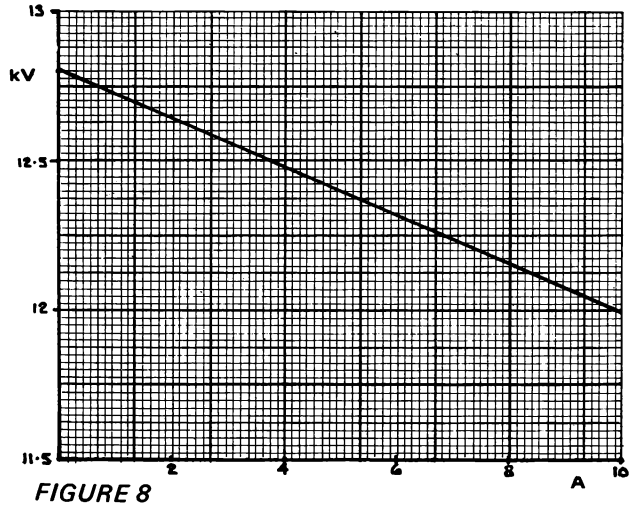


FIGURE 8

5.2 H.V. Stacks

There are two points for consideration in selecting rectifiers, i.e. the voltage and current ratings. The maximum peak voltage expected from the transformer is $9500 \times 2^{1/2} \times 1.1 = 14800V$, assuming a 10% rise in supply voltage. Allowing 35% above this figure for safety, stacks capable of withstanding 20kV will be needed. Twenty avalanche rectifiers, type 1AS029, rated at 1000V each and connected in series are well suited for this application.

The current rating of 1AS029 devices has been partly discussed in section 5.1. First, the asymmetrical peak current expected during a fault is 80A and the nominal current per stacks is $10 \times 1.1/3 \times 3 = 1.22A$ mean both inside the rating of 1AS029 devices. Normally, equipments of this power would have a circuit breaker in the input to the transformer to cope with any overloads or fault currents. The speed of operation of an a.c. circuit breaker is about 60ms, i.e. 3 cycles in a 50Hz system. Taking into account the safety factor, the stacks should be capable of withstanding the fault current for at least 5 cycles, i.e. 100ms, In our example the value of the steady state fault current is $145 \times 1.1/3 = 54A$. allowing 10% for unbalance. This value is again within the rating of the devices. As discussed in section 3, a loss of the devices. will necessitate an additional series resistor connected to each stack. The value of this resistor can be evaluated from:–

$R_S = 20 \times 0.875/10 \times 1.5 = 1.17\Omega$ say 1.2Ω ....(.. see section 3)

Summing up:–

Three H.V. stacks will be connected in each arm of a three phase bridge giving a total of 18 stacks.

A 1.2Ω series resistor is added to each stack.

Each stack will consist of 20 1AS029 avalanche rectifiers.

5.3 Efficiency

From equation 10

$P_R = 10 \times 2 \times 1.0 \times 20 = 0.4kW$

As the copper losses are $= 2.4kW$

The total losses $= 2.8kW$

$\therefore$ From equation (9) $\eta = [1 - 2.8/122.8]\,100\%$

$= 97.7\%$ at full load

Total losses at half load $= (0.4/2) + (2.4/4) = 0.8kW$

Approximately D.C. voltage at half load $= 12000 + 800/2$
$= 12400V$

See Figure 8

The output power at half load $= 12400 \times 5/1000 = 62kW$

$\therefore$ Efficiency $= [1 - 0.8/62.8]\,100\% = 98.7\%$ at half load

5.4 Power Factor

From equation (11) $\cos u = 1 - 2 \times 512/12800 = 0.916$

$\therefore u = 23^{o}\ 36 = 0.413$ rad

From equation (12) $\tan \phi_1 = (0.413 - 0.4 \times 0.916)/0.16 = 0.3$

$\therefore \phi_1 = 17^{o}$

$\cos \phi_1 = \cos 17^{o} = 0.956$

Assuming the magnetising current = 2.5%, from Figure 7, $\cos \phi$, the displacement factor, is 0.95 at full load.

At half load:–

$\cos u = 1 - 2 \times 256/12800 = 0.959$

$u = 16^{o}\ 24' = 0.286$ rad

$\tan \phi_1 = (0.286 - 0.282 \times 0.959)/0.282 = 0.2$

$\phi_1 = 11^{o}\ 24'$, $\cos \phi_1 = 0.98$

and from Figure 7 $\cos \phi = 0.97$ (the magnetising current for half load is 5%)

5.5 Protection

As the equipment is supplying an inductive heating load an R.C. network connected in the primary winding of the transformer has been added.

The primary current

$I_P = 134.4 \times 1000/3^{1/2} \times 440 = 176$A

$I_M = 2.5 \times 176/100 = 4.4$A

$C = 350 \times 4.4/440 = 3.5\,\mu$F From equation (13)

and the series resistor

$R = 100/3.5 \simeq 28.5\,\Omega$ From equation 14

As discussed in section 5.2, the stacks selected for the equipment are within their capabilities for the first asymmetrical pulse, as well as for the steady state short circuit current for the time of 100ms. The circuit breaker selected must be able to open at up to 60ms to give a sufficient safety margin for satisfactory generation.

6. CONCLUSIONS

H.V. stacks, using series connected avalanche rectifiers, have already proved themselves in practice to be reliable and efficient. However, users have been reluctant to accept, for large outputs, the paralleling of H.V. stacks. This report attempts to justify paralleling by giving some guidance as to how this can be done and give satisfactory operation.

The result of the tests showed that even allowing for a loss of 10% of the diodes in one string, a reasonable balance of current in various strings can be achieved by adding suitable series resistors.

7. REFERENCES

1. The Calculations of Rectifier and Inverter Performance Characteristics, by J.C. Read, I.E.E. Proceedings 1945.

2. Protective Methods for Silicon Rectifier Equipment, by J.A. Budek and A.H. Marchant, Direct Current Nov. 1964.

HIGH VOLTAGE RECTIFIERS

DEVICE TYPE	PEAK REPETITIVE REVERSE VOLTAGE V_{RRM}	AVERAGE RECTIFIED FORWARD CURRENT A	PEAK SURGE CURRENT 1 cycle at 50Hz	PEAK SURGE CURRENT 5 cycles at 50Hz	MAX.REVERSE LEAKAGE CURRENT AT V_{RRM}
1S150R06	6kV	1.5	80	50	2μA
1S150R08	8kV	1.5	80	50	2μA
1S150S10	10kV	1.5	80	50	2μA
1S150S12	12kV	1.5	80	50	2μA
FO69	16kV	2.5	80	50	2μA

STACKS CAN BE SPECIALLY BUILT TO INDIVIDUAL REQUIREMENTS. CONTACT PRODUCT MARKETING, BEDFORD.

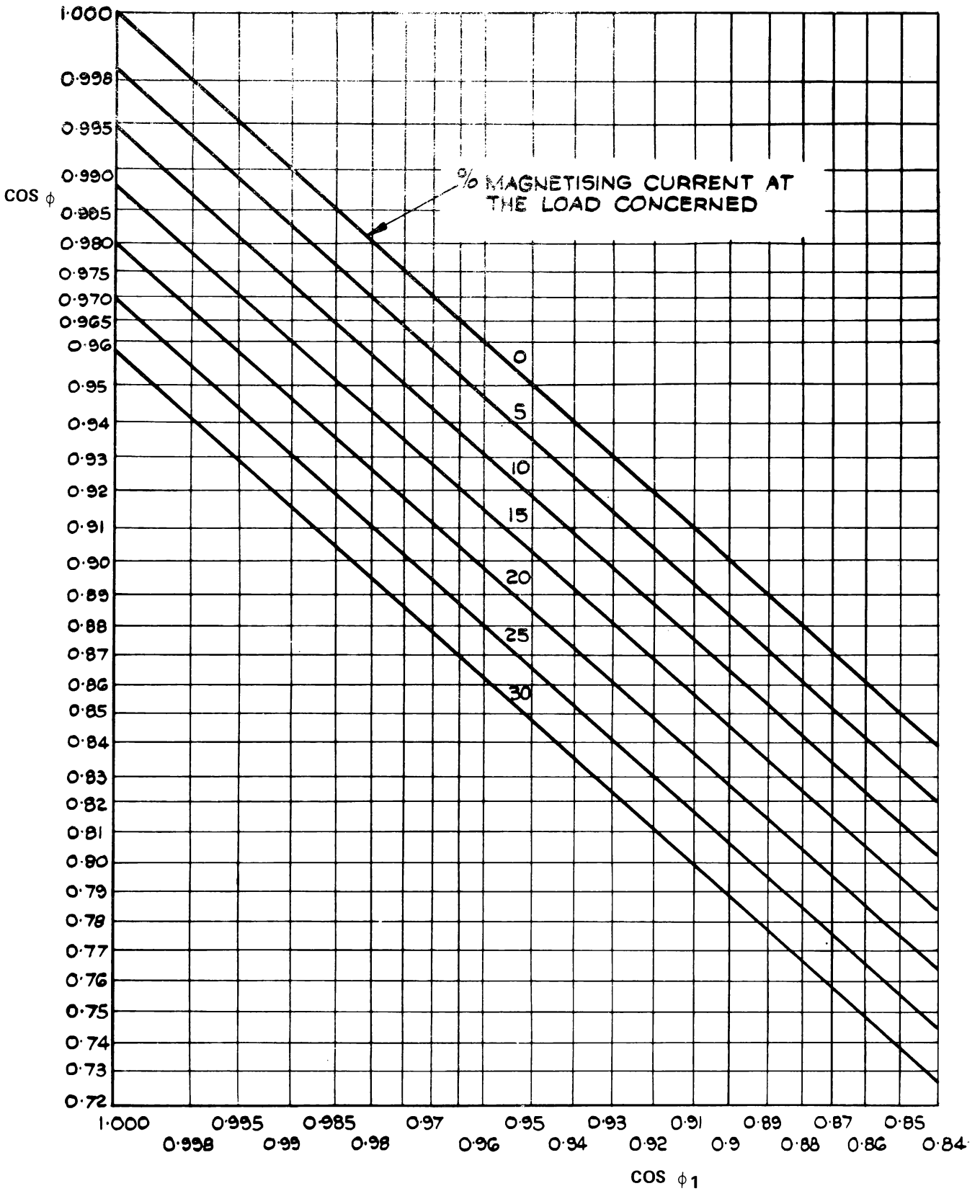


FIGURE 7 **EFFECT OF MAGNETISING CURRENT ON COS φ**

MOS FET
FM Tuner Design
(CA 164)

MOSFET FM TUNER DESIGN

By
Richard Klein & Glen Coers

INTRODUCTION

Dual-gate MOSFETs in an FM tuner provide many advantages over bipolar, junction field-effect, and single-gate MOS field-effect transistors. RF amplification and mixing are aided by use of a low-feedback-capacitance transistor with low noise figure and large dynamic range. A second gate is available for either AGC or local oscillator injection. High, stable RF and conversion gains are easily obtained with inexpensive, commercially available coils and without need for neutralization. This report presents test data and design tips which can be used to design with the *3N201 dual-gate MOSFET at 100 MHz. The 3N201 is an N-channel, depletion mode, dual-gate, MOS transistor with integral back-to-back zener diodes between both gates and the source to eliminate the need for special precautionary handling procedures.

100-MHz RF AMPLIFIER

DC CONSIDERATIONS

Figure 1 shows some typical 3N201 device data. It is noted in Figure 1c that for the highest Gate-1-to-drain transconductance, Gate-1-to-source (V_{G1S}) voltage should be 0.5 volts. Figure 1e indicates nearly flat transconductance for Gate-2-to-source voltage (V_{G2S}) of 4 volts and above. (A resistance should be placed in series with Gate 2 to limit excessive gate zener current caused by accidental application of V_{G2S} voltages above the typical internal zener voltage of ±12 volts.) To insure that the device is operated within its rated 450 mW, V_{G1S} should not exceed 0 volts with V_{G2S} = 4 volts and a 15-volt supply voltage. Operation of the device at I_{DSS} or V_{G2S} = 4 volts, V_{G1S} = 0 volts, V_{DS} = 15 volts, and T_A = 25°C, will be discussed later.

Biasing the MOSFET at I_{DSS} may pose a power supply regulation problem. From Figure 1g, a unit-to-unit total spread of from 5 mA to 30 mA can be expected. This high current can be the cause of some troublesome ground loops and unwanted oscillator pulling with AGC action. A suitable solution is the use of self-bias. Superimposed onto Figure 1g is a load line drawn to represent a 270-ohm source resistor and a 1.3-volt Gate-1-to-ground voltage. The obvious purpose of this combination is to reduce the steady-state bias current variation from 25 mA to 5 mA and to bias the typical I_{DSS} device at 1/2 I_{DSS}.

*3N201 is a special device fabricated by Texas Instruments Incorporated, Dallas, Texas.

GAIN AND STABILITY CONSIDERATIONS

The typical 3N201 100-MHz parameters are shown in Figures 1a through 1c. The reverse transfer admittance is too small to measure on the General Radio admittance bridge. Instead, a Boonton capacitance bridge was used to measure the 1-MHz reverse transfer capacitance, C_{rss}. Further inspection of this data reveals that at 100 MHz the input and output conductances are too small to measure accurately. This makes an accurate design on paper very difficult, if not impossible, to prepare. Some insight can, however, be acquired on the problem of gain and stability by making the following assumptions (see Figures 2 and 3):

1) $Y_{rs} = j\omega$ (C_{rss} + stray cap.) = 0.022 mmho
2) $Re(y_{is}) << G_s'$ (source conductance)
3) $Re(y_{os}) << G_L'$ (load conductance)
4) $G_s' = 1$ mmho
5) $|Y_{fs}| = 12$ mmho

Here it is assumed that the input conductance of the device is $Re(y_{is})$ and the output conductance is $Re(y_{os})$ as in the case of no feedback, Y_{rs}. A source conductance of 1 mmho was chosen to offer the best device noise figure, voltage gain from the antenna, and some mismatch to reduce skewing with AGC action. Tests have shown the device noise performance to be excellent for R_s' ranging *from 1 kΩ to 2 kΩ*. Care must be taken to shield the input circuitry from the output circuitry.

A figure of merit which can be used to estimate stability is defined by Stern[1]:

$$K = \frac{2\,(g_{11} + G_S)\,(g_{22} + G_L)}{|Y_{12}\,Y_{21}| + Re\,(Y_{12}\,Y_{21})} \qquad (1)$$

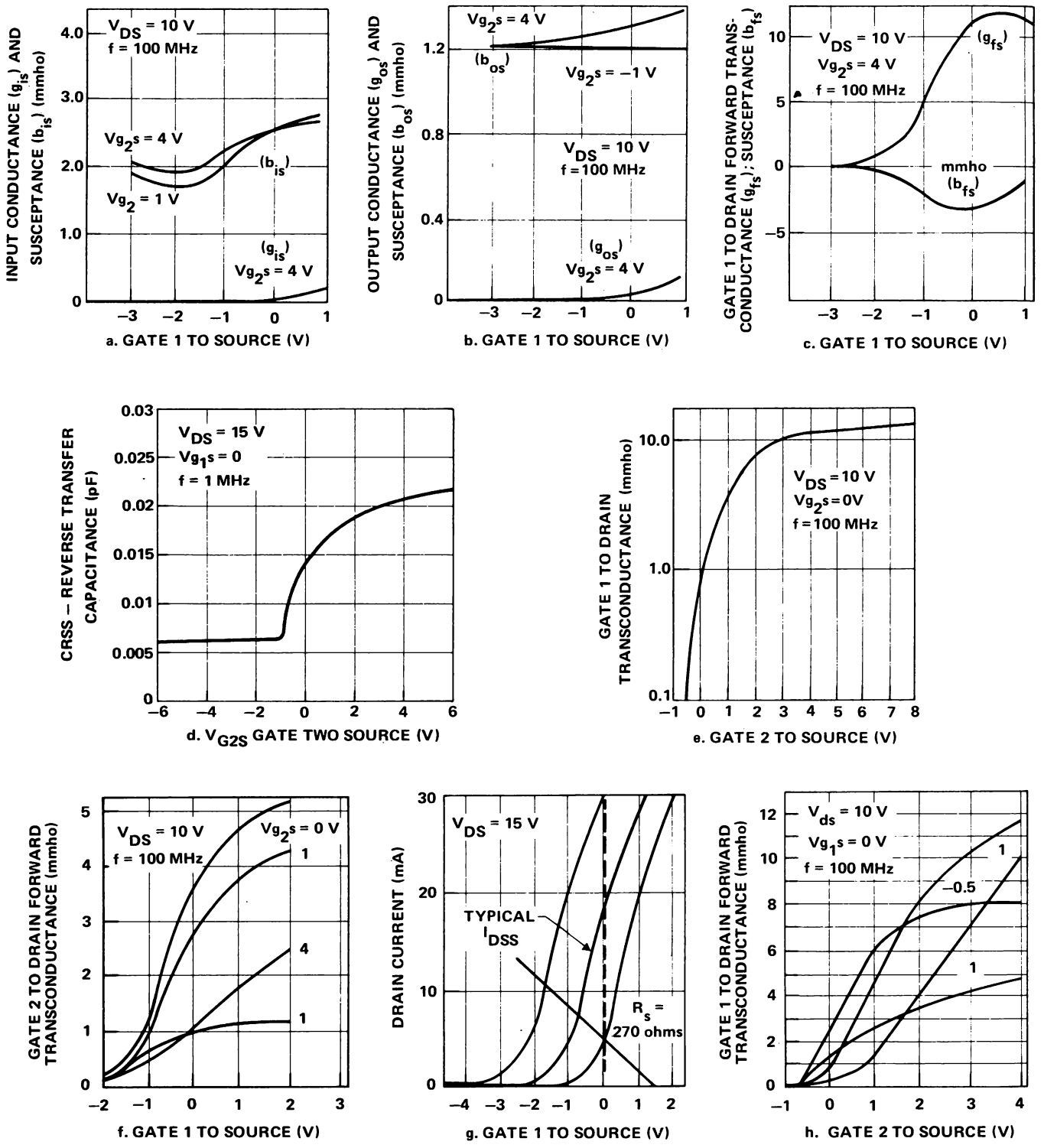


FIGURE 1. Device Data

where

K = stability factor;

$R_L' = 1/G_L'$;

$R_S' = 1/G_S'$

Solving for R_L'

$$R_L' = \frac{2}{K R_S' [|Y_{12} Y_{21}| + \mathrm{Re}(Y_{12} Y_{21})]}$$

For K = 2, R_L' = 4.8 kΩ, and from this the voltage gain is calculated to be

$$A_V = |Y_{fs}| R_L' = 57.5 \quad (3)$$

LVG* = 35.2 dB

In reality this gain gave objectionable skewing in the test fixture. A more acceptable load was experimentally determined to be 2 kΩ. Therefore LVG = 27.6 dB.

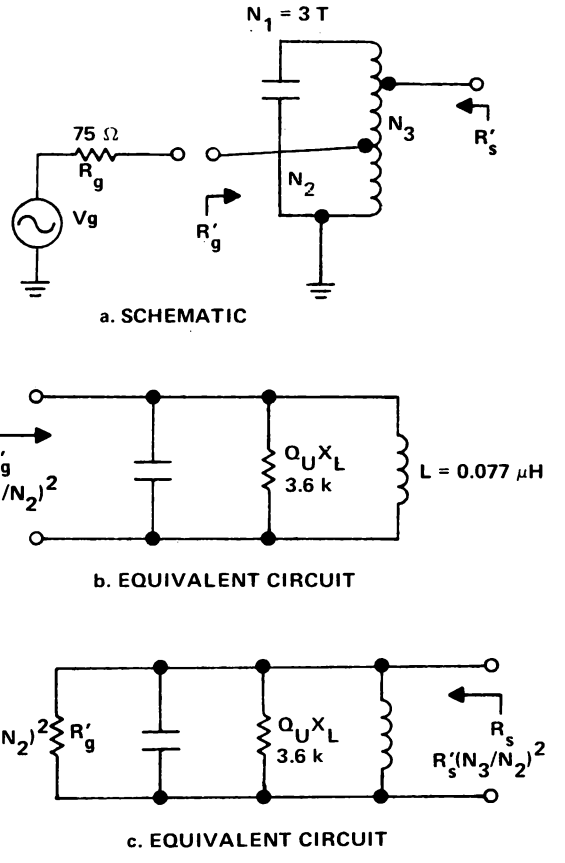


FIGURE 2. Input Coil

INPUT-COIL CONSIDERATIONS

The design of the input coil can proceed with the following assumptions (see Figure 2):

1) Loaded Q < 40
2) VSWR = R_g'/R_g < 2:1
3) Q_U = 75
4) X_L = 48 ohms (0.077 μH)
5) Device input resistance neglected.

An inductance of 0.077 μH was chosen, so that a standard tuning capacitor with a delta C = 15 pF would tune the 88-MHz-to-108-MHz FM band.[2] Unloaded Q's of

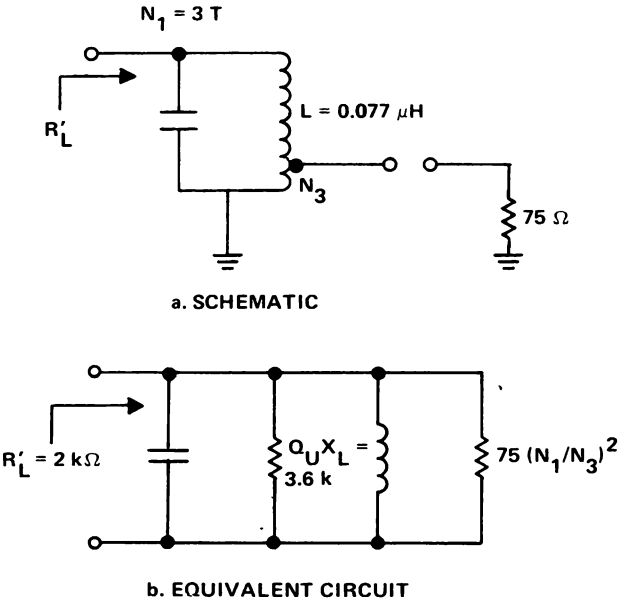


FIGURE 3. Output Coil

75 and 140 are easily obtained by proper choice of ferrite tuning slug.

The only resistance to be transformed down to match the 75-ohm antenna impedance is the coil loss $Q_U X_L$, with reference to Figure 2b,

$$(N_1/N_2)^2 = Q_U X_L/75 = 48 \quad (4)$$

$$N_2 = 0.434 \text{ turns}$$

$$N_1 = 3 \text{ turns}$$

With reference to Figure 2c,

$$R_S = \frac{R_g' Q_U X_L}{R_g' + Q_U X_L} = 1.8 \text{ K} \quad (5)$$

$$N_3 = N_1 (R_S'/R_S)^{1/2} = 2.24 \quad (6)$$

$$Q_L = R_S/X_L = 37.5 \quad (7)$$

The coil loss, which directly contributes to noise figure, is the loaded to unloaded Q ratio.[2] For this case, Q_L/Q_U = 0.5 (6 dB). This is a significant degradation of noise performance. If the computations are performed again with a VSWR = 2:1 or R_g' = 150 ohms and an unloaded Q = 140, the new Q_L = 36.3 and Q_L/Q_U = 0.26 (−2.6 dB). The key here is relaxation of the allowable VSWR.

The input voltage gain for the first calculation is computed simply as

$$LVG = 20 \log_{10} (N_3/N_2) = 14.2 \text{ dB}$$

*LVG (log voltage gain) is used here to distinguish between voltage and power gain.

OUTPUT-COIL CONSIDERATIONS

Design of the output coil can proceed by making the following assumptions (see Figure 3a):

1) $40 < Q_L < 60$
2) $Q_U = 75$
3) $X_L = 48$ ohms
4) Device output resistance neglected.

From Figure 3b solving for an $R_L' = 2\ k\Omega$

$$R_L' \doteq 75\ (N_1/N_3)^2$$

$$Q_U X_L/[75\ (N_1/N_3)^2 + Q_U X_L] \quad (9)$$

$$N_3 = 0.387 \text{ turns}$$

$$V_g = (N_3/N_1) = 1/8\ (LVG) = (-17.8\ dB) \quad (10)$$

$$Q_L = R_L'/X_L = 41.5 \quad (11)$$

The total gain can now be calculated as

$$\text{Gain} = \text{input} + \text{device} + \text{output}$$

$$\text{Gain} = 11.8 + 27.6 + (-17.8) = 21.6\ dB \quad (12)$$

Note that this is power gain because both input and output impedances are the same.

With an input and output loaded Q = 40, the image frequency (100 MHz + 21.4 MHz) will be better than 50 dB down, a standard requirement of most radio manufacturers.[3]

CIRCUIT EVALUATION

This design was used as a guide to construct a test fixture. Tests were made to explore the gain characteristic, detuning of 100-MHz reference frequency, and 3-dB bandwidth changes with AGC action, as well as third-order intermodulation degradation.[4] Three circuit configurations were used (Figures 4, 5, and 6). The circuit used to take the data shown in Figures 7a through 7c was biased at $I_d = 1/2\ I_{DSS}$ and used fixed bias on Gate 1 while AGC was applied to Gate 2 only. The circuit of Figures 8a through 8d was biased at $I_d = 1/2\ I_{DSS}$ and slaved Gate 1 to Gate 2 so that Gate 1 would come down with Gate 2. The circuit of Figures 9a through 9d was biased at I_{DSS} with AGC voltage applied to Gate 2. Some points of interest are:

1) 2 dB more gain when biased at I_{DSS}
2) Biasing $I_d = I_{DSS}$ results in a 2:1 increase in frequency shift (Figures 7b and 9b), an erratic bandwidth change (Figure 9c), and a slight worsening of the intermodulation figure (Figure 9d) with AGC over the Gate 1 fixed bias condition (Figure 7c).
3) Slaving Gate 1 reduces the low-attenuation frequency shift of some devices with AGC; increases gain-reduction slope, and increases the intermodulation figure of merit of devices beyond 40 dB of attenuation.
4) The best intermodulation figure was obtained at $I_d = 1/2\ I_{DSS}$ and fixed bias on Gate 1 (Figure 7c).
5) Devices with steepest gain-reduction slopes tend to have the worst intermodulation figures.
6) The device tended to be more stable with less skewing when biased at $1/2\ I_{DSS}$.

THE MIXER

A test fixture was constructed to measure the conversion gain and $f_o + 1/2$ IF distortion for a variety of bias conditions. Data are presented for both Gate 1 and Gate 2 local oscillator injection. The mixer was similarly constructed to the RF amplifier, except that a 10.7-MHz series trap was used at Gate 1, and a tuned load of approximately 5 kΩ at 10.7 MHz.

Figures 10a and 10b contain (for the bias point) conversion power gain versus oscillator injection and $f_o + 1/2$ IF distortion (dB) versus oscillator injection for the case of Gate 1 injection. It is interesting to note the flatness of these curves above 600 mV rms oscillator injection. A conversion gain of 20 dB was typical, as was an $f_o + 1/2$ IF spurious rejection of 55 dB. The spurious test was made with no gate selectivity for a worst-case analysis. The low pinch-off devices (−2 V at 20 μA I_d) gave a gain of typically 22 dB; high pinch-off devices (−5 V at 20 μA I_d) gave gains of typically 18 dB.

Figures 10c and 10d show that, by injecting the local oscillator into Gate 2 an average conversion gain of 14 dB was observed, and 65 dB $I_o + 1/2$ IF spurious rejection. With the local oscillator set to 3 volts rms, spurious rejection was 68 dB. This form of injection eliminates, for all practical purposes, the interaction often observed between RF and oscillator circuits during alignment.

A complete tuner was built with injection at Gate 1 (Figure 11). Performance specifications are as follows:

Power gain	40 dB
3-dB limiting	0.9 μV
30-dB quieting	*1.5 μV
Image rejection	50 dB
$f_o + 1/2$ IF	80 dB
All other spurious	> 100 dB
VSWR	1.2:1

Measurements taken with a conventional four-stage IF amplifier. Test frequency, 100 MHz ± 75 kHz.

CONCLUSIONS

The dual-gate MOSFET is well suited to FM tuner service as an RF amplifier and as a mixer. As an amplifier it provides high gain, low noise, and a large AGC range

*0.7 μV with VSWR = 2:1

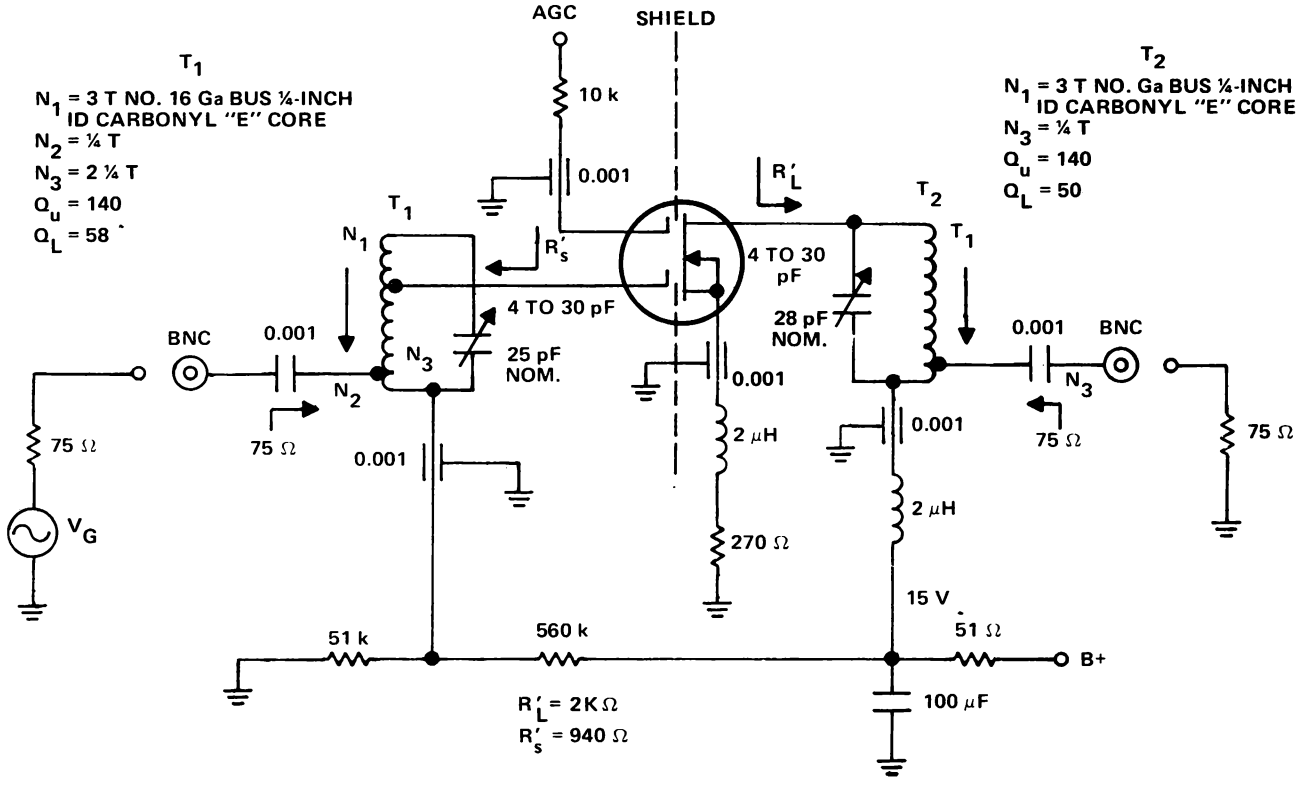


FIGURE 4. Fixed Gate 1 Bias 1/2 I_{DSS} Test Fixture

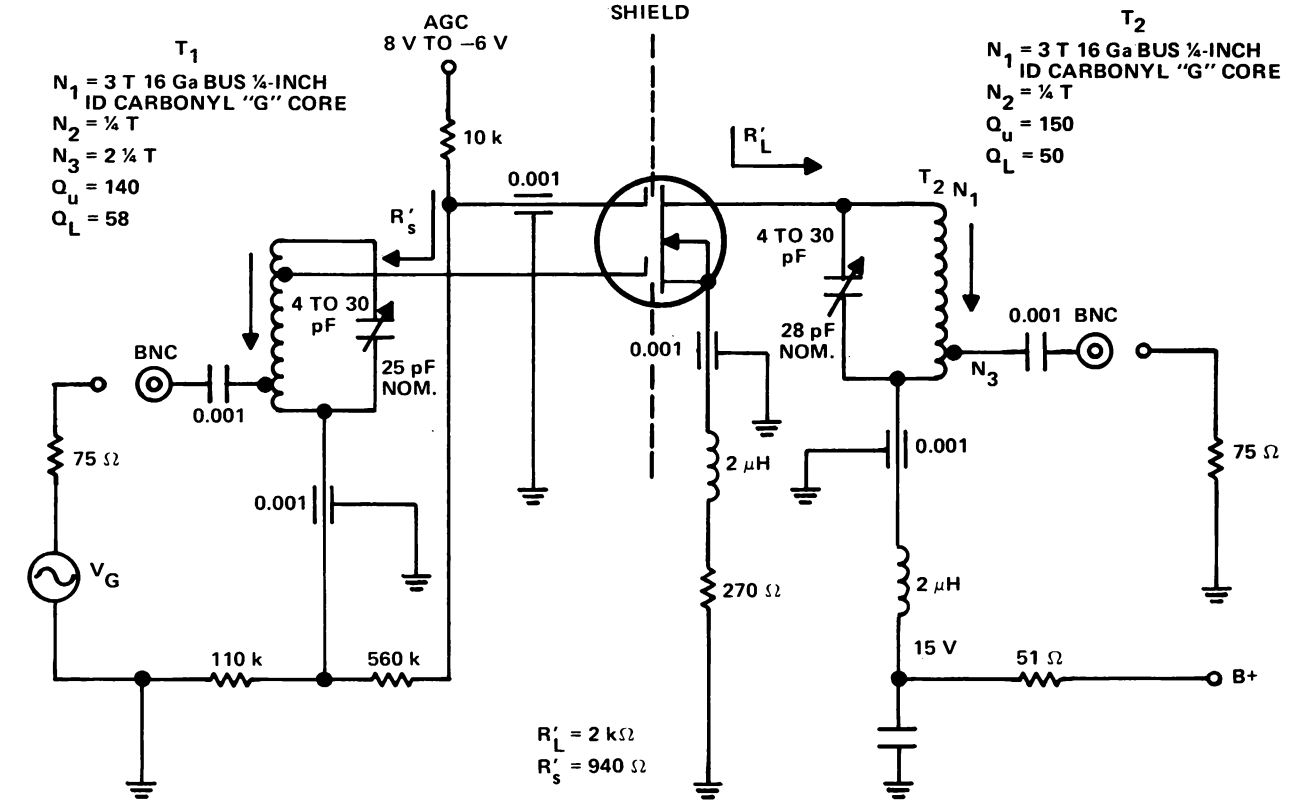


FIGURE 5. Variable Gate 1 Bias 1/2 I_{DSS} Test Fixture

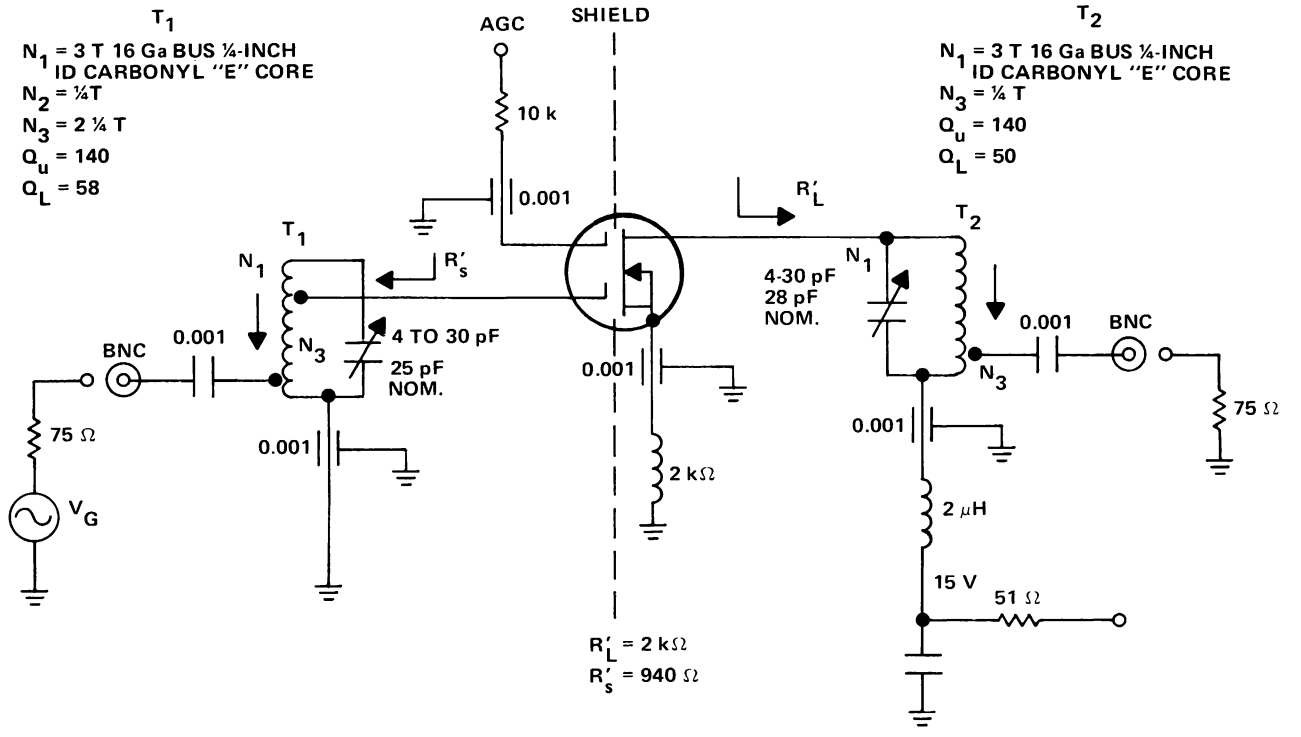


FIGURE 6. I_{DSS} Test Fixture

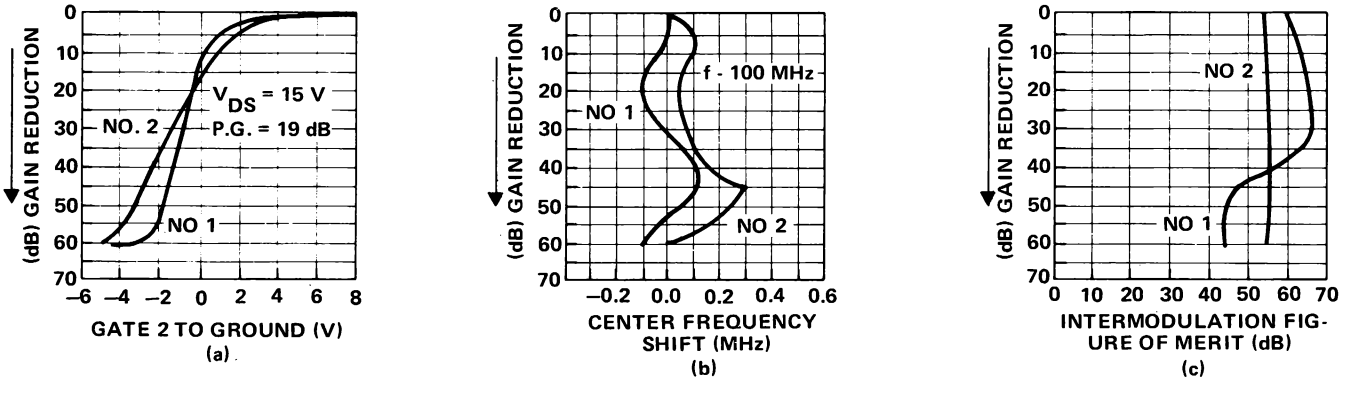


FIGURE 7. RF Performance Data with Gate 1 Fixed Biased (Schematic, Figure 4)

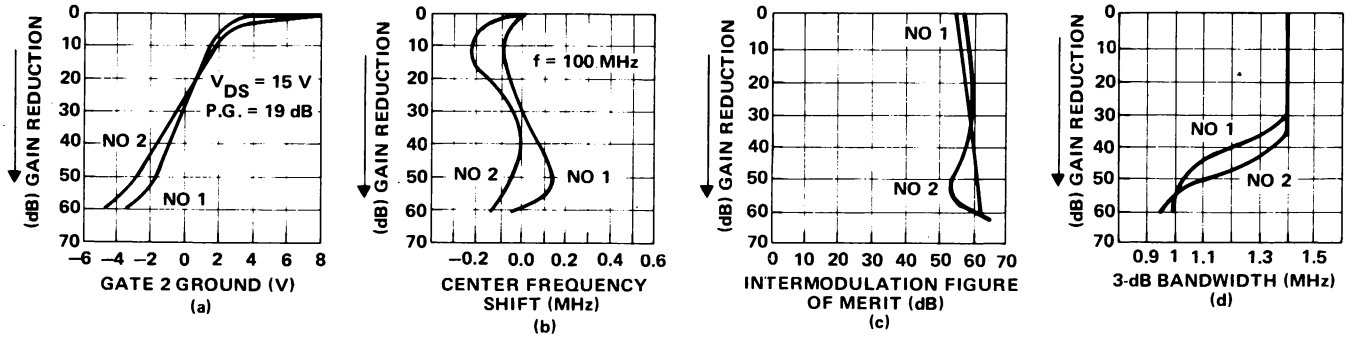


FIGURE 8. RF Performance Data with Gate 1 Slaved to Gate 2 (Schematic, Figure 5)

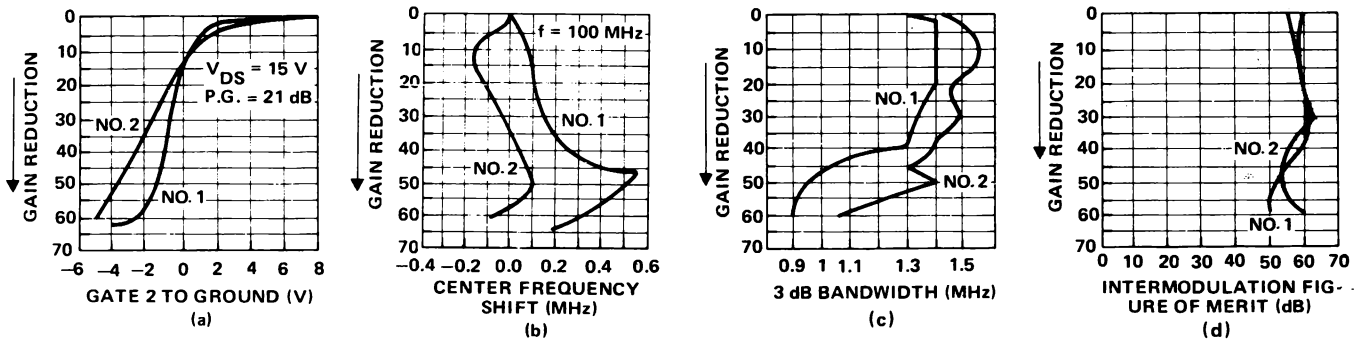


FIGURE 9. RF Performance Data Biased at I_{DSS} (Schematic, Figure 6)

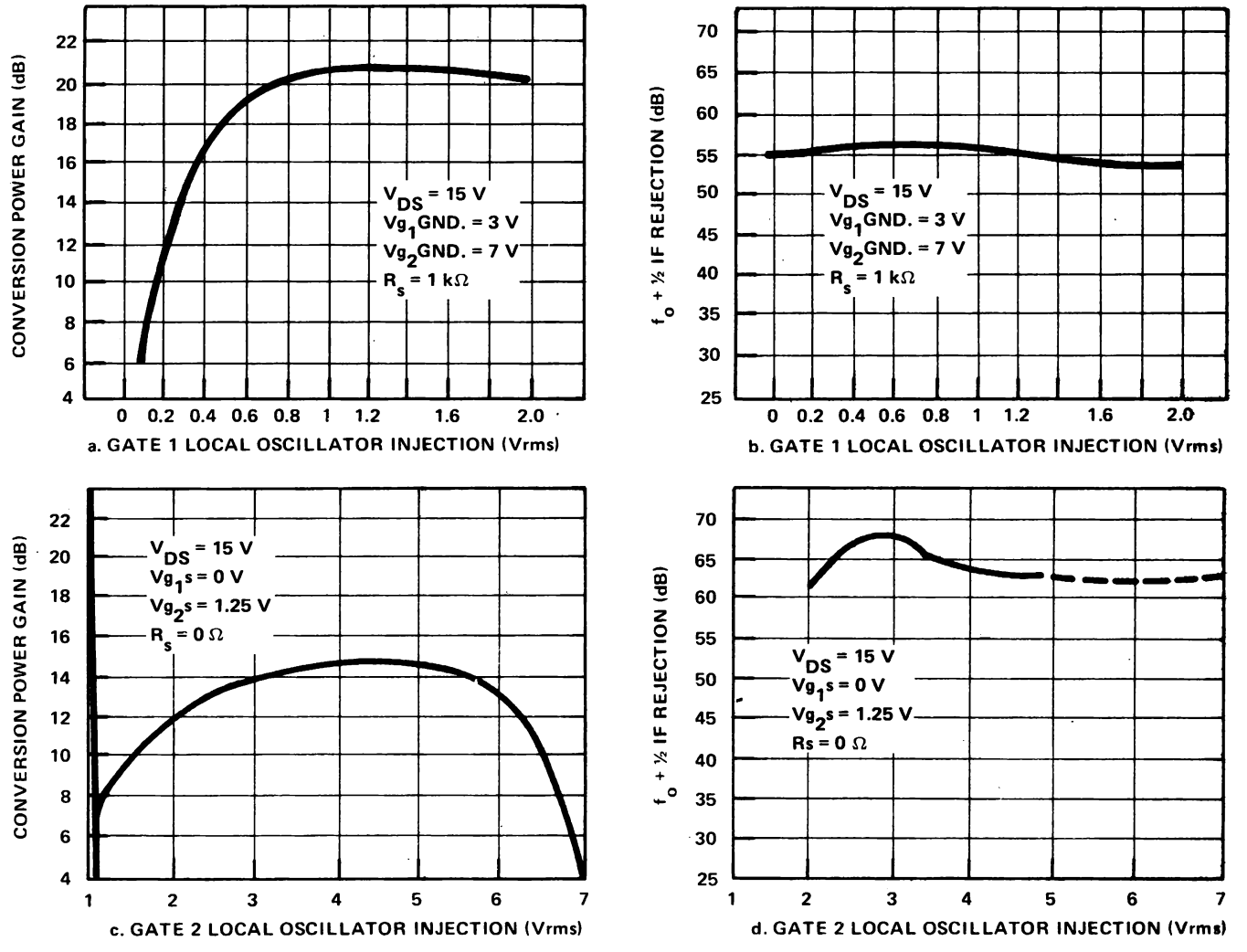

CONVERSION POWER GAIN (dB)
V_{DS} = 15 V
Vg_1GND. = 3 V
Vg_2GND. = 7 V
R_s = 1 kΩ
a. GATE 1 LOCAL OSCILLATOR INJECTION (Vrms)
f_o + ½ IF REJECTION (dB)
b. GATE 1 LOCAL OSCILLATOR INJECTION (Vrms)
V_{DS} = 15 V
Vg_1s = 0 V
Vg_2s = 1.25 V
R_s = 0 Ω
c. GATE 2 LOCAL OSCILLATOR INJECTION (Vrms)
Rs = 0 Ω
d. GATE 2 LOCAL OSCILLATOR INJECTION (Vrms)

FIGURE 10. Mixer Performance Data (Schematic, Figure 11)

without overload. As a mixer the dual-gate MOSFET has large conversion gain and high spurious rejection. Gate 2 L.O. injection offers 10 dB better spurious rejection but requires three times the signal. Gate 2 local oscillator injection does have an average of 6 dB less gain than Gate 1, but the gain loss necessary to eliminate all signs of RF L.O. interaction could easily make up the difference.

REFERENCES

1. Texas Instruments Incorporated, *Solid-State Communications*, New York, McGraw-Hill Book Company (1966), pp. 64-65.
2. Texas Instruments Incorporated, *Circuit Design for AM/FM, and TV*, New York, McGraw-Hill Book Company (1967), p. 113.

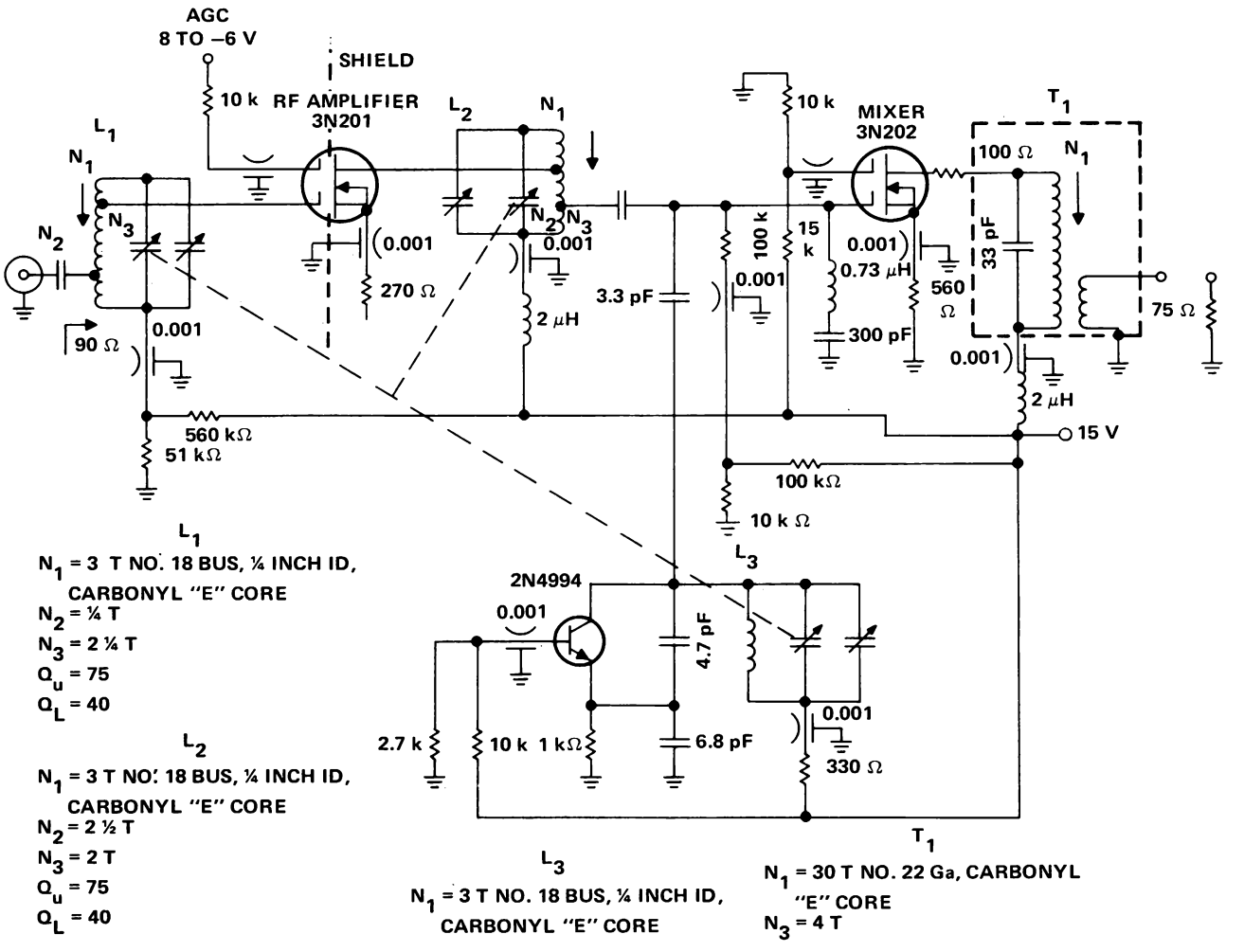


FIGURE 11. FM Tuner Application

3. David N. Leonard, *FM RF Amplifiers and Mixers Using Junction Field-Effect Transistors*, Texas Instruments Incorporated, Application Report (1967), pp. 7-9.
4. Ibid., p. 13.

20 Watts single-Sideband amplifier
(CA 168)

20 WATT SINGLE SIDEBAND AMPLIFIER FOR LOW VOLTAGE APPLICATIONS

By
Garry Garrard

If single sideband amplifiers operate from low voltage power supplies (for example, in mobile applications) rather than the more usual 28 volt supply, the design requirements are much more difficult to meet. Not only does the transistor current handling capability need to be much greater, but also the collector impedance matching becomes more difficult because of the lower impedances involved. This makes the wideband transformer design more critical.

The principal cause of nonlinearity in transistors used for SSB amplifiers is change in internal cutoff frequency, f_T, with collector current. The transistors used should have an f_T that is nearly constant over the working current range. The BLY 63 transistors used in the circuit in this report were originally intended as VHF mobile devices, but due to their high robustness, and constant f_T characteristics, they are very suitable for SSB applications.

CIRCUIT DESCRIPTION

A circuit diagram of the push-pull power amplifier is shown in Figure 1.

Input Circuit

Transformers T1 and T2 form a 180° power-splitting hybrid. Transformer T1 provides two outputs nominally of equal amplitude and 180° phase difference. Any imbalance is corrected by transformer T2. Errors in phase and power are dissipated in resistor R1.

This circuit also gives sufficient impedance matching to provide a reasonable input Voltage Standing Wave Ratio (VSWR).

Output Circuit

The collector load (R_L) required may be calculated from the well known expression:

$$P_{out} = \frac{\left(V_{CC} - V_{CE(sat)}\right)^2}{2\ R_L} \qquad (1)$$

If

P_{out} = 10 W for each device

V_{CC} = 13.5 V

$V_{CE(sat)}$ = 2 V (for example)

Then

R_L = 6.6 Ω theoretically

Thus the required impedance transformation is

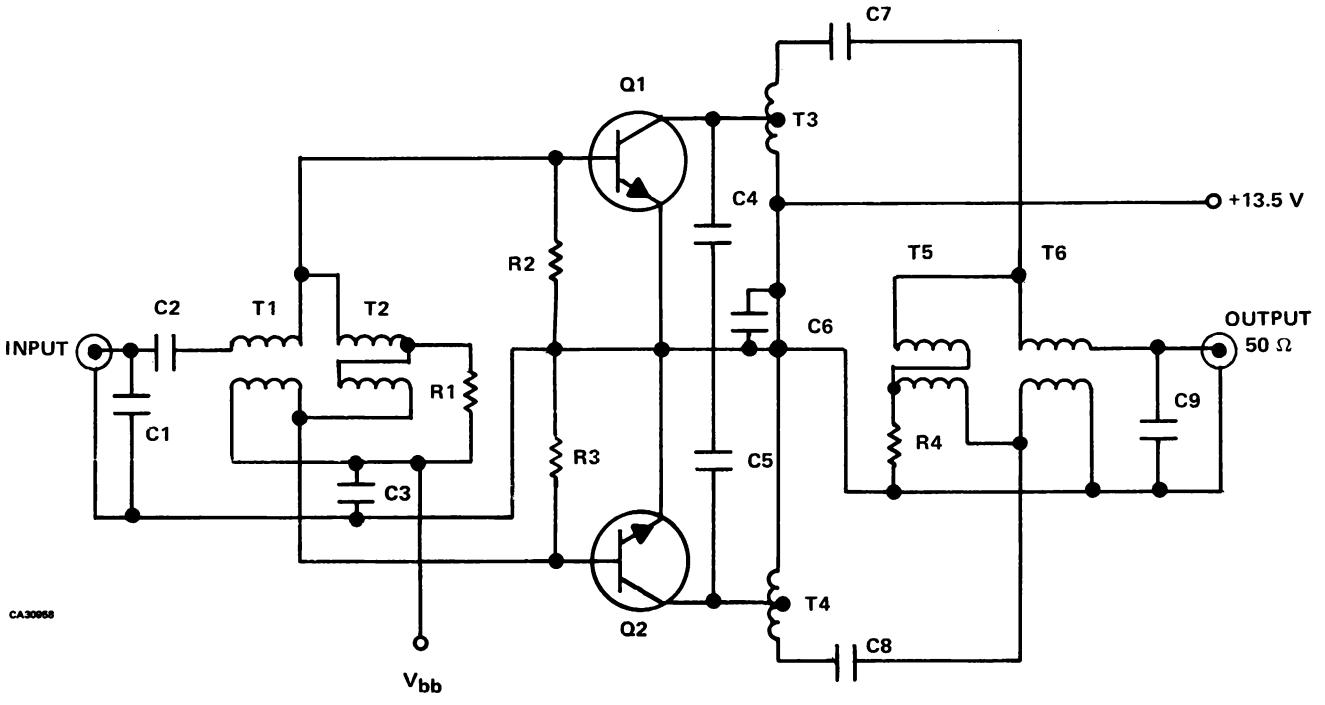
$$\frac{50}{6.6} = 7.6$$

However, using distributed transformers, only certain integer values of impedance transformation are possible. The nearest of these values to 7.6 is 8, given by a 4:1 impedance transformer and an additional impedance ratio of 2.1 in the unbalance-to-balance transformation.

There are several ways of combining 4:1 transformers and balance-to-unbalance transformers to achieve the required push-pull output. The configuration used was chosen because it was possible to achieve the required performance with relatively simple transformer windings. Even though the number of ferrite cores required is not the minimum possible, the overall mechanical complexity is less than that required if more complex winding techniques are used.

T3 and T4 are 4:1 distributed transformers, transforming the 6.25 Ω collector load to 25 Ω. The two anti-phase 25 Ω outputs are combined and transformed to 50 Ω in transformers T5 and T6, which forms a similar hybrid to transformers T1 and T2 on the input.

If some relaxation in performance is permissible, transformer T5 may be omitted. This will worsen the intermodulation distortion by 2 or 3 dB at rated output, and also give higher harmonic output.



CAPACITORS		TRANSFORMERS	
C1	200 pF CERAMIC	T1, T2, T3, T4, T6	18 TURNS OF TWISTED PAIR 30 SWG (28 AWG) ON INDIANA GENERAL CF106 TORROID
C2, C3, C6, C7, C8	0.1 μF CERAMIC		
C4, C5	270 pF CERAMIC	T5	18 TURNS OF 2 TWISTED PAIRS (4 STRANDS TWISTED TOGETHER) 34 SWG (31 AWG) ON INDIANA GENERAL CF106 TORROID
C9	39 pF CERAMIC		
RESISTORS		**TRANSISTORS**	
R1	12.5 Ω NON-INDUCTIVE	Q1, Q2	BLY 63
R2, R3	22 Ω		
R4	6 Ω NON-INDUCTIVE		

FIGURE 1. 20 Watt, 1.6 to 30 MHz Push-Pull Amplifier

TRANSFORMER DESIGN

All the transformers are of distributed construction and are designed using the principles described in references 1 and 2. Optimum winding impedances for each transformer are given in Table 1. Constructing windings to the impedances in Table 1 will result in very large transformers, in spite of the fact that only very small ferrite cores are necessary to handle the power.

Table 1

Transformer	Optimum Characteristic Impedance (Ω)
T1	50
T2	25
T3	12.5
T4	12.5
T5	25
T6	50

In this design, all transformer windings, except T5, are wound with a single pair of twisted wires giving a characteristic impedance of approximately 70 Ω. In order to achieve satisfactory low frequency performance, 18 turns are necessary for transformers T3 and T4 on the ferrite cores used. This gives a winding length of 18 cm, or an equivalent electrical length ($\beta\ell$) at 30 MHz of 6.5°.

From information in Reference 1:

$$Z_{in} = Z_o \left\{ \frac{Z_L \cos \beta\ell + j Z_o \sin \beta\ell}{2Z_o (1 + \cos \beta\ell) + j Z_L \sin \beta\ell} \right\} \quad (2)$$

Where

Z_{in} = low impedance input (collector load)

Z_o = winding impedance

Z_L = load impedance

With a 25 Ω load, and a winding as above,

$$Z_{in} = (5.88 + j\ 2.2)\ \Omega$$

Thus there is an inductive element in the collector load when using a high line impedance, together with a lower resistive part than required.

Experience shows that a complex collector load impedance with an inductive element giving a phase angle of even 10° can give serious degradation of intermodulation distortion even though the change in modulus is quite small. A collector load of the same complex value and phase angle but with capacitive reactance will have little effect on linearity, however. This makes it necessary to compensate for the above inductive element in the collector load.

The transformer input impedance above may be considered as an equivalent parallel circuit as shown in Figure 2. The addition of a shunt capacitor of reactance −j 18 will result in a resistive load of 6.7 Ω at 30 MHz: C = 300 pF.

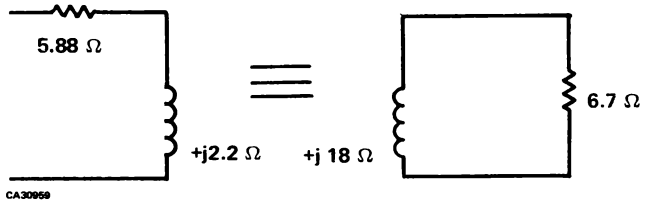


FIGURE 2. Transformer Input Impedance Considered as an Equivalent Parallel Circuit

Capacitors C4 and C5 on the circuit diagram, together with the output capacity of the transistors make up this compensating reactance. Capacitor C9 performs the same function for the output hybrid. As the frequency is reduced the line impedance becomes less critical and the capacitors have less effect on the circuit.

BIAS SUPPLY

The bias circuitry is not critical providing it has a reasonably low output impedance, and may be adjusted to give about 10 mA of quiescent current in the BLY 63 transistors.

Fairly simple temperature compensation may be used. Ballasting built into the transistors will prevent thermal runaway. The bias circuit used for making measurements is shown in Figure 3.

It is advisable to use a pair of BLY 63 transistors with dc gain matched to within approximately 10% for optimum performance, unless separate bias supplies are used for the two devices.

PERFORMANCE

Detailed information on performance is given in Figures 4, 5, 6, 7, and 8. It may be summarized briefly as follows:

Frequency Range	1.5 to 30 MHz
POUT	20 W
Supply Voltage	13.5 V nominal

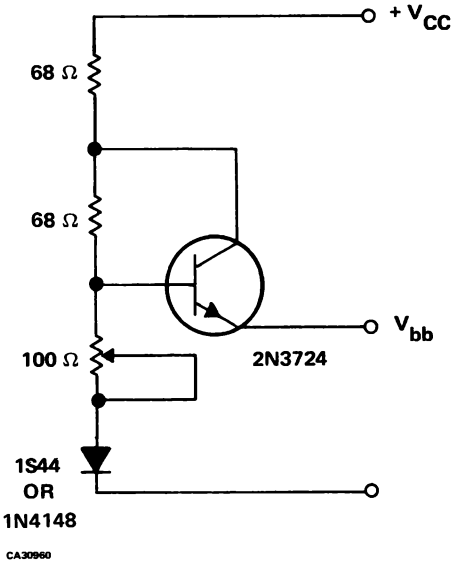


FIGURE 3. Bias Circuit Used for Measurements

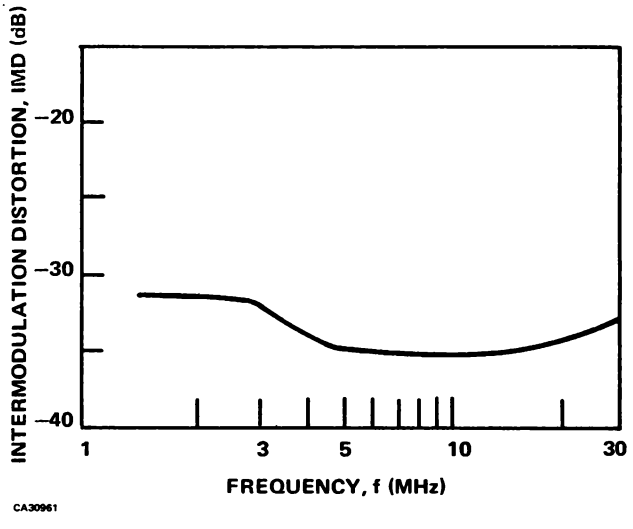


FIGURE 4. Intermodulation Distortion versus Frequency. (V_{CC} = 13.5 V. P_{OUT} = 20 W PEP, 10 W Average.)

Gain	16 dB minimum
Intermodulation Distortion	−30 dB relative to either signal of two tone output.

The amplifier will withstand any mismatch at full output power.

DRIVER STAGE

With 16 dB gain, the maximum drive level required is 0.5 W. This may be simple obtained from a single BLY 62 transistor in class A operation.

A suitable circuit is shown in Figure 9. Overall gain of the driver and push-pull output stage is 33 dB minimum. With the drive level required, the addition of the extra stage results in very little degradation of linearity from that resulting from the output stage. The maximum input power

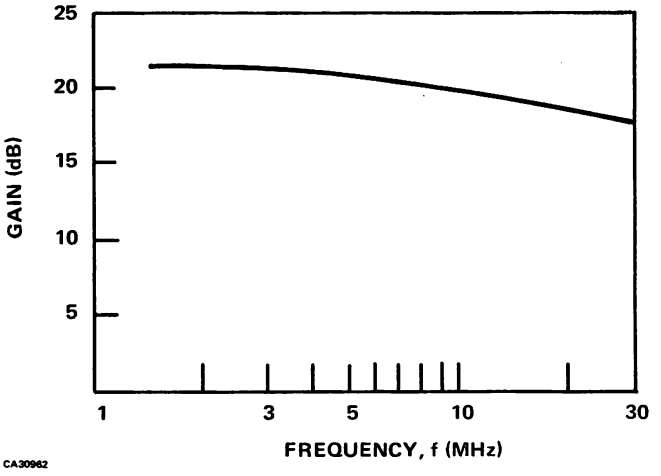


FIGURE 5. Gain versus Frequency. (V_{CC} = 13.5 V. P_{OUT} = 20 W PEP, 10 W Average.)

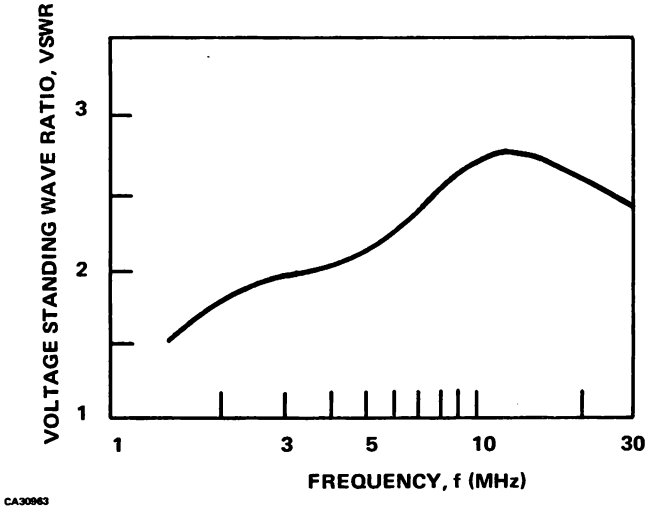


FIGURE 6. VSWR versus Frequency. (V_{CC} = 13.5 V. P_{OUT} = 20 W PEP, 10 W Average.)

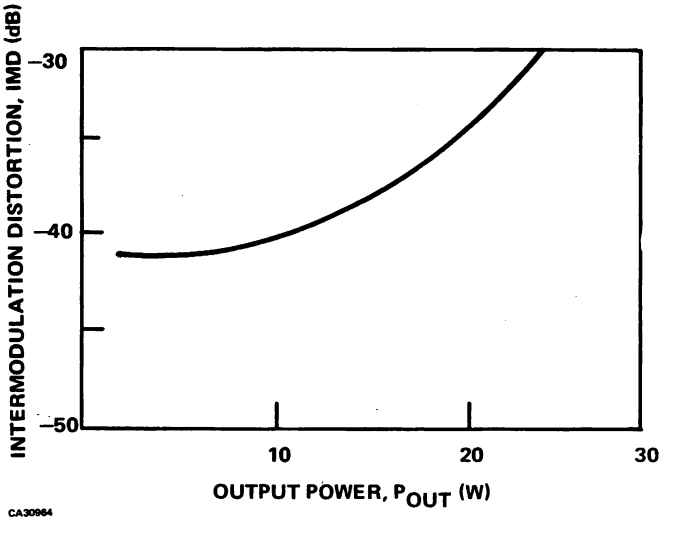


FIGURE 7. Intermodulation Distortion versus Output Power (V_{CC} = 13.5 V. Frequency = 30 MHz.)

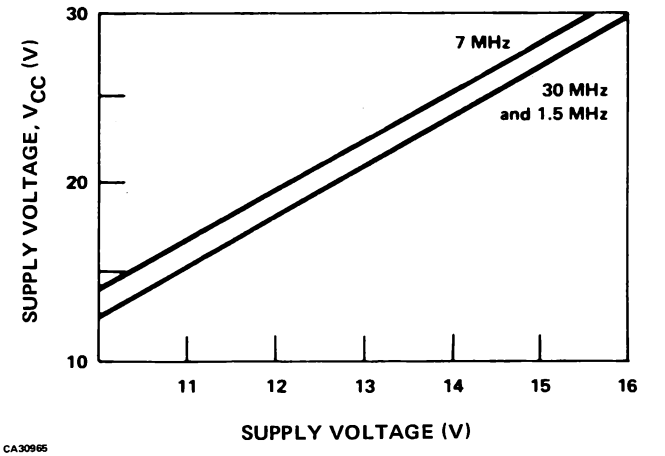
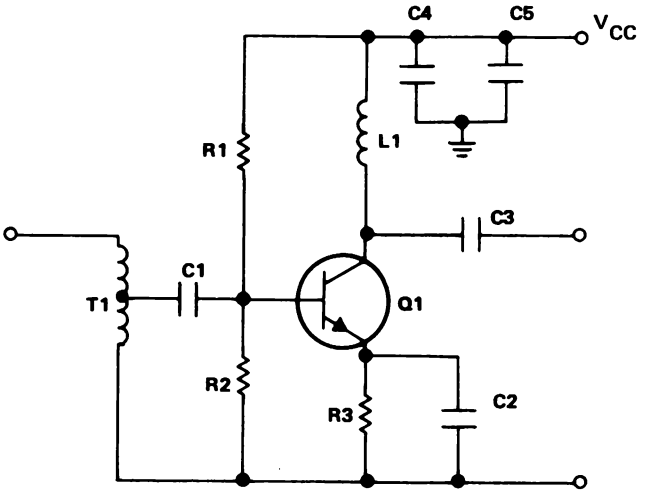


FIGURE 8. Linear Output Capability versus Supply Voltage. (IMD = −30 dB.)



R1		150 Ω
R2		22 Ω
R3		2.7 Ω
C1, C2, C3, C4, C5		0.1 μF CERAMIC 4 μF ELECTROLYTIC
L1	24T	30 SWG ENAMELLED WIRE (28AWG) ON INDIANA GENERAL CF102 TORROID.
T1	16T	OF TWISTED PAIR 30 SWG (28AWG) ENAMELLED WIRE ON INDIANA GENERAL CF102 TORROID.
Q1	BLY62	

CA30966

FIGURE 9. Driver Stage

then required is 10 mW at the top of the band, and considerably less at the center of the band.

REFERENCES

1. Ruthroff, C. L., Some Broadband Transformers, Proc. IRE, August 1959, pp. 1337-1342.

2. Couse, T. and Pitzalis, O., Broadband Transformer Design for RF Transistor Power Amplifiers, Proc. 1968 Electronics Components Conference, pp. 207-216.

Programable unijunction Transistor

PROGRAMABLE UNIJUNCTION TRANSISTOR

by
Glen Coers

The programable unijunction transistor, PUT, is a general purpose low power thyristor. It is a three terminal device which exhibits a negative resistance region under certain operating conditions. The most numerous PUT applications are in relaxation oscillator and, trigger and timing circuits. This device, however, can also be used as a lower power complementary SCR in applications as a lamp driver and ring counter.

The PUT exhibits characteristics similiar to that of a conventional unijunction transistor (UJT). However, when compared to a conventional unijunction transistor, the PUT offers many advantages. It's programable, η,I_P, I_V,R_{BB}. It has low leakage, high sensitivity, and high breakdown voltage. It operates with low voltage. It provides fast high energy trigger pulses, and it's low cost.

The device is available from Texas Instruments in a low cost TO-92 plastic package (A7T6027 and A7T6028) and TO-18 metal can (2N6116, 2N6117, and 2N6118).

CHARACTERISTICS OF UNIJUNCTION TRANSISTORS

PUT Device Physics

The programable unijunction transistor is a solid state semiconductor device composed of four layers of alternate conductivity type semiconductor material.[1] Figure 1 shows the physical construction of a PUT. Three junctions, J1, J2, and J3, are formed by the four layers of P-and N-type silicon. To see more clearly the operation of the device, an equivalent structure is illustrated in Figure 2. The model of Figure 2 is a two transistor analog and the device can be analyzed in terms of parameters of two transistors. The junction J1 acts as the emitter-base junction for the NPN transistor. J3 acts as the emitter-base junction for the PNP transistor. J2 serves as collector-base junction for both devices.

The NPN transistor has a current gain β_N. The PNP section has a current gain β_P. These current gains will increase with increasing current flow in their respective equivalent transistors. Figure 3 illustrates the V-I characteristic developed at the anode by this circuit.

As seen in Figure 3, when the anode voltage is less than V_S, only a small leakage current flows from gate to anode. As the anode voltage is raised above the gate voltage, gate current will begin to flow from the anode to the gate. This is emitter current for the PNP transistor which will

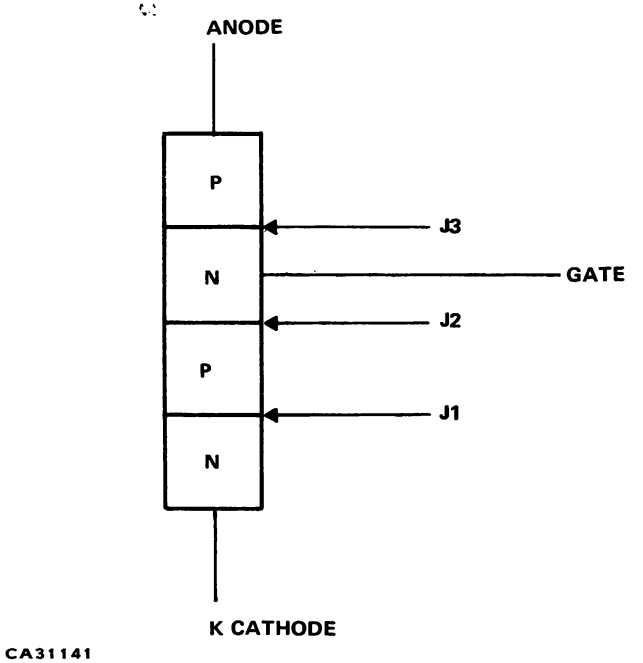


FIGURE 1. Construction of a Programable Unijunction Transistor

cause PNP collector current to flow ($\alpha_P I_A$). The NPN base current times β_N is collector current for the NPN and is also base current for the PNP. This re-enforces the initial gate current. At low currents, the NPN and PNP current gains are low. However, as the currents increase, the gain of both transistors increases and regenerative action results. When this occurs, a negative resistance is developed between the anode and cathode and the device goes into a high conduction state. The current at which this regenerative action takes place is called peak-point current, I_P. I_P is strongly dependent on R_G. Figure 4 illustrates how I_P and R_G are related. Increasing R_G causes I_P to decrease.

Valley current, I_V, is also a function of R_G. Figure 5 illustrates valley current versus R_G. For large values of anode current the NPN-PNP transistors have enough current gain to sustain the regenerative conditions and supply NPN collector current to R_G. As the anode current is lowered, a point is reached where the current within the NPN-PNP loop and the current supplied to R_G is just enough to sustain conduction. This is the holding current level. It is not the valley-point current (I_V). The valley current can be

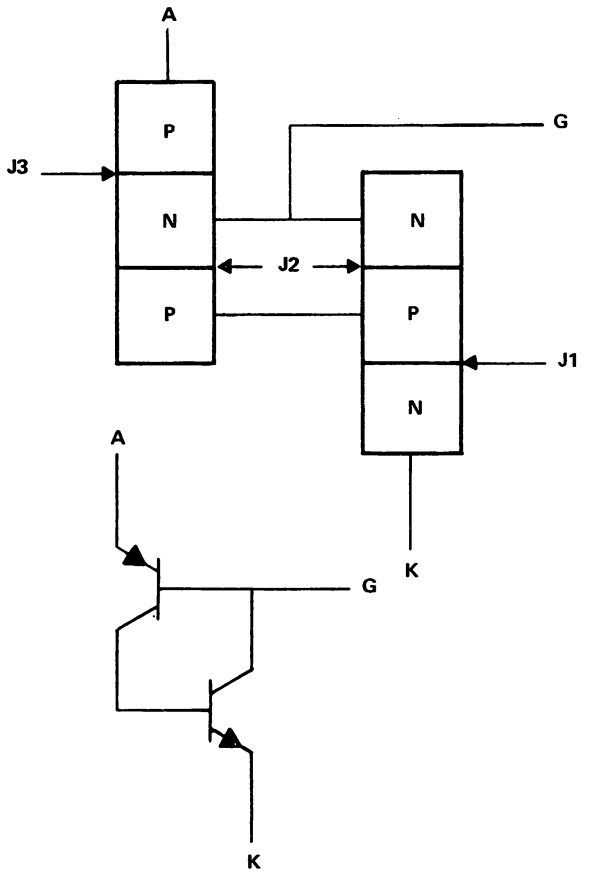


FIGURE 2. Equivalent Structure of a Programable Unijunction Transistor

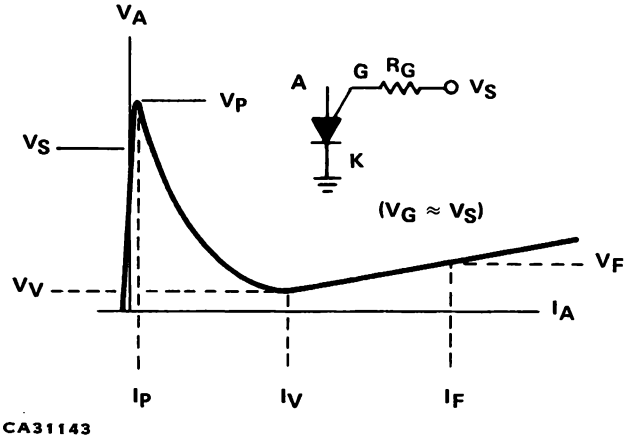


FIGURE 3. Anode – Cathode Characteristic's of the Circuit in Figure 2

defined as the point where dv/dI = 0. Refer to Figure 3.

$$I_V = \left(\frac{1+\beta_P}{\beta_P \beta_N - 1}\right)\left(\frac{VS - VCE_{(Sat)}}{R_G}\right) \quad (1)$$

Equation 1 shows that I_V is inversly proportional to R_G. Keeping in mind that current gain of the transistors is a function of current, equation 1 is used only to illustrate the relationship between I_V to R_G.

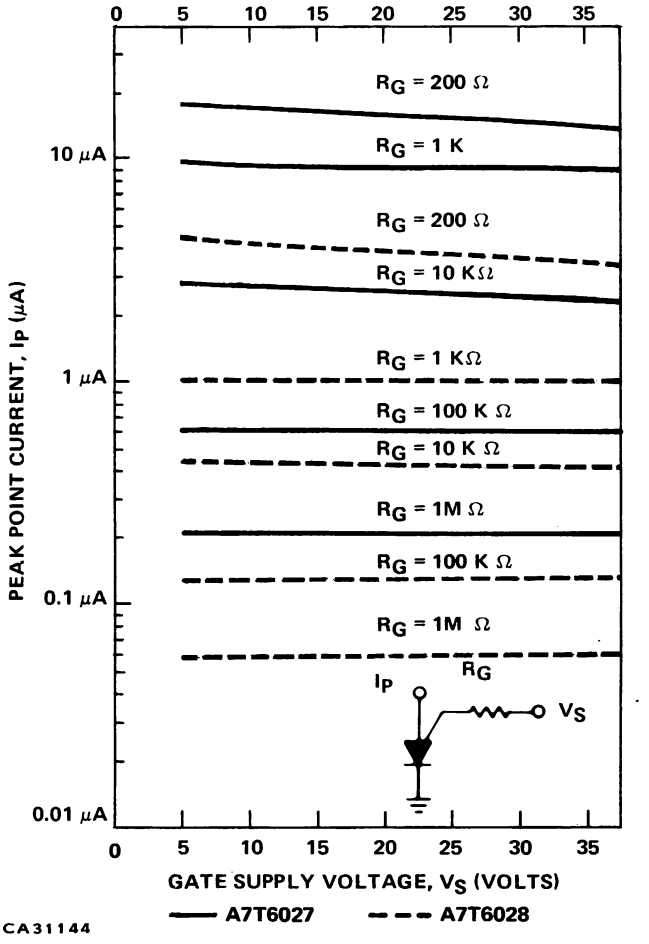


FIGURE 4. Relationship of Peak-Point Current, I_P, and Gate Resistance R_G

Comparison of Standard UJT and PUT

The operating characteristics can be easily understood by comparing the PUT with the conventional UJT.[2] Figure 6(a) illustrates a basic conventional unijunction transistor circuit. Figure 6(c) is the same circuit except the UJT has been replaced by the PUT and two resistors, R1 and R2. The equivalent circuits are also shown [Figure 6(b) and 6(d)]. Lets look at operation of the UJT circuit in Figure 6(b). When the diode becomes forward biased, R1 (equivalent emitter-base resistance) is modulated to a lower value of resistance. This results in a negative resistance characteristic between the emitter and base 1.

The PUT operates similarly but instead of using conductive modulation, the negative resistance is developed by the regeneration inherent in a PNPN device as shown in Figure 6(d). The resistors R1 and R2 control the voltage at which the diode conducts. η (eta) and therefore, V_P (refer to Figure 3) are determined by the value of R_1 and R_2.

$$\eta = \frac{R1}{R_1 + R_2} \qquad (2)$$

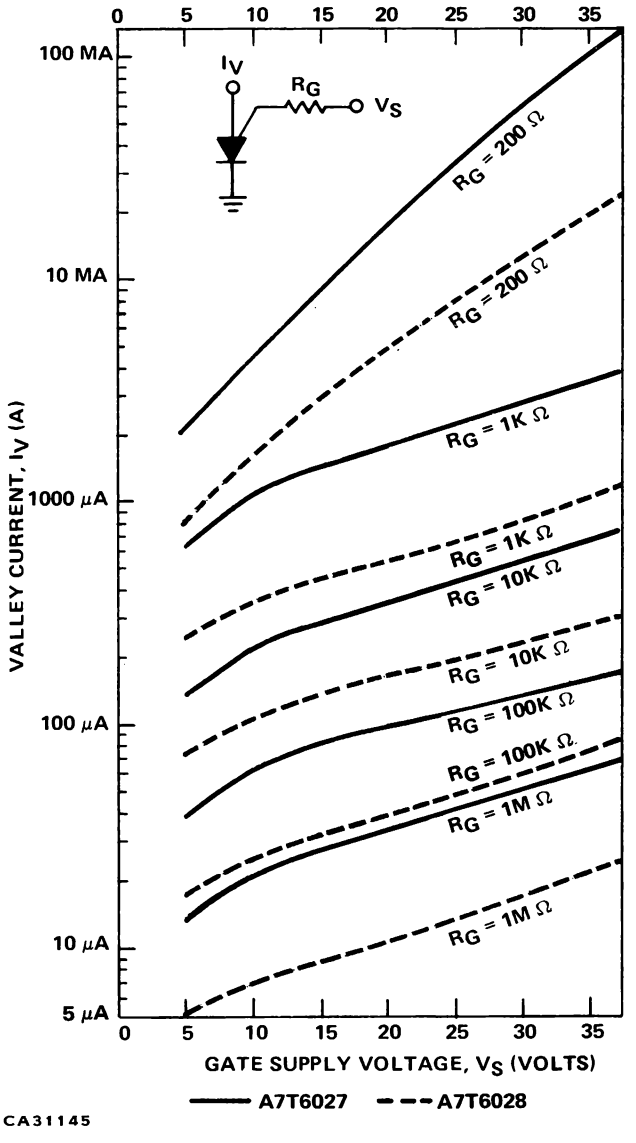


FIGURE 5. Valley Current, I_V, versus Gate Resistance, R_G

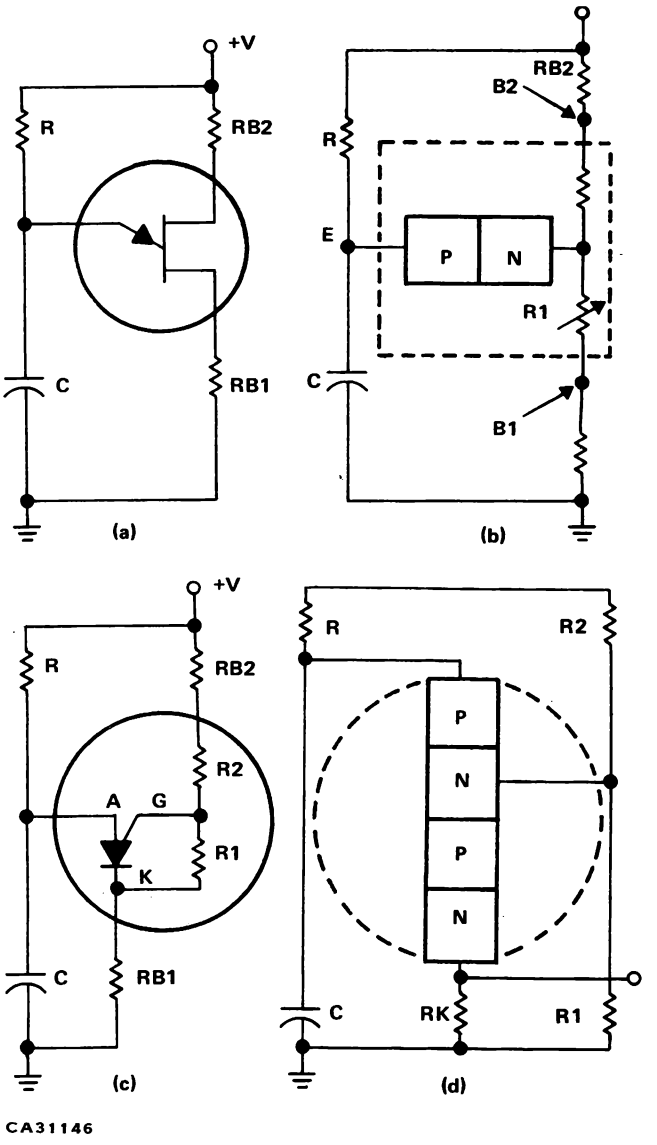


FIGURE 6(a). Basic Unijunction Transistor Circuit. (b) Equivalent Circuit of (a). (c) Basic PUT Circuit. (d) Equivalent Circuit of (c)

BASIC PUT OSCILLATOR CHARACTERISTICS

How To Select R and C Values

The basic PUT relaxation oscillator circuit, which is the basic building block in most PUT timer and oscillator circuits, is shown in Figure 7. When power is applied, capacitor C_A charges exponentially through resistor R_A until the voltage on the capacitor equals the anode firing voltage, V_P. At this voltage, the anode gate junction becomes forward biased and the anode goes into the negative resistance region. Capacitor C_A discharges through the anode (POINT C) and a positive pulse is available at the cathode (POINT A). Also, a negative pulse is available at the gate (POINT B).

After the capacitor has discharged the PUT will turn off if resistor R_A meets certain conditions. Capacitor C_A will start to charge up again and the cycle will be repeated.

For this sequence to occur, the value of R_A must meet certain requirements. These requirements are illustrated by the curve in Figure 8. (To show greater detail, this curve is not drawn to scale.)

In the PUT oscillator circuit, capacitor C_A will charge until the anode voltage is equal to V_P. At this point on the characteristic curve, I_A will be flowing. For the PUT to fire, the value of resistor R1 must be small enough to allow I_P to flow. Resistor R_A must, therefore, meet the following requirements:

$$R_A < R_{MAX} = \frac{V_1 R2 - (R1 + R2)\, V_T}{(R1 + R2)\, I_P} \quad (3)$$

$$R_A > R_{MIN} = \frac{V_1 - V_V}{I_V} \quad (4)$$

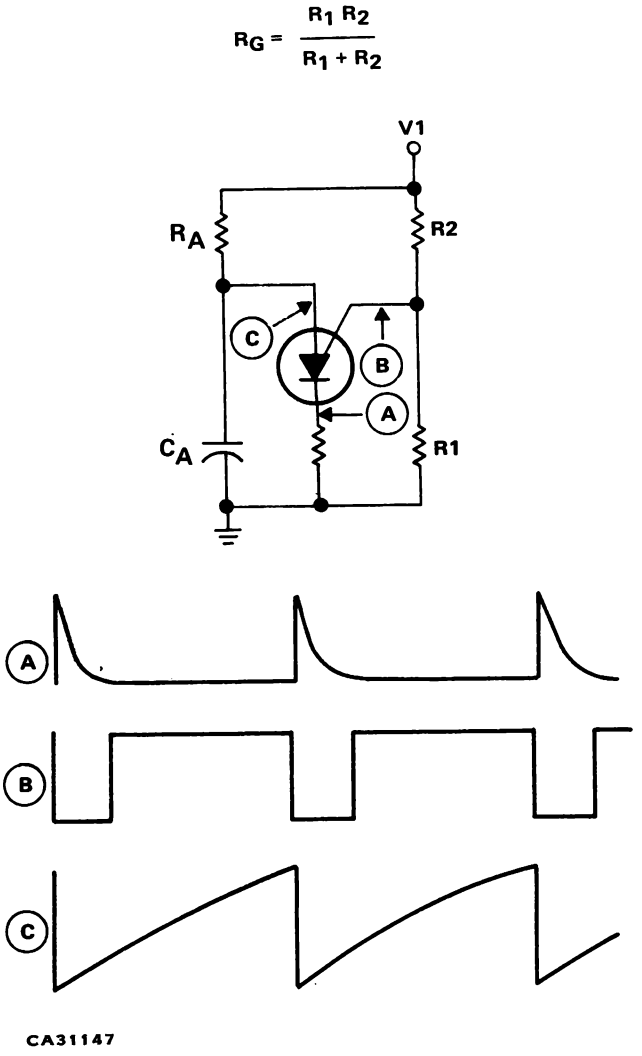


FIGURE 7. PUT in a Typical Relaxation Oscillator Circuits with Pulse Waveforms Available

Figure 8 illustrates the anode characteristics for the PUT in three different regions. Load line number one (LL1) intercepts the characteristic curve in the cutoff region. This does not allow enough current to trigger the PUT. The reason for this is that the resistance value is too large. If R_A is selected less than R_{MAX} the PUT will turn on, and C_A will discharge through the anode. If R_A is too small and allows anode current larger than valley current, I_V, to flow, a stable state in the saturation region will result and load line number two (LL2) will intersect the anode characteristic curve in the positive resistance region. The minimum R_A that can be used to assure oscillation can be defined by this equation:

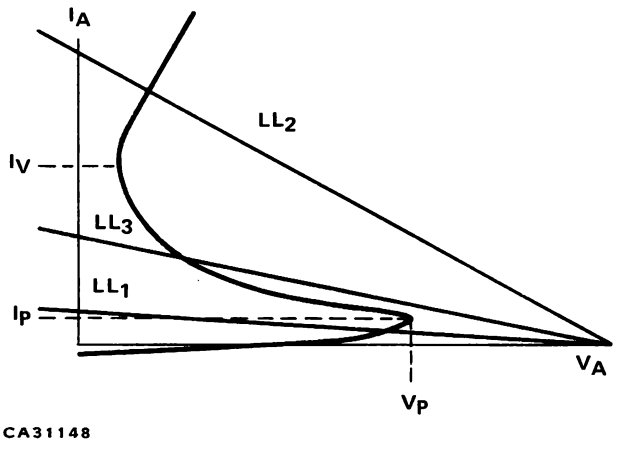


FIGURE 8. PUT Operation in Oscillator Depends Upon Value of R1 which Determines Load Line Region

Under actual operating conditions, the variation in valley voltage with respect to valley current in the area of the valley point is so small that to assure turn off, R_A should be selected to be two to three times larger than R_{MIN}.

If the anode resistance is selected properly, load line number three (LL3) will be in the negative resistance region. This is ideal for device oscillation.

The time required for a complete period (determined by Capacitor C_A) can be derived from the following equations. The voltage across the capacitor is given by

$$e_C = \frac{1}{C} \int i dt \quad (5)$$

The voltage between the anode and ground with respect to time is given by:

$$V_A = V_V + (V_1 - V_V)\left(1 - e^{-t/R_A C_A}\right) \quad (6)$$

where $V_A = V_C$

Substitute

$$V_A = V_T + \left(\frac{R_1}{R_1 + R_2}\right) V_1$$

and solve for T:

$$\frac{1}{f} = T = R_A C_A \ln \frac{V_1 - V_V}{V_1 - V_T - \left(\frac{R_1 V_1}{R_1 + R_2}\right)} \quad (7)$$

If switching times are included the equation becomes:

$$\frac{1}{f} = T = R_A C_A \ln \frac{V_1 - V_V}{V_1 - V_T - \left(\frac{R_1 V_1}{R_1 + R_2}\right)} + t_{on} + t_{off} \quad (8)$$

A simplification of this equation which is more practical is:

$$\frac{1}{f} = T = R_A C_A \ln\left(\frac{R_1 + R_2}{R_2}\right) \quad (9)$$

or

$$\frac{1}{f} = T = R_A C_A \, 2.3 \log\left(\frac{R1 + R2}{R2}\right) \quad (10)$$

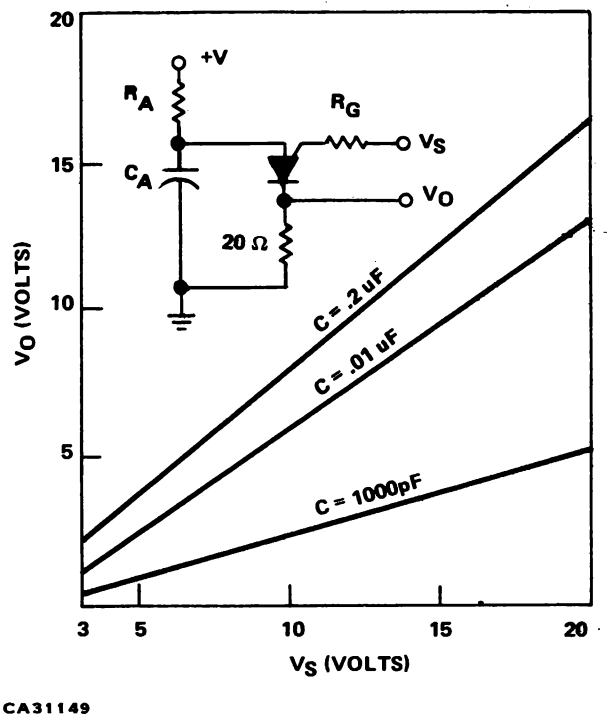


FIGURE 9. Pulse Output Voltage for Various Capacitor Values

OUTPUT CHARACTERISTICS OF PUT CIRCUIT

The dynamic resistance of a PUT in saturation is approximately 3 ohms. This results in high peak pulse output. This can be seen by referring to the characteristics shown in Figure 9. This is attributed to the PNPN nature of this device (as opposed to the conductivity modulation of the conventional UJT). The forward conductance is high and the risetime is fast. Risetime is typically 65 nanoseconds with a maximum of 80 nanoseconds specified.

A conventional UJT dissipates power depending on R_{BBO} and V (B2B1). The current flow in the PUT during the off condition is leakage and therefore, there is essentially no power dissipation.

There are several ways in which the PUT can be connected to obtain different combinations of parameters. Figure 10 shows three possible ways of connecting the PUT in order to satisfy different requirements. For the typical application [Figure 10(a)] the resistor ratio R1 and R2

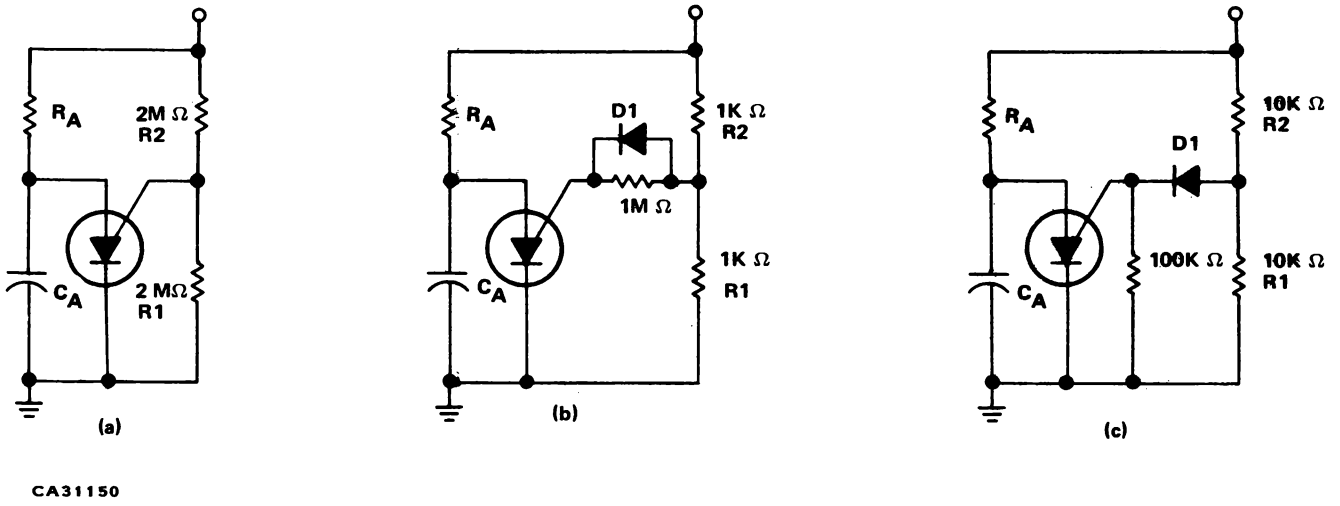


FIGURE 10. Three Different PUT Circuit Configurations to Achieve Different Parameter Combinations

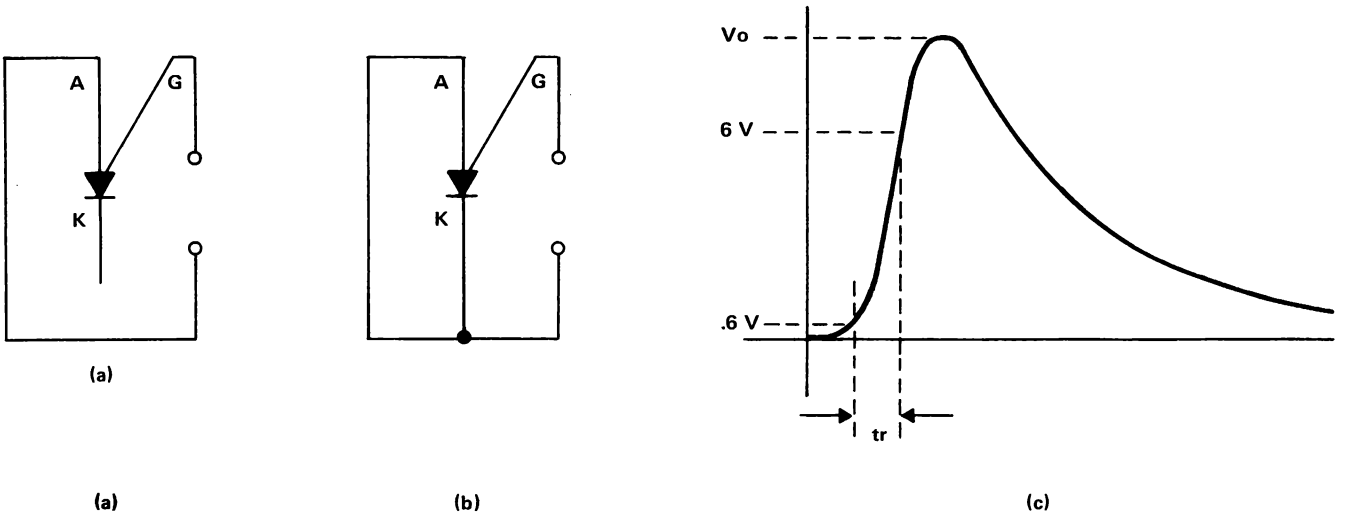


FIGURE 11. Illustrations to Clarify Definition of Parameters, (a) IGAO, (b) IGKS, and (c) VO and t_r.

would be chosen to obtain the desired eta or V_P. The Thevinin equivalent resistance (R_G) is chosen to meet the I_P and I_V requirement. The highest practical value of R_G is 1 megohm. This will yield a low I_P and low I_V. The lowest practical of R_G value is 200 ohms. This will yield a high I_P and high I_V.

Figure 10(b) shows a slightly different configuration to obtain a low I_P and a high I_V. When the device is off, the effective value of R_G is 1 megohms and therefore meets the requirement for low I_P. When the device turns on, the gate approaches ground. This forward biases the diode D1. The diode impedance is now very low and the effective value of R_G is the parallel combination of R_1 and R_2 which are low in value meeting the requirement for high valley current. Figure 19(c) illustrates a circuit possible with a PUT but difficult with a standard UJT – that of temperature compensation.

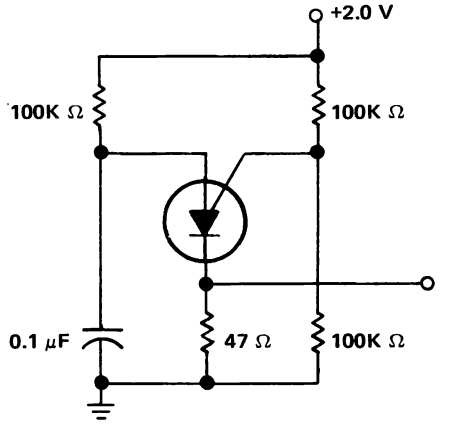


FIGURE 12. Basic Relaxation Oscillator Circuit Using PUT

CIRCUIT APPLICATIONS OF THE PUT

The following circuits show the wide range of applications in which the PUT can be used.

Figure 12 shows the PUT used in a basic relaxation oscillator. This circuit is the same circuit described earlier. This one, however, shows typical components values. Note the low voltage operation of this circuit. The PUT can be used in circuits with supply voltages as low as 2.0 volts and as high as 40.0 volts.

Figure 13 shows the PUT used in a typical timing circuit. In this circuit, when S1 is closed, capacitor C1 charges to V_P and triggers the PUT. The positive output pulse at the anode turns on the SCR which supplies a ground for the load.

The long delay timer shown in Figure 14 utilizes the low leakage of the Texas Instruments A7T6027 PUT. The current provided by the 500 megohm resistor is not enough to cause the Q2 to fire. But at 60 second intervals Q1

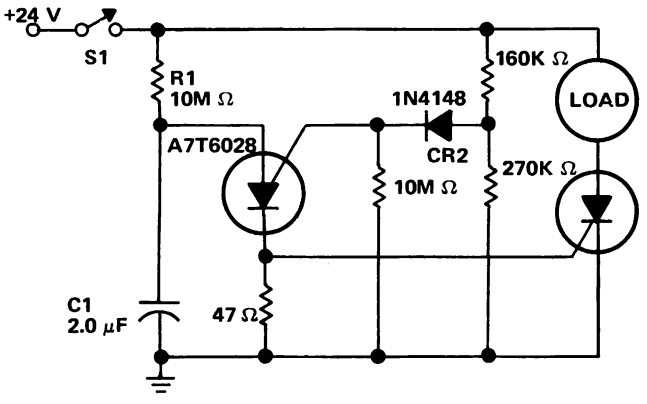


FIGURE 13. Typical PUT Timing Circuit

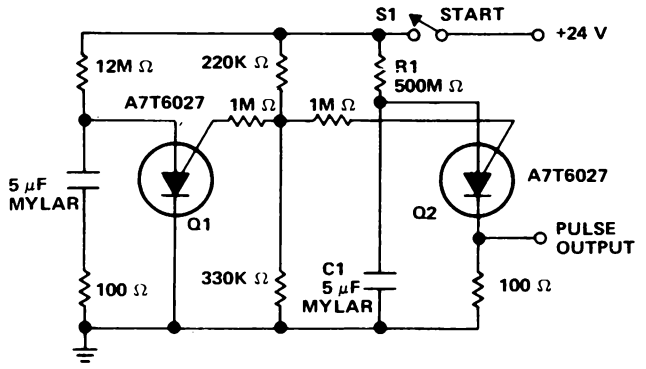


FIGURE 14. A Long Delay Timer PUT Circuit

triggers and causes the gate of Q2 to go to a slightly lower voltage. When the capacitor has reached this voltage, $+V_T$, Q2 triggers. The triggering current will come from the capacitor instead of the series resistor.

The voltage controlled oscillator illustrated in Figure 15 has numerous applications. An important advantage of this circuit is the high impedance at the control terminal. This point can be driven directly by a high impedance voltage source. The frequency change and voltage change are linear through a large dynamic range. The 2N2222 transistor is used to shape the output pulse and control its amplitude.

Figure 16 shows a Texas Instruments A7T6027 PUT used in a unique low cost zero crossing detector. In this circuit a PUT is used to obtain an output pulse every 360 degrees at zero crossing as shown in Figure 16(b). The circuit is reliable and provides excellent line voltage rejection. A

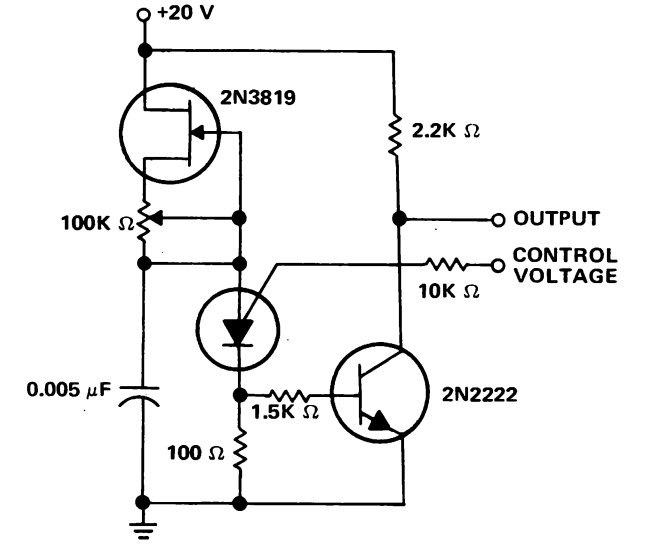


FIGURE 15. Voltage Controlled Oscillator

twenty per cent change in line voltage results in a change in phase of less than one degree. The potentiometer R1 allows a phase adjustment of approximately ±5 degrees.

The circuit in Figure 17 eliminates contact bounce which can cause false triggering of logic circuits. When S1 is closed, the capacitor charges to V_P and triggers the PUT. The device is programed so that I_V will be exceeded and the PUT will be in a stable condition. Thus, only one pulse will be generated at the output.

A method which has been used successfully to extend the operating range of a conventional UJT and which can be applied to a PUT is shown in Figure 18. The 2N3724 npn transistor helps to discharge the capacitor C and increase valley current. This technique enables smaller values of resistor R to be used, increasing the dynamic range of the PUT circuit.

Figure 19 shows a TI A7T6027 PUT used in an inexpensive, one-capacitor multivibrator circuit. Usually two large capacitors are required in multivibrator design. This circuit needs only one inexpensive film (Mylar) capacitor C1. The output symmetry can be adjusted with the timing resistors R1 and R2. At the start of the cycle, Q1 is off. C1 is charged through R1 until V_P is reached whereupon the PUT is triggered turning off Q2. The collector of Q2 goes toward supply. The combination of CR2 and R3 supply latching current for the PUT. When C discharges through R2, Q2 is turned on thereby removing the latching current from the PUT. The gate will rise to the voltage set by R4 and R5 and the cycle will repeat.

A retriggerable one shot circuit using a PUT is shown in Figure 20. A positive pulse is available at point B when a positive input pulse is received at point A . The output will remain high if another input pulse is received before the end of the timing cycle. Initially, the PUT is in conduction; hence the anode and gate are at approximately ground potential. When a positive pulse is applied at A ; the 2N2222 discharges the capacitor and unlatches the PUT. The gate then goes positive to a voltage set by R1 and R2. When the 2N2222 turns off the capacitor charges to V_P and fires the PUT thereby pulling the gate back to ground. At any time during the charge portion of the cycle if another pulse is received at point A the capacitor is discharged and the timing is started again.

DEFINITION OF PARAMETERS

I_P Peak-Point Current – The minimum current required to cause the PUT to go into conduction. (Figure 3.)

V_T Offset Voltage – Offset voltage is the difference in voltage between V_S and anode voltage when the device triggers. $V_T = V_P - V_S$ (Figure 3).

I_V Valley-Point Current – The region where the transition is made from the negative resistance region to the positive resistance region. $dV/dI = 0$ (See Figure 3.)

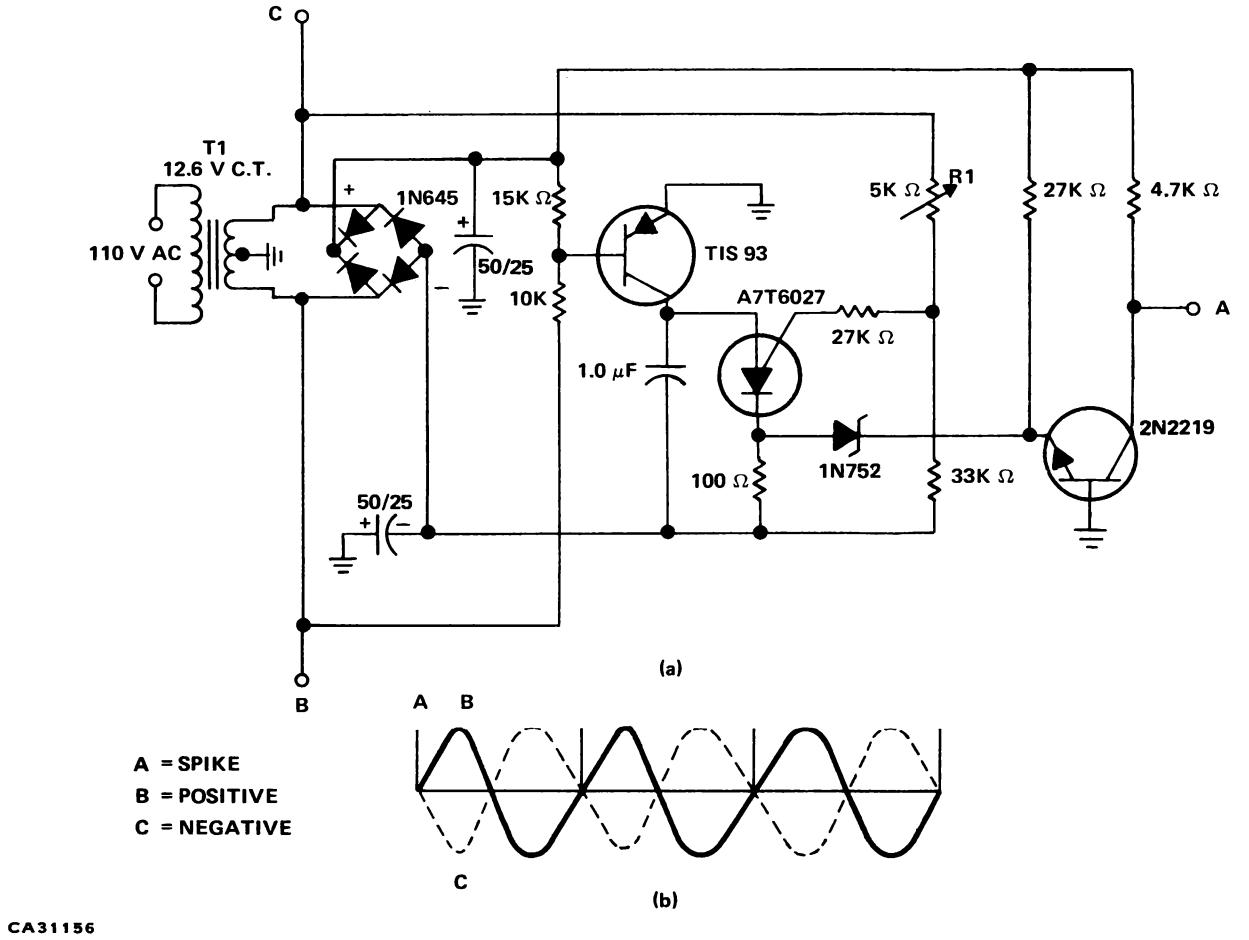


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FIGURE 16. Low Cost Zero Crossing Detector

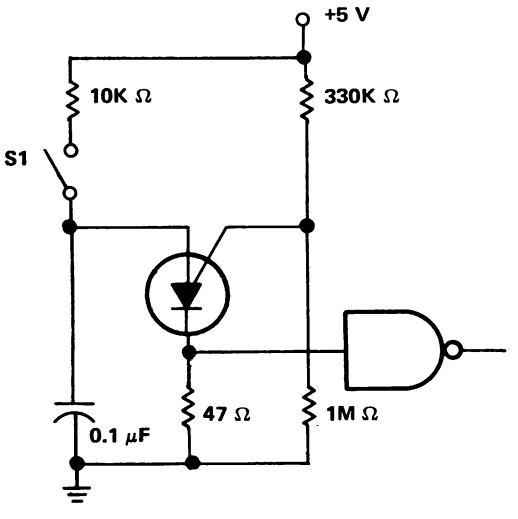

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FIGURE 17. Switch Bounce Eliminator Circuit

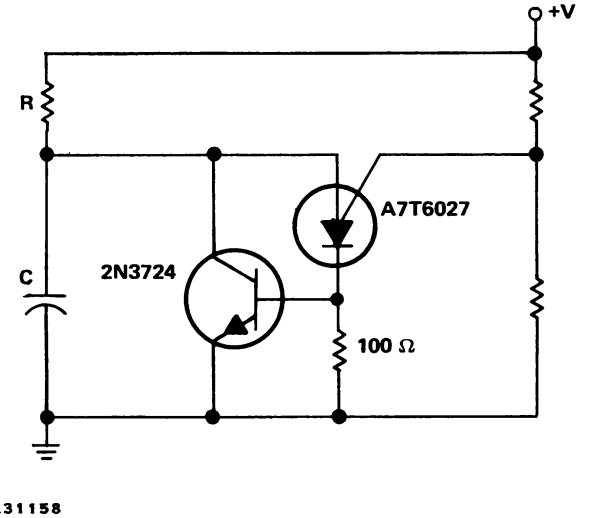

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FIGURE 18. PUT Circuit To Extend Operating Range of Conventional UJT

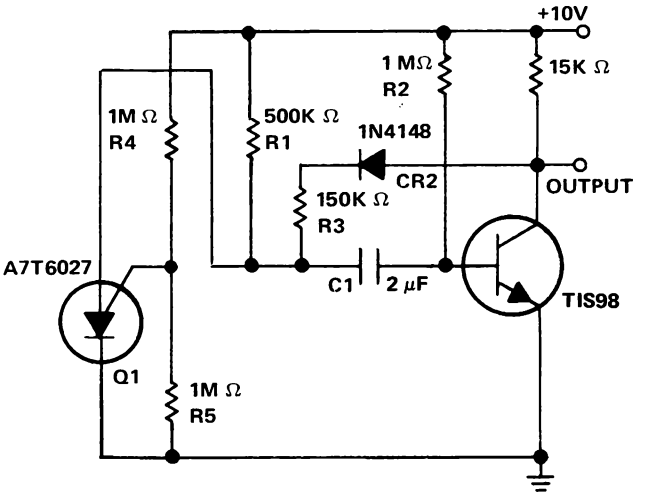


FIGURE 19. Inexpensive One-Capacitor Multivibrator

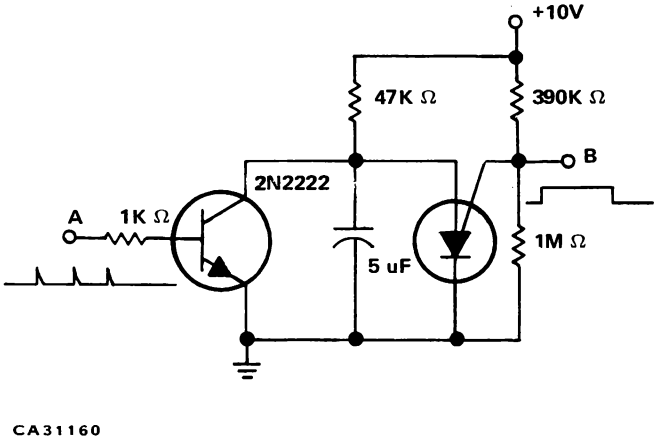


FIGURE 20. PUT Retriggerable One Shot Circuit

IGAO Anode to Gate Leakage – Anode to gate leakage current with the cathode open. (Figure 11(a).)

IGKS Gate to Cathode Leakage – Gate to cathode leakage with the cathode and anode shorted together. (Figure 11(b).)

VF Forward Voltage – Voltage between the anode and cathode at a specified current. (Figure 3.)

VO Pulse output Voltage – The peak voltage measured across a resistor in series with the cathode when the PUT is operating as a relaxation oscillator under specified conditions. (Figure 11(c).)

t_r Rise Time – The time required for the output voltage taken across a resistor in series with the cathode, to go from one specified value to another. (Figure 11(c).) while operating under specified conditions.

REFERENCES

1. Texas Instruments Application Report CA-66, "SCR Switching Methods," Smith, Carroll, August, 1969.
2. Texas Instruments Application Report CA-68, "The How and Why of Unijunction Transistors," Crawford, R. H. and Dean, R. T., March, 1969.

TEXAS INSTRUMENTS

TV design considerations using High gain dual-gate MOSFET's (CA 173)

TV DESIGN CONSIDERATIONS USING HIGH GAIN DUAL-GATE MOSFETS

Sam Weaver

Dual-Gate MOSFETS have been in existence for several years. Three years ago a two-stage IF was designed using the SFB 8970, later to be registered as the 3N201, 3N202, and 3N203 series. Admittedly, it's performance was marginal having a sensitivity of 700 μV for 1 volt of output video. Also, the maximum video output without clipping was only 2 volts.[1]

At the same time, a complete high frequency section for a color TV was designed using MOSFETS in the RF amplfier, mixer and two stages of a three-stage IF. The performance was excellent with the exception of the VSWR. Performance of the tuner is shown in Table I. Overall AGC performance is shown in Figure 1. Total gain reduction was greater than 110 dB on channel 2 and slightly over 100 dB on channel 11.[2]

TV manufacturers were very cautious about using the new MOSFETS in their designs. However, they did appear. One manufacturer used one as an RF amplifier with a

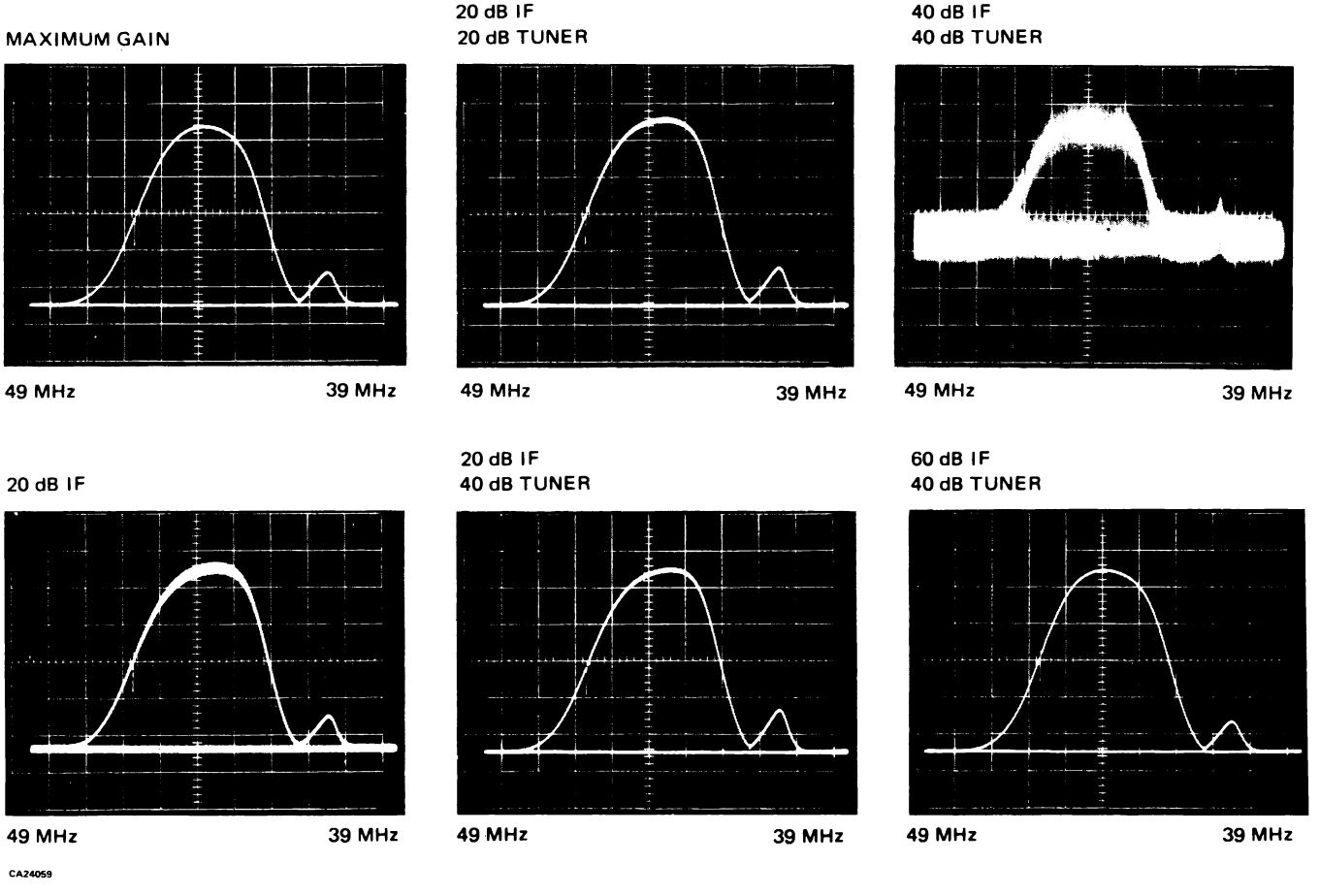


FIGURE 1. Overall Response Curves for Different AGC Points: Vertical Scale is 1 V per Division; Horizontal Scale is 1 MHz per Division

cascade bipolar mixer; another used one as a mixer with a common-base bipolar RF amplifier; still another used one as two stages of a three-stage IF amplifier. Now there appear tuners with both RF and mixer using dual-gate amplifiers.

THE HIGH TRANSCONDUCTANCE 3N211

Now for the first time a high performance two-stage IF with the 3N211, and 3N213, operating with a tuner using the 3N211 and 3N212 can meet all the requirements of a top-of-the-line TV set. A comparison of the 3N201 series with the improved 3N204 series and now the 3N211 series is shown in Table 2. Looking at Figure 2 the schematic of the high frequency section designed three years ago using the 3N201, we find that the RF amplifier gain can be increased by 8 dB, the mixer by 6 dB, and the two IF stages by 8 dB and 6 dB respectively. Since the

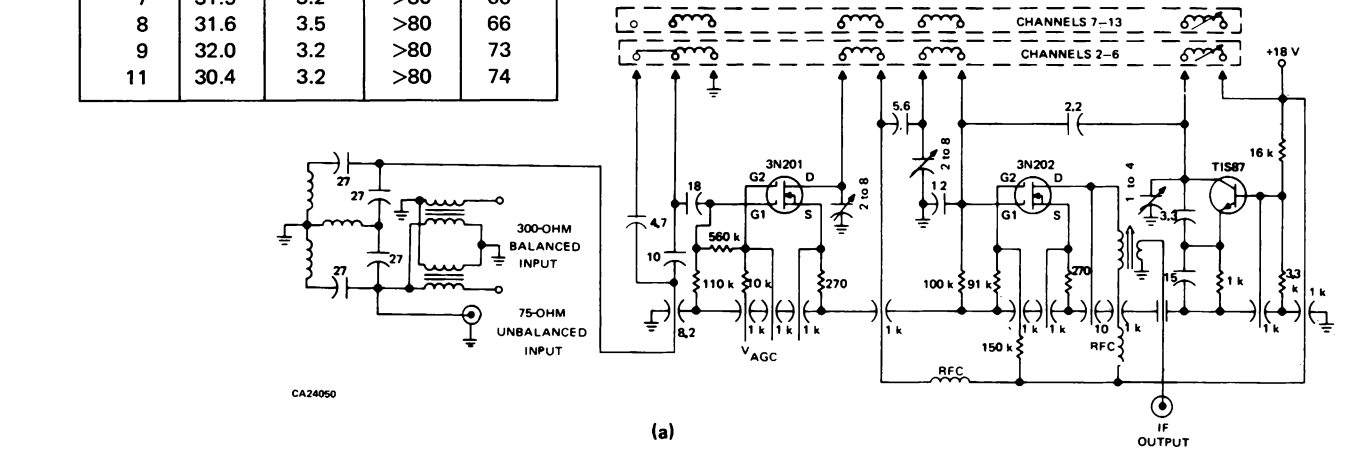
Table I. Performance of Tuner

Channel	Power Gain (dB)	Noise Figure (dB)	IF Reject. (dB)	Image Reject. (dB)
2	35.0	2.0	>90	79
4	32.2	2.4	>90	64
5	32.2	2.5	>90	70
7	31.5	3.2	>80	66
8	31.6	3.5	>80	66
9	32.0	3.2	>80	73
11	30.4	3.2	>80	74

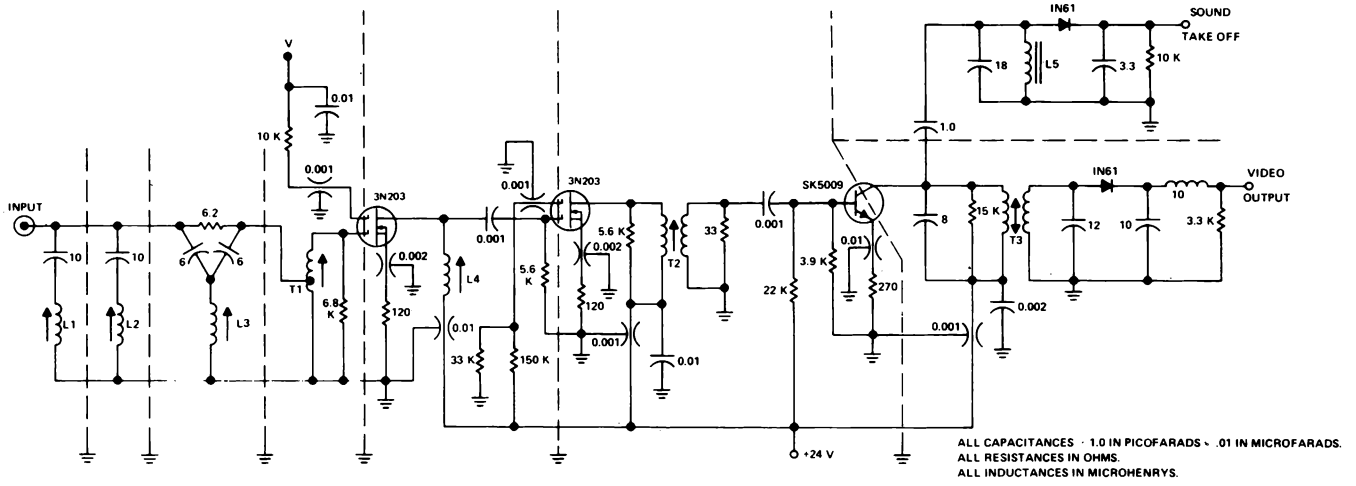
Table 2. Gain Performance of Dual-Gate MOSFETS

	3N201	3N204	3N211 3N213*	
RF Amplifier (200 MHz)	20	24	28	dB
Mixer (200-45 MHz)	18	21	24	dB
AGC-IF (45 MHz)	24	28	32	dB
Second IF (45 MHz)	24	28	–	dB
Output IF (45 MHz)	24 Bipolar 30	–	30	dB

*3N213 APPLIES ONLY TO OUTPUT IF



(a)



NAME	FREQ	Quu	L	TURNS	WIRE SIZE	FORM
L1: ADJACENT PIX	39.75 MHz	130	1.5 μH	17	30	1/4" DIA
L2: SELF SOUND	41.25 MHz	170	1.5	17	24 (Spaced)	1/4" DIA
L3: ADJACENT SOUND	47.25 MHz	115	0.95	11	26	1/4" DIA
L4: INTERSTAGE	44.00 MHz	110	1.78	17	30	1/4" DIA
L5: SOUND TAKEOFF	41.25 MHz	122	0.8	7	30	1/4" DIA
T1: 1ST STAGE INPUT	44.00 MHz	87	2.66	16/1.5	30	1/4" DIA
T2: INTERSTAGE	44.00 MHz	90	3.95	24/1.5	30	1/4" DIA
T3: OUTPUT	44.00 MHz	105 P / 120 S	1.41 P / 0.78 S	11/7	34	1/4" DIA

(b)

FIGURE 2. High Frequency TV Section: (a) Dual-Gate MOSFET VHF Tuner, (b) Dual-Gate MOSFET Model

bipolar IF output stage provided 30 dB of gain, we have within 2 dB the equivalent gain now provided by the increased performance of the new dual-gate MOSFET series.

CONSTRUCTION

Gain:

Simplified equations for the y parameters have been derived from the models shown in Figure 3. These equations are shown in Figure 4. From basic MOSFET theory,

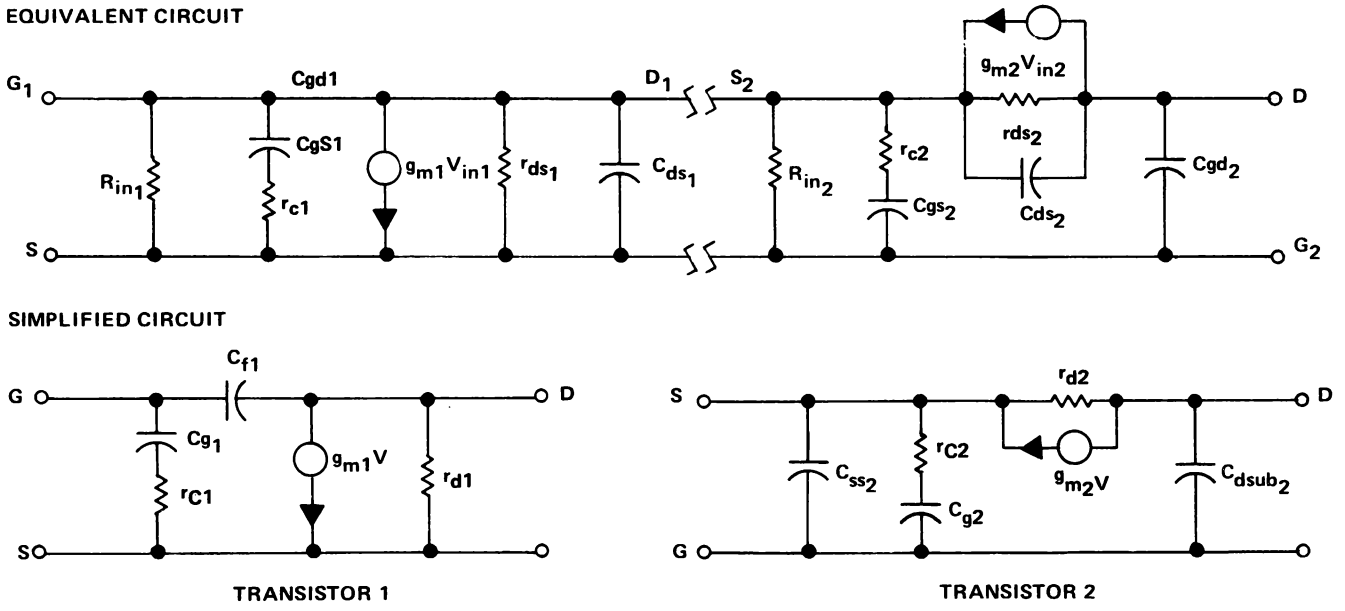
$$g_m = \frac{W}{L}\frac{E_o}{t_{ox}} \bar{u}_n \left[-V_{GS(OFF)}\right] \quad (1)$$

where W and L are width and length, respectively, of the channel; t_{ox} is the oxide thickness; E_o its dielectric constant; and $\bar{u}_n$ is the effective electron mobility. To obtain the high value of gain desired for this device, Y_{12} is maximized, meaning g_{m1} is maximized. Figure 5 shows the geometry of the device and the very large W/L ratio used to get high g_m. The oxide is made as thin as possible while maintaining reliability, and $\bar{u}_n$ is made high by special annealing to minimize interface states.

Noise:

Figure 6 shows the equation for noise factor of the dual-gate MOSFET which describes the noise behavior of the 3N201, 3N204, and 3N211 MOSFETs at frequencies above the point where 1/f noise is negligible up through the useful frequency range of the devices. To minimize noise figure, g_{m1} is maximized, corresponding to the identical process for maximizing of gain. In addition, to extend the frequency range, L_1 is made smaller than L_2 consistant with maintaining large g_{m2}. C_T is made as small as possible by minimizing the gate metal overlap of the center region, by keeping the oxide over the center region as thick as possible, and by making the center region diffusion as thin as possible.

Note that to describe the noise factor properly, the g_{11} in the noise equation is less than the g_{11} in the y parameter equation. This apparent discrepancy is necessary since the actual noise figure of the dual-gate MOSFET may be less than 3 dB under a condition of power matching. (The typical noise figure of the 3N211 at 200 MHz under power matched conditions is very close to 3 dB, but the 3N204 is typically 2.6 dB.) This phenomena may be explained by the distributed nature of the channel resistance. The signal (with input noise) is applied across the entire gate and receives a certain amplification. But the noise generated by the channel resistance near the source receives much less amplification while that generated near the drain, where the channel is narrowed by the gate-source bias voltage, receives more amplification. The result is that the MOSFET presents a real component of impedance to the signal which does not correlate to a thermal-noise



APPROXIMATE EQUATIONS:

$Y_{11} = \omega^2 C_{g1}{}^2 r_{c1} + j\omega C_{f1}$	$Y_{11} = 1/r_{d2} + g_{m2} + j\omega(C_{ss2} + 1/2\ C_{g2})$
$Y_{12} = -j\omega C_{f1}$	$Y_{12} = -1/r_{d2}$
$Y_{21} = g_{m1} - j\omega(C_{f1} + 1/2\ C_{g1})$	$Y_{21} = 1/r_{d2} - g_{m2} + j\omega(1/2\ C_{g2})$
$Y_{22} = 1/r_{d1} + j\omega C_{f1}$	$Y_{22} = 1/r_{d2} + j\omega C_{dsub2}$

FIGURE 3. Dual-Gate MOSFET Model

$$Y_{11} = \omega^2 C_{g1}{}^2 r_c + \frac{\omega^2 C_{f1}\,[g_{m2}\,(C_{f1} + 2/5\,C_{g1}) + g_{m1}\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})]}{g_{m2}{}^2 + \omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})^2}$$

$$+ j\omega \left[\frac{g_{m1}g_{m2}C_{f1} - \omega^2 C_{f1}\,(C_{f1} + 2/5\,C_{g1})(C_{f1} + C_{SS2} + 3/5\,C_{g2})}{g_{m2}{}^2 + \omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})^2} + C_{f1} + C_{g1} \right]$$

$$Y_{12} = -\frac{1}{r_{d2}} \left[\frac{\omega^2\,C_{f1}\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})}{g_{m2}{}^2 + \omega^2 (C_{f1} + C_{SS2} + 3/5\,C_{g2})^2} \right] - j\omega \frac{C_{f1}}{r_{d2}} \left[\frac{g_{m2}}{g_{m2}{}^2 + \omega^2 (C_{f1} + C_{SS2} + 3/5\,C_{g2})^2} \right]$$

$$Y_{21} = \frac{g_{m1}g_{m2}{}^2 - 2/5\,\omega^2\,g_{m2}\,C_{g2}(C_{f1} + 2/5\,C_{g1}) - \omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})(2/5\,g_{m2}\,C_{g1} + g_{m2}C_{f1} + 2/5\,g_{m1}C_g)}{g_{m2}{}^2 + \omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})^2}$$

$$-j\omega \left[\frac{g_{m1}g_{m2}(C_{SS2}+C_{f1}+C_{g2}) + 2/5\,g_{m1}g_{d1}C_{g2} + g_{m2}^2\,(f_1 + 2/5\,C_{g1}) - 2/5\,\omega^2 C_{g2}(C_{f1} + 2/5C_{g1})(C_{SS2} + C_{f1} + 3/5C_{g2})}{g_{m2}^2 + \omega^2 (C_{SS2} + C_{f1} + 3/5\,C_{g2})^2} \right]$$

$$Y_{22} = \frac{1}{r_{d2}} \left[\frac{\omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})\,(C_{f1} + C_{SS2} + C_{g2})}{g_{m2}{}^2 + \omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})^2} \right]$$

$$+ j\omega \left\{ C_{dsub2} + \frac{1}{r_{d2}} \left[\frac{g_{m2}\,(C_{f1} + C_{SS2} + C_{g2})}{g_{m2}{}^2 + \omega^2\,(C_{f1} + C_{SS2} + 3/5\,C_{g2})^2} \right] \right\}$$

$$g_m = \frac{W}{L} \frac{e_o}{t_{ox}} \bar{\mu}n \left(-V_{GS(OFF)}\right) \qquad r_c \approx \frac{2}{5\,g_m}$$

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FIGURE 4. Y-Parameters of the Dual-Gate MOSFET

resistance.

At 200 MHz this phenomena is good news. And with some detuning the noise figure can be lowered to a typical 2.2 dB for the 3N211 and 2.0 dB for the 3N204. At the lower TV channel frequencies, however, the situation becomes quite complicated. If the input circuit is adjusted for minimum noise figure at 45 MHz, the typical value is 1.5 dB for both FETs. But the mismatch caused by the extremely high input impedance is so high that excessive standing wave ratios are encountered. Actually, because of feed back in the first device (transistor number 1 in Figure 3), the FET is not unconditionally stable, and power matching becomes impossible. A compromise is necessary, resulting in higher noise figures at the low channels than at the high channels in a properly designed VHF TV tuner.

Y–PARAMETERS

Figure 7 shows the typical transfer functions vs frequency for these devices. The transimpedance Y_{21} is shown for the 3N213 separately from the other devices. Its higher breakdown voltage requires a tradeoff in Y_{21}. The other Y parameter curves are typical for all devices.

Note that although ReY_{21} decreases with frequency, the numerical value of Im Y_{21} increases such that $|Y_{21}|$ remains almost constant to beyond 400 MHz. The feedback parameter Y_{12} has some very unusual characteristics. The feedback increases very rapidly with frequency, but is so small that below 300 MHz it cannot be accurately measured with present commercial equipment. Extrapolating the curves to 200 MHz shows the feedback to be equivalent to a resistor greater than 100K and a capacitor less then

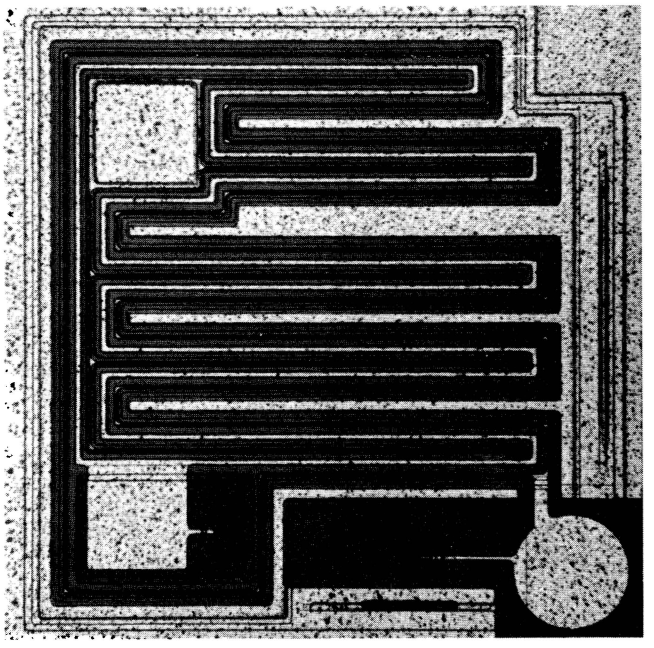

FIGURE 5. Geometry of the Dual-Gate MOSFET

$$F = 1 + \frac{g_{11}}{g_s} + \frac{(g_{11} + g_s)^2}{g_s} R_N$$

where

g_s = generator impedance

g_{11} = input conductance of the grounded-source transistor (transistor #1) given by this equation:

$$g_{11} = \frac{(\omega C_{g1})^2}{2\, g_{m1} \left[1 + \left(\frac{\omega C_{g1}}{2\, g_{m1}}\right)^2\right]}$$

and where

$$R_N = \frac{2}{3\, g_{m1}} \left[1 + \left(\frac{L_1}{L_2}\right)^2 \left(\frac{\omega C_T}{g_{m2}}\right)^2\right]$$

and

L_1, L_2 are the gate lengths of transistors 1 & 2 respectively C_T is the total centerpoint to ground capacity

$C_T = C_{ds1} + C_{gs2} + C_{sub}$

C_{sub} is the capacitance between the substrate and and the junction of drain 1 and source 2 and the other symbols are as defined by the model in Figure 3.

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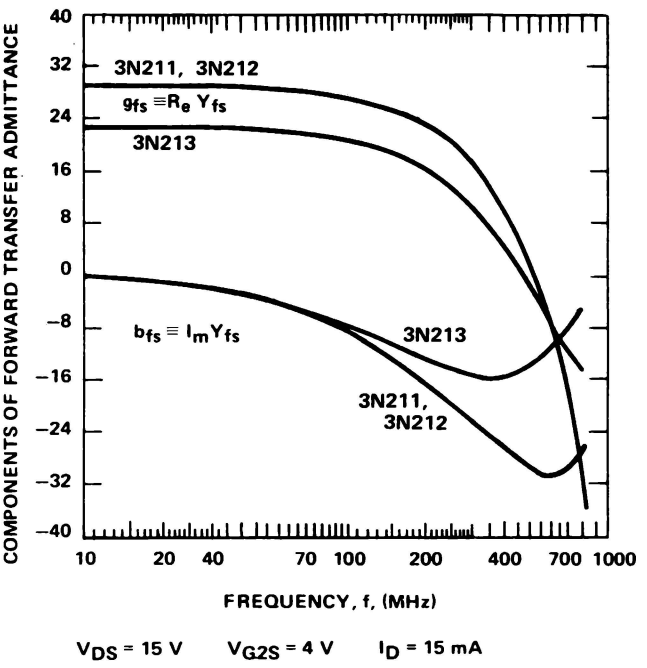
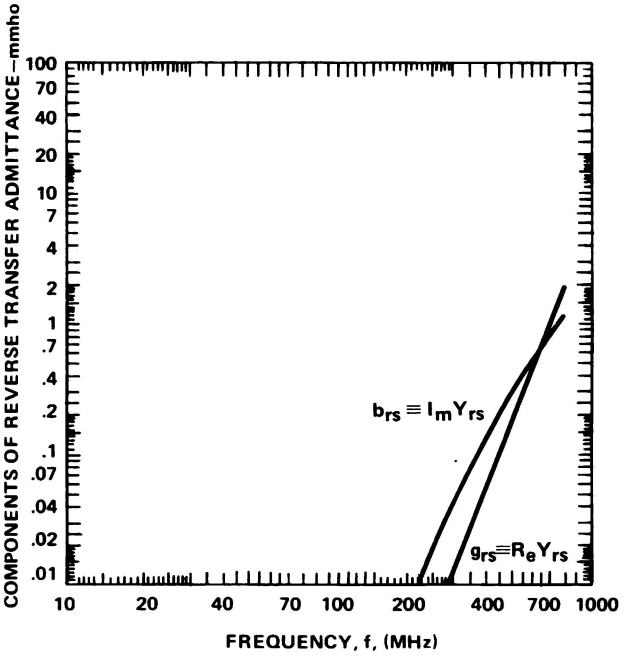
FIGURE 6. Noise Figure Equation of the Dual-Gate MOSFET



(a) Forward Transfer Admittance Versus Frequency



(b) Reverse Transfer Admittance Versus Frequency

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FIGURE 7. Components of Small-Signal Common-Source Gate-One

0.03 pF, in parallel, connected between drain and gate-one. Such a small amount of feedback eliminates the need for neutralization.

Because of the very high input and output resistances, however, the feedback is not negligible and shows up in the Y_{11} and Y_{22} characteristics. Figure 8 shows the results of

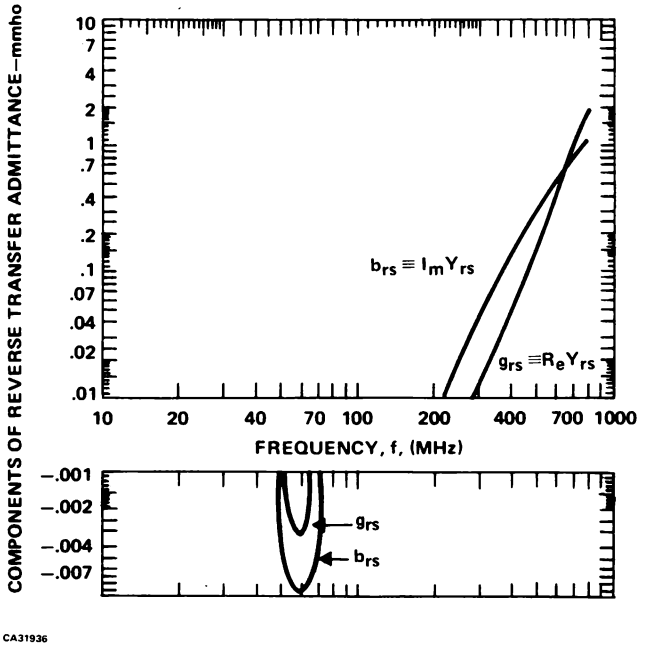


FIGURE 8. Components of Small-Signal Common-Source Gate-One Reverse Transfer Admittance Versus Frequency

an attempt to measure Y_{12} at the lower frequencies. Because of the very large change in value between 300 MHz and 800 MHz, the parameter is plotted on log-log paper. (At 800 MHz the feedback is equivalent to a 500-ohm resistor in parallel with 0.3 pF.) However, the function does go through zero, and reaches a detectable negative value at 60 MHz. Detectable, in this case, means that a null was reached with a change of less than an estimated one-tenth of a division on the GR 1607 Immittance Bridge with a X0.1 multiplier plate. There was no detectable feedback at 45 MHz and only one device out of 15 characterization samples showed a detectable value at 70 MHz. The lower portion of the graph is the best estimate of a typical value at the lower frequencies.

All of this measurement is purely academic since even the best layout in a practical circuit will provide enough feedback to swamp the internal feedback of the device at these low frequencies.

The feedback of the first transistor of the cascode structure causes a conditionally unstable state as mentioned above. This feedback, not the overall feedback, causes the peculiar characteristics observed in the input and output admittance parameters shown in Figure 9. The real part of Y_{11} and Y_{22} goes toward zero, and in some devices a negative real part is observed. Because of this zero conductance, external loading in the 60-MHz region is required to provide the proper bandwidth. Calculated values of bandwidth assuming zero conductance are greater than that actually obtained in practice. In the final section of this paper a comparison is made between the calculated performance and the actual performance of a practical breadboard of a TV IF amplifier.

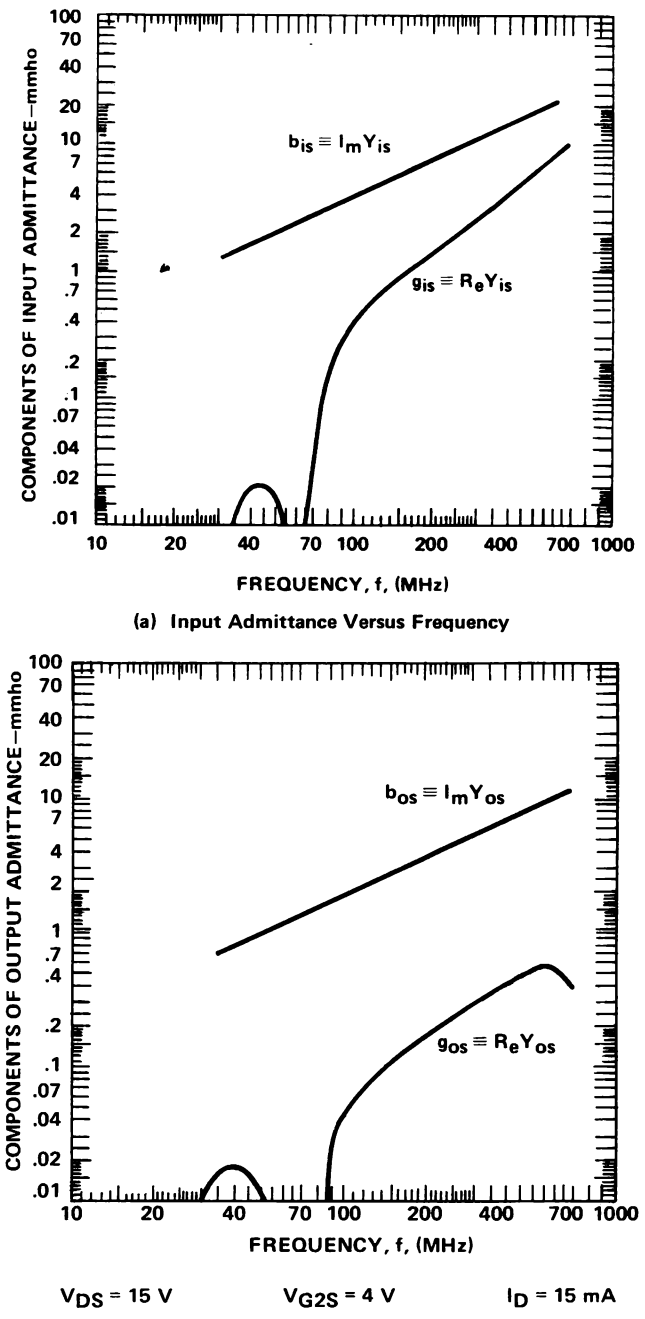


FIGURE 9. Components of Small-Signal Common-Source Gate-One

This feedback phenomenon was also present in the original dual-gate MOSFETS, but the gain was not sufficiently high to make it significant.

A caution which must be observed in the application of the dual-gate MOSFET, and especially for the high g_m units, is seen in the simplified Colpitts type oscillator schematic in Figure 10. The capacitances shown are those of the chip. The input and output tuning coils resonate with the chip capacitances. The external source impedance is any impedance that may be present due to insufficient by-passing of the source. One may inadvertently have an

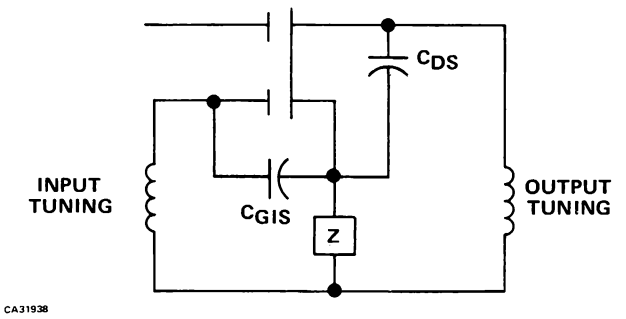


FIGURE 10. Simplified Colpitts Type Oscillator

excellent oscillator depending upon the size and type of impedance present in the source. I recommend ac grounding the case in any amplifier application to minimize this possibility.

BIASING FOR MINIMUM CROSS MODULATION

Cross-Modulation in the TV RF amplifier and mixer has became a very important consideration in tuner design. This phenomena arises from the third-order effects in the transfer characteristic of the amplifier. Figures 11 and 12 show the transfer characteristic of a typical 3N211, having an I_{DSS} of approximately 15 mA. The first derivative of this characteristic is Y_{fs} vs V_{G1S} and is shown in Figure 13 for a typical device. The drain characteristics are measured with pulse techniques and the Y_{fs} is measured at 1 KHz. The inflection points on the curves of Figures 11 and 12 appear as maximum points on the curves of Figure 13, within the accuracy of measurement.

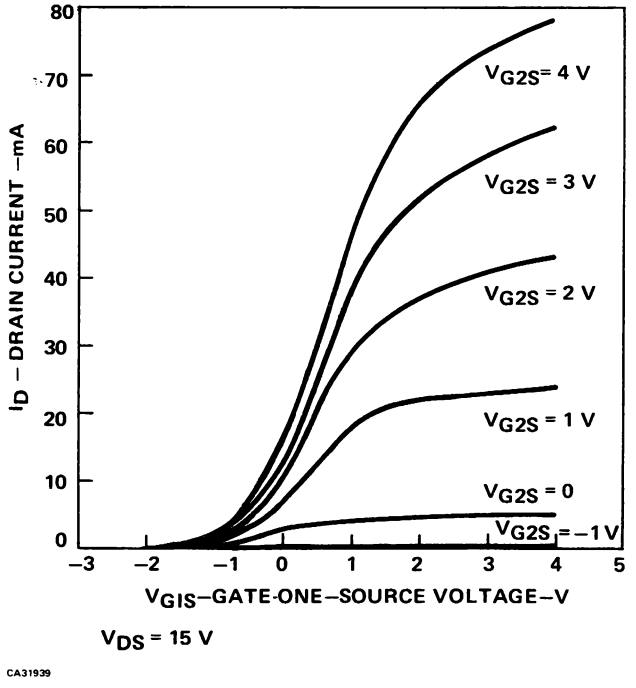


FIGURE 11. Transfer Characteristic of a Typical 3N211 Dual-Gate MOSFET

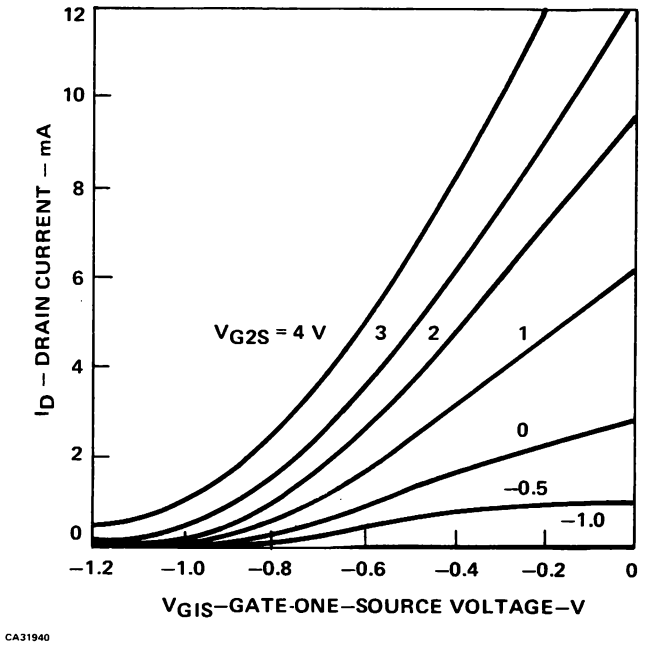


FIGURE 12. Transfer Characteristic of a Typical 3N211 Dual-Gate MOSFET

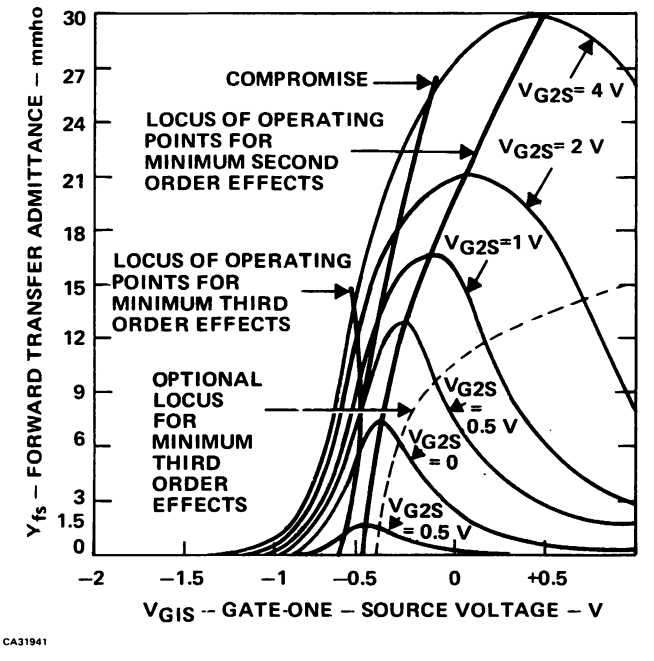


FIGURE 13. Y_{fs} Versus V_{GIS} of a Typical 3N211 Dual-Gate MOSFET

The maximum points on the Y_{fs} curve would appear as zero points on the derivative of Y_{fs} or as points of minimum second-order effects. A locus of operating points for minimum second-order effects is shown. You would not want to bias a mixer at any of these points but rather at a point where the slope is a maximum.

The maximum slope occurs at the inflection points of the Y_{fs} curve which are the zero points of the second derivative of Y_{fs}, or third derivative of I_D. Therefore, a line drawn through these points is the locus of operating points

for minimum third-order effects (and maximum second-order effects).

For this typical device, then, having $V_{G1S(off)}$ = 1.8 volts at V_{G2S} = 4 volts and V_{DS} = 15 V, the optimum operating point for a mixer is V_{G1S} = −0.55 volts, corresponding to $I_D \approx 6$ mA as seen from Figure 12. One could get more conversion gain by increasing gate-two voltage to a point near the zener breakdown of the protective diodes (6 volts minimum) and determining the inflection point on the Y_{fs} vs V_{G1S} curve at this V_{G2S} value.

For an RF amplifier undergoing AGC, and for minimum cross modulation, the AGC bias should follow the locus of points for minimum third order effects. Unfortunately, following this line does not allow one to realize the maximum gain potential of the device, and a compromise is necessary. Fortunately, a compromise which does not drastically degrade crossmodulation performance and allows a relatively simple biasing scheme is available. In the appendix a biasing scheme is worked out to provide the approximate locus of operating points shown on the compromise line in Figure 13. The values are shown in Figure 14. The points at $V_{G2S} = 4$, $V_{G1S} = -0.15$, at $V_{G2S} = 1$, $V_{G1S} = -0.40$ and at $V_{G2S} = -0.6$, $V_{G1S} = -0.6$ are the exact points taken to derive the bias resistor values. More complex schemes could provide four or five exact points.

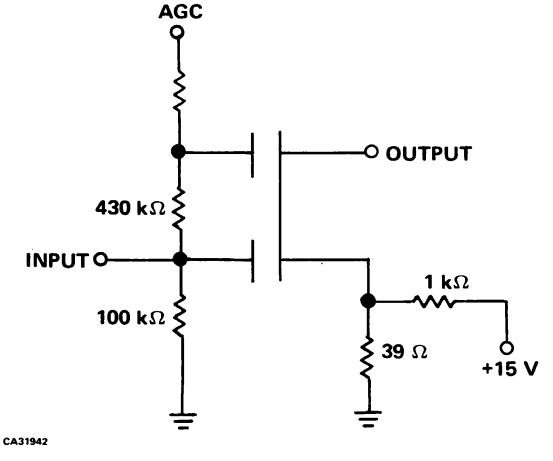


FIGURE 14. RF Amplifier Bias

The optional locus for minimum cross modulation could be used. However, the utilization of the high gain characteristics of this device would require excessive I_D. An operating point at $V_{G2S} = 2$ V, and $V_{G1S} = 0.6$ volts, for example, where the g_m is only 17 mmhos, causes $I_D = 20$ mA.

MIXER OPTIMIZATION

The bias point for maximum mixing action has been given in the previous section. However, mixer conversion gain is also very dependent on local oscillator injection voltage; the optimum injection voltage for maximum gain is so large that it causes an increase in I_D. The result is that the increased drop across the source resistor moves V_{G1S} and V_{G2S} off the desired operating point. The resistor must then be decreased to restore this point. Then, of course, the I_D increases even more. A practical method of optimizing for conversion gain is to use a well-bypassed variable source resistor and maintain the constant voltage necessary to set V_{G1S} and V_{G2S} at the proper values while adjusting the local oscillator voltage for the optimum value.

REVIEW OF DESIGN PROCEDURE FOR TWO-STAGE IF

Because of the high Y_{fs}, high input and output impedances, and the low feedback, the design equations are very simple. The broad bandwidth of the TV IF requires relatively low load resistances, so that the shunting effect of ReY_{11} and ReY_{22} is small enough to be neglected. (Refer to Texas Instruments Application Report CA-133 for the effects of ReY_{11} and ReY_{22}.)

Output Stage:

A double-tuned output circuit with approximately equal primary and secondary Q's will be used in this design to provide the proper bandpass characteristics. Given an equivalent detector load impedance, R_{DL}, the proper Q, known from bandwidth requirements, can be established. The additional primary resistive loading can be determined from the equivalent output capacitance of the FET.

Because of the high gain available, an additional compromise may be made to increase the video output level. The voltage swing on the FET is limited by its breakdown, $V_{(BR)DS}$ but additional resistive loading at the collector will allow more current swing, delivering more power into the matched secondary, and thus to the detector. The additional loading, of course, decreases the gain of the stage, but it also linearizes the stage, producing less second and third order effects. Additional capacitance in parallel with the decreased loading resistor will be required to maintain the proper value of Q. The sound detector signal may be taken off the collector, providing a portion of the loading. The self-sound trap may be placed in the secondary before the video detector to eliminate 4.5 MHz sound in the video.

Interstage

The interstage may consist of a single-tuned circuit with the bias resistors of the output FET providing the proper 45 MHz loading to establish the proper bandwidth. Total capacitance shunting this resistance is C_{OSS}, the output capacitance of the first FET, in parallel with C_{ISS}, the input capacitance of the second FET.

Input

The input circuit contains the adjacent sound and picture traps and matches the impedance of the signal from the mixer to the impedance of the loading resistors required to establish the desired bandwidth. Again, the loading

resistors may consist of the bias resistors of the stage unless they present too large a current drain on the AGC system. In this case, a separate loading resistor decoupled from gate-one is required. Since the gates do not draw current the loading on the AGC circuit may be made as small as desired with a separate decoupled loading resistor.

45 MHz IF CIRCUIT DESIGN

Design equations:

1) Voltage gain step-up from mixer to input of first FET:

$$V_1 = \sqrt{R_{L1}/R_S} \quad (2)$$

Where R_{L1} is the equivalent 45 MHz load at gate-one and R_S is the signal impedance from the mixer.

2) Voltage gain in first FET (3N211):

$$V_2 = Y_{fs}R_{L2} \quad (3)$$

Where R_{L2} is the equivalent 45 MHz load at the drain of the first FET, which is also at the gate-one of the second FET (3N213).

3) Voltage gain in second FET:

$$V_3 = Y_{fs}' R_{L3}/2 \quad (4)$$

Where R_{L3} is the equivalent 45 MHz load at the drain of the second FET, uncoupled from the secondary.

4) Voltage gain (loss) to detector input:

$$V_4 = \sqrt{R_{DL}/R_{L3}} \quad (5)$$

Where R_{DL} is equivalent detector load impedance.

5) Overall gain:

$$V_T = V_1V_2V_3V_4 \quad (6)$$

6) Sensitivity:

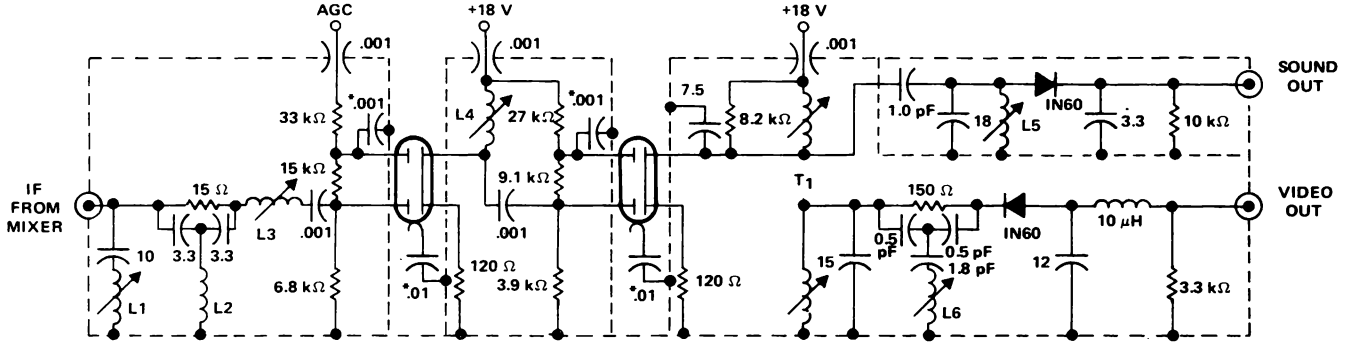
$$S = E_{DC}/V_Tn \quad (7)$$

Where E_{DC} is the detected video and n is the detector efficiency.

Performance of IF Breadboard

Design calculations for a two-stage IF amplifier are given in Appendix B, and bias resistors are calculated in Appendix C. A breadboard using essentially the values calculated and shown schematically in Figure 15 was constructed with the results shown in Figure 16. The video output available without clipping was over 6 volts, indicating that the compromise in the output stage was too much in favor of video output over gain. A reduction in output loading (increasing the drain load resistor to 12K) would increase the gain by 2 dB, if we assume negligible loading by the sound detector, giving a sensitivity of 250 μV instead of the measured 300 μV. Because of the bandwidth narrowing effect described above in the discussion of the y parameters, this reduced loading would, however, decrease the interstage bandwidth and increase the skewing with AGC.

The bandwidth in the input and interstage tuned circuits were reduced from the calculated 10 MHz to about



L1: 21T =34 DOUBLE-SPACED, 7/32" CARDBOARD FORM
L2: 14T =26 7/32" CARDBOARD FORM
L3: 22T =30 7/32" CARDBOARD FORM
L4: 19T =30 7/32" CARDBOARD FORM
L5: 7T =30 7/32" CARDBOARD FORM
L6: 50T =36 DOUBLE-SPACED, 5/16" CARDBOARD FORM
T_1: PRI: 12T =30 } ADJUSTABLE COUPLING
SEC: 9T =30 } 7/32" CARDBOARD FORM
ALL TUNING SLUGS ARE TYPE "J"

NOTES:
*LEADLESS DISC CAPACITORS
CAPACITORS <1 IN μF, EXCEPT AS NOTED
>1 IN pF

FIGURE 15. Two-Stage TV IF Amplifier

IF Response

39.75 MHz > 30 dB down
41.25 MHz > 40 dB down
47.25 MHz > 30 dB down
42.17 MHz ~ 6 dB down
47.25 MHz = 6 dB down

Sensitivity = 300 μV for 2 V of video (carrier 85% modulated)
AGC Range = 68 dB
AGC Voltage = +7.0 volts to −7.0 volts
CA31944

FIGURE 16. Performance of Two-Stage IF

7 MHz and from the calculated 6 MHz to about 5 MHz. As a result, a slight skewing with applied AGC was noticeable. The typical device provided a maximum AGC range of 68 dB rather than the 70 dB first reported.

An attempt was made to take the 4.5-MHz sound directly from the output stage as was done in the IF described in TI Application Report CA-133. However, this stage is so linear that the 4.5 MHz being generated was negligible, and a separate sound detector is required. No attempt was made to measure the output of the sound detector.

REFERENCES

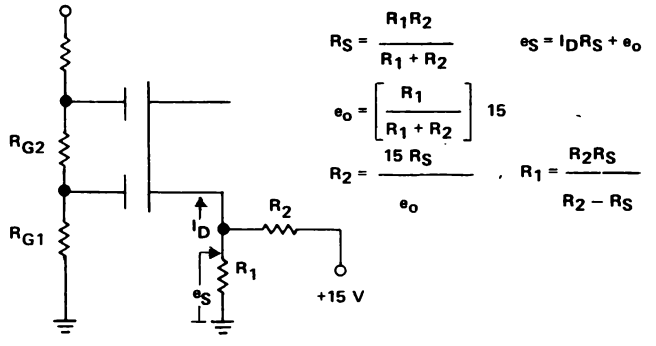
1. Weaver, Sam, "Dual-gate MOSFETs in TV IF Amplifiers," Texas Instruments Application Report CA-133, December 1969.

2. Wilcox, Don, "MOSFETs in Color Television High-Frequency Section" Texas Instruments Application Report CA-136, October 1969.

ACKNOWLEDGEMENT

The author thanks Dr. Jim Fiebiger for the information contained in the section entitled Construction.

APPENDIX A



$$e_S = I_DR_S + e_o \tag{8}$$

$$R_S = \frac{R_1R_2}{R_1 + R_2} \tag{9}$$

$$e_o = \left[\frac{R_1R_2}{R_1 + R_2}\right] 15 \tag{10}$$

$$R_1 = \frac{R_2R_S}{R_2 - R_S} \tag{11}$$

$$R_2 = \frac{15R_S}{e_o} \tag{12}$$

V_{G2} is voltage between gate-two and ground
V_{G1} is voltage between gate-one and ground
V_{G2S} is voltage between gate-two and source
V_{G1S} is voltage between gate-one and source

$$R_R = \frac{R_{G1}}{R_{G1} + R_{G2}} \tag{13}$$

$$R_{G2} = \frac{R_{G1}(1\text{-}R_R)}{R_R} \tag{14}$$

$$V_{G2} = V_{G2S} + I_DR_S + e_o \tag{15}$$

$$V_{G1S} = R_R(V_{G2}) - (I_DR_S + e_o) \tag{16}$$

$$V_{G1S} = R_R(V_{G2S} + I_DR_S + e_o) - (I_DR_S + e_o) \tag{17}$$

The locus of operating points in Figure 13 define V_{G1S} and V_{G2S} and, with Figure 12, I_{DS}. With these parameters defined, there remains an equation with three unknowns, R_R, R_S, and e_o, from which the bias resistors can be calculated. Picking three points from the locus in Figure 15, setting up three simultaneous equations, and solving will give values for R_R, R_S and e_o.

Pick the following points:

$$1)\quad V_{G2S} = 4.0, V_{G1S} = -0.15, I_D = 13 \tag{18}$$

$$2)\quad V_{G2S} = 1.0, V_{G1S} = -0.40, I_D = 3.2 \tag{19}$$

3) $V_{G2S} = -0.6, V_{G1S} = -0.6, I_D = 0.35$ (20)

The equations to be solved are these:

$$-0.15 = R_R(4.0 + 13R_S + e_o) - (13R_S + e_o) \quad (21)$$

$$-0.40 = R_R(1.0 + 3.2R_S + e_o) - (3.2R_S + e_o) \quad (22)$$

$$-0.60 = R_R(-0.60 + 0.35R_S + e_o) - (0.35R_S + e_o) \quad (23)$$

From which

$$R_R = 0.1825, R_S = 0.0371K, e_o = 0.59 \quad (24)$$

Setting $R_{G1} = 100K$,

R_{G2} becomes 430k and $R_2 = 1K$, $R_1 = 39$ ohms. (25)

APPENDIX B
CALCULATION OF IF SENSITIVITY

Input Stage

Assuming a broad bandwidth requirement of 10 MHz for minimum AGC skewing, the Q of the input circuit will be Q = 45/10 = 4.5. From Figure 9, the C_{iss} of the first FET provides $B = \omega C = 1.8$ mmhos. Since $Q = \omega CR$, the total loading resistance, including the matched impedance from the mixer, is $R_1 = 4.5/1.8 = 2.5K$. The signal load, assuming a match, is $R_{L1} = 2R_1 = 5K$. Assuming 50 ohms impedance from the mixer:

$$V_1 = \sqrt{5000/50} = 10 \quad (26)$$

First FET

From Figure 7 the y_{fs} at 45 MHz is essentially that at 1 KHz. From Figure 13 and biasing considerations, select $y_{fs} = 27$ mmhos. From Figure 11, C_{oss} of the first FET and C_{iss} of the second give B = 0.9 + 1.8 = 2.7 mmhos. For an interstage bandwidth of 6 MHz, Q = 7.5, and $R_{L2} = 7.5/2.7 = 2.8K$.

$$V_2 = (27)(2.8) = 75 \quad (27)$$

Second FET

The y_{fs} of the high-voltage FET is about 6 mmhos less than the higher gain unit. Select $y_{fs} = 21$ mmhos. After compromising for increased video output, R_{L3} is selected to be 8.2K.

$$V_3 = (21)(8.2/2) = 86 \quad (28)$$

Voltage Gain To Detector

With a measured detector efficiency, n, of 66% and a video load of 3.3K, the equivalent detector load is $R_{DL} = 3.3K/2x0.66 = 2.5K$.

$$V_4 = \sqrt{2.5/8.2} = 0.55 \quad (29)$$

Overall Gain

$$V_T = (10)(75)(86)(.55) = 37{,}300 \quad (30)$$

Sensitivity

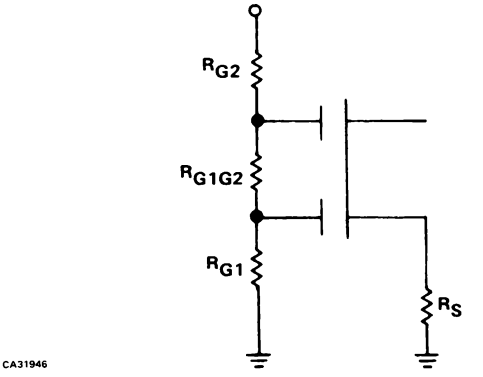
With the carrier 6 dB down on the bandpass curve, the total gain at the peak bandpass is twice the carrier frequency gain. For two volts detected video, four volts E_{DC} must be used in the sensitivity equation:

$$S = 4/37{,}300x0.66 = 0.00018 \text{ or } 180\ \mu V \quad (31)$$

With a tuner gain of 40 dB and a required sensitivity of 3 μV for the TV set, an if sensitivity of 300 μV is required. Over 4 dB additional loss may be expended in the traps of this if amplifier while still meeting the sensitivity requirements.

APPENDIX C

DESIGN OF IF AMPLIFIER BIAS



Stage One

Pick operating point at $V_{G2S} = 4V$, $V_{G1S} = 0$, (I_D = 15 mA). Read $y_{fs} = 27$ mmhos from Figure 15. From bandwidth considerations at 45 MHz, signal load should be 5K.

Let $R_S = 120$ ohms.
Source to ground voltage $e_S = (120)(.015) = 1.8V$.
For $V_{G1S} = 0$, and estimated $R_{G1} = 7.5K$,
$I_{BIAS} = 1.8/7.5K == 0.24$ mA.
For $V_{G2S} = 4V$, $R_{G1G2} = 4/0.24 = 16K$.
Total signal load $R_{L1} = (16)(7.5)/(16 + 7.5) = 5.1K$.

Stage Two

Similar operating point for the output device gives $y_{fs} = 21$ mmhos. Signal load is given as 2.8K.

Let $R_S = 120$ ohms. $e_S = 1.8V$.
Estimate $R_{G1} = 3.9K$. $I_{BIAS} = 1.8/3.9K = 0.46$ mA.
$R_{G1G2} = 4/0.46 = 8.7K$, approximately 9.1K.
$R_{G2} = (18 - 5.8)/0.46 = 26.5K$, approximately 27K.
Signal load = (3.9)(9.1)/(3.9 + 9.1) = 2.72K.

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